The Traps that cause Breakdown in Deeply Scaled SiON Dielectrics

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Abstract

We show that a minimum of two traps is required to cause breakdown in SiON films down to 10Å. At least one trap must be an interface state and at least one must be a bulk state. At low voltages, the rate limiting step for breakdown is the generation of interface traps and is controlled by the release of H^0.

Introduction

SiON remains the gate dielectric of choice for state-of-the-art silicon technologies. Although manufacturability considerations limit scaling of the physical thickness to about 12Å to ensure adequately high barrier heights with silicon [1,2], thinner equivalent oxides may be attained with the appropriate level of nitrogen incorporation. As SiON dielectrics are pushed into the extremes of scaling, it becomes increasingly important to advance the understanding of the degradation and breakdown mechanisms of these materials.

In this work, we assess the roles of bulk and interface traps in the breakdown of deeply scaled SiON films, along the mechanisms that create these stress induced defects. We will show there is a transition from bulk trap controlled to interface trap limited breakdown. While the generation of interface traps becomes the rate limiting step, we present a simple geometric model to show that both bulk and interface traps are required to form a percolation path, and provide an estimate of the bulk trap diameter. Although anode hole injection (AHI) has been shown to be a plausible mechanism below its 6eV threshold energy [3,4], we rule out AHI as the primary cause for breakdown at low V_G. Accordingly, the mechanism for breakdown and the explanation for the TDDB power law model [5] are confirmed to be due to anode hydrogen release. We show that the hydrogen species causing breakdown depends on the magnitude of the stress voltage.

Experiment

NMOS devices with 10Å to 32Å EOT PNO films from full-flow CMOS processes are stressed in inversion with V_G ranging from +2V to +4V. Gate areas from 3×10^{-9} cm^2 to 4×10^{-4} cm^2 are utilized. The generation of bulk and interface traps are monitored by SILC [6] and LV-SILC [7] respectively. For the SILC and LV-SILC measurements, gate areas $\geq 10^{-7}$ cm^2 are used to avoid the complications arising from the quantized effects of trap generation in small area devices [8].

Results

Hydrogen release from the anode during TDDB stress has been shown to be a plausible mechanism for dielectric breakdown at low voltages [9]. In a recent work, it was shown that trap generation and breakdown are triggered by the release of two hydrogen species (H^+ and H^0) from the anode in two separate anode reactions [10] as shown in Figure 1. H^+ is desorbed by holes, but H^0 could be desorbed by holes (Figure 1a) or electrons (Figure 1b). For NMOS stressed in inversion, H^+ and H^0 both create interface traps at the poly interface when they are released. After migrating into the dielectric, H^+ subsequently creates SiON bulk traps while H^0 subsequently creates pwell interface traps (Fig. 2).

To further explore the two reaction model and the roles of bulk and interface traps on SiON breakdown, we evaluate the voltage and temperature dependence of Q_{BD}, SILC, and LV-SILC. The voltage acceleration factor for Q_{BD} is defined as:

$$AF(Q_{BD}) = -\partial \ln Q_{BD}/\partial V_G \quad (1)$$

The voltage acceleration factors for SILC and LV-SILC are derived from the trap generation power law:

$$N(Q) = bQ^m \quad (2)$$

$$Q_{BD} = (N_{BD}/b)^{1/m} \quad (3)$$

Where N_{BD} is the trap density at breakdown. Inserting (3) in (1) and assuming that N_{BD} is independent of V_G, the acceleration factors for SILC and LV-SILC are:

$$AF(N(Q)) = (1/m)*\partial \ln b/\partial V_G \quad (4)$$

Note that it is not necessary to stress to breakdown to extract the voltage dependence of SILC and LV-SILC, because the V_G dependence is carried solely in the trap generation pre-factor b. The voltage acceleration factors are plotted in Figure 3. A transition from bulk trap limited breakdown to interface trap limited breakdown occurs at about 2.7V, as AF(SILC) tracks AF(Q_{BD}) above 2.7V and AF(LV-SILC) tracks AF(Q_{BD}) below 2.7V. This transition coincides with the onset of multi-electron hydrogen release below the 2.5V – 3.0V threshold energy for vibrational excitation [11]. A transition from single electron to multi-electron vibrational excitation has also been observed in Q_{BD} measurements in this voltage range. [9]. Since voltage-driven breakdown arises from the processes that dissipate the energy of tunneling electrons arriving at the anode [12], the sharply differing acceleration

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factors for bulk and interface trap generation shown in Figure 3 support the two reaction model shown in Figures 1 and 2.

To compare the temperature dependence of Q_{BD} with SILC and LV-SILC, we will assume that N_{BD}, b and Q_{BD} follow an Arrhenius relationship with activation energy ΔH:

$$\Delta H(N_{BD}) = -k_B*\partial \ln N_{BD}/\partial(1/T) \quad (5)$$

$$\Delta H(b) = -k_B*\partial \ln b/\partial(1/T) \quad (6)$$

$$\Delta H(Q_{BD}) = -k_B*\partial \ln Q_{BD}/\partial(1/T) \quad (7)$$

Inserting (3), (5), (6) into (7), ΔH for SILC and LV-SILC are:

$$\Delta H(Q_{BD}, N(Q)) = (1/m)*[\Delta H(N_{BD}) - \Delta H(b)] \quad (8)$$

Unlike the V_G dependence, the temperature dependence of parameters from both trap generation (b) and breakdown (N_{BD}) must be determined. The temperature dependence of Q_{BD} for 13Å SiON films with 10^{-7} cm^2 gate area stressed at +2.2V is shown in Figure 4. The data fit an Arrhenius relationship between 75°C to 150°C, with ΔH ~ 0.65eV. The temperature dependences of the trap generation pre-factor b and the trap density at breakdown N_{BD} are shown in Figures 5 and 6 respectively. The activation energies are tabulated in Figure 7 and confirm that interface traps are the defects that control breakdown at low V_G.

We now evaluate whether AHI is the mechanism for breakdown at low V_G. A band diagram for AHI for NMOS stressed in inversion is shown in Figure 8. It can be seen that there is insufficient energy to inject holes over the barrier. However, this by itself does not rule out AHI because inelastic scattering might result in a high energy tail. Figure 9 shows the change in capacitance after stress. Two trap peaks are evident. Since the sum of the charge $Q_1 + Q_2 \approx 1.2*Q\Delta_{VT}$, the traps are predominantly acceptor states [10]. Because holes create only donor states [13,14], AHI is ruled out as the primary mechanism for interface trap generation. Therefore, since we have shown that interface traps control breakdown, AHI is ruled out as the mechanism for low voltage breakdown. Accordingly, at low V_G, the mechanism for breakdown and the explanation for the TDDB power law [5] is anode hydrogen release. Below about 2.7V, H^+ desorption no longer controls breakdown, as the release of this species is the mechanism for bulk trap generation. Therefore, below 2.7V, breakdown is controlled by electron induced desorption of H^0 and the correct anode reaction sequence is that in Fig. 1b. The reduced role of H^+ release relative to H^0 may be due to the higher bias and current required for hole induced desorption of H^+ for multi-carrier vibrational excitation [15].

We will now explore the roles of bulk and interface traps on the formation of SBD percolation paths in SiON dielectrics. Weibull slopes (β) for PNO films with EOT from 10Å to 32Å are shown in Figure 10. The t_{OX} dependence weakens below about 22Å but is still apparent. The t_{OX} dependence of β in SiON films is not unique, because both the physical thickness and nitrogen profiles are modified to scale EOT. The sub 20Å portion of the curve is enlarged in Figure 11. If β were to become thickness independent, this would open up the possibility that only 1 trap is needed to cause breakdown [16,17]. The Weibull slope (Figure 11) remains ≥ 1.1 and continues to scale with thickness down to 10Å. Accordingly, at least 2 traps are needed to form a percolation path. While LV-SILC senses interface states, it does not distinguish at which interface (or both interfaces) the traps are located. In Figure 12a, we use the cell based approach [18] to schematically illustrate a percolation path formed by 2 interface traps at the maximum oxide thickness (arbitrarily, $5a_o$) that this can occur. Figure 12b shows the possible percolation paths involving only interface traps with $t_{OX} = 4a_o$. However, a model involving only interface traps does not predict the observed t_{OX} scaling trend of the Weibull slope, since the number of traps in the percolation path is always two. Therefore, at least one bulk trap must be involved to capture the correct thickness scaling trend. A possible scenario incorporating bulk and interface traps in the percolation path and exhibiting the correct t_{OX} scalability of the Weibull slope is shown in Figure 13.

In the cell based approach, a simple relationship $\beta = mt_{OX}/a_o$ arises [18], where m is the trap generation power law exponent in (2) and a_o is the defect size. a_o is determined from the slope of β vs. t_{OX}. Since $\beta \neq 0$ at $t_{OX} = 0$, the existence of an interfacial layer that offsets the oxide thickness has been proposed [18]. Since a mixture of interface and bulk traps are required for breakdown, a single defect size will not be extracted from the slope. Instead, we find the instantaneous value of a_o for each β. When plotted against t_{OX}, a_o asymptotically approaches its bulk value as t_{OX} increases, as shown in Figure 14. It is not necessary to account for an interfacial layer to find the asymptotic value of a_o. Similarly, the result will be the same whether the x-axis of Figure 14 is physical or electrical oxide thickness. Using m = 0.26 [10], the diameter of SiON bulk traps is about 4Å.

Summary

Breakdown transitions from being bulk trap controlled to interface trap limited below 2.7V. Anode hole injection is ruled out as the breakdown mechanism at low V_G and the explanation for the TDDB power law is confirmed to be anode hydrogen release. The mechanism for breakdown transitions from hole induced H^+ desorption to electron induced H^0 release below 2.7V. While the generation of interface states becomes the rate limiting step, both bulk and interface traps are required for breakdown to occur. The bulk trap diameter is 4Å, resulting in the Weibull slope remaining t_{OX} dependent and > 1 down to 10Å EOT.

Acknowledgements

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Nominal Anode Interface Reactions – (a) Hydrogen desorption by holes only	
$(Si\text{-}H)^c + h^+ \leftrightarrow Si^0 + H^+$	(1)
$(Si\text{-}H)^d + h^+ \leftrightarrow Si^+ + H^0$	(2a)
$H^0 + H^+ \leftrightarrow H_2^+$	(3)
$(Si\text{-}H)^c + (Si\text{-}H)^d + 2h^+ \leftrightarrow Si^+ + Si^0 + H_2^+$	(4a)

Nominal Anode Interface Reactions – (b) Hydrogen desorption by holes and electrons	
$(Si\text{-}H)^c + h^+ \leftrightarrow Si^0 + H^+$	(1)
$(Si\text{-}H)^f + e^- \leftrightarrow Si^- + H^0$	(2b)
$H^0 + H^+ \leftrightarrow H_2^+$	(3)
$(Si\text{-}H)^c + (Si\text{-}H)^f + h^+ + e^- \leftrightarrow Si^- + Si^0 + H_2^+$	(4b)

Figure 1. Models for nominal anode reactions: (a) Only hole desorption mechanisms operative. (b) Both electron and hole desorption operative. (4a) or (4b) is the effective reaction. $(Si\text{-}H)^c$, $(Si\text{-}H)^d$, and $Si\text{-}H)^f$ are precursors. After [10].

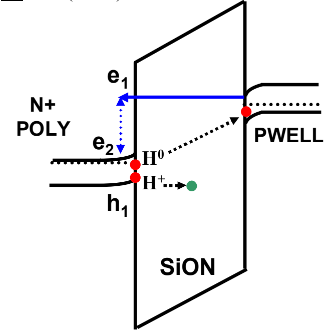

Figure 2. Band diagram for trap generation. e_1 tunnels into the anode, impact ionizes, and creates e_2 and h_1. H^+ and H^0 are subsequently desorbed. H^+ generates bulk and poly-SiON interface traps. H^0 generates traps at both interfaces. After [10].

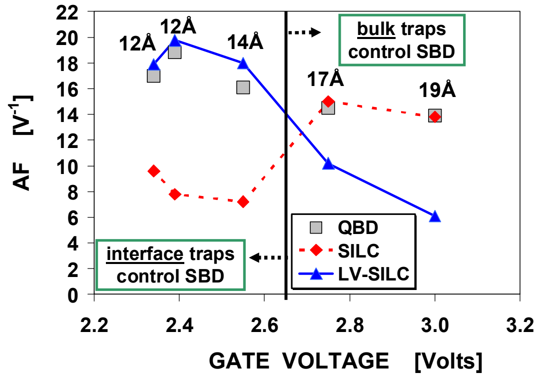

Figure 3. AF for Q_{BD}, SILC, and LV-SILC. A transition between bulk and interface trap controlled breakdown occurs at 2.7V.

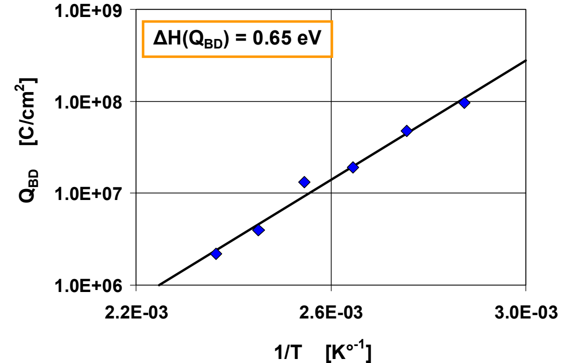

Figure 4. Arrhenius plot for Q_{BD}. 13Å films with 10^{-7} cm^2 gate area are stressed at +2.2V from 75°C to 150°C.

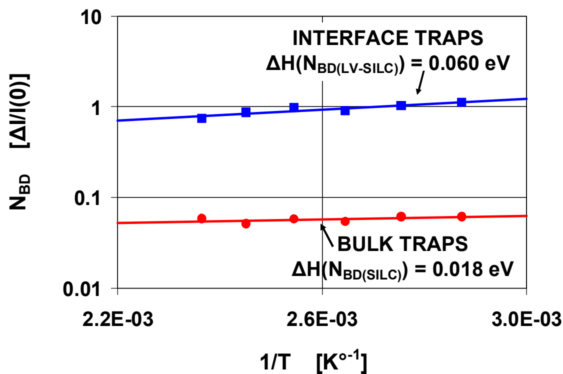

Figure 5. Arrhenius plot for the trap generation pre-factor b for the same devices used in Figure 4.

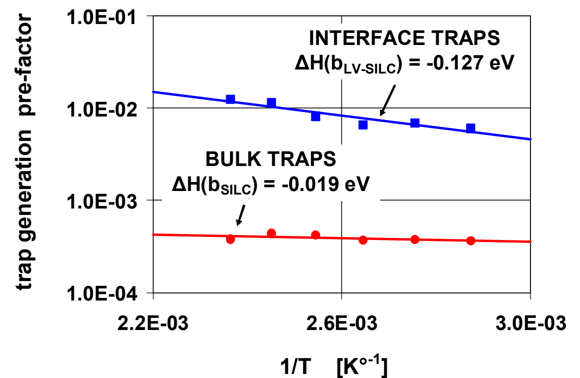

Figure 6. Arrhenius plot for the trap density at breakdown N_{BD} for the same devices used in Figure 4.

ΔH directly from Q_{BD}	ΔH from SILC	ΔH from LV-SILC
0.65 eV	0.12 eV	0.66 eV

Figure 7. ΔH for Q_{BD} and trap generation using equations (5) – (8) and Figures 4 – 6. The temperature data verify that interface traps control breakdown.

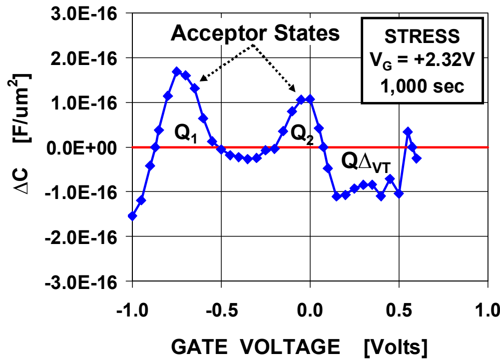

Figure 9. Change in capacitance after +2.3V stress of 12Å PNO films. The 2 peaks are predominantly acceptor states. After [10].

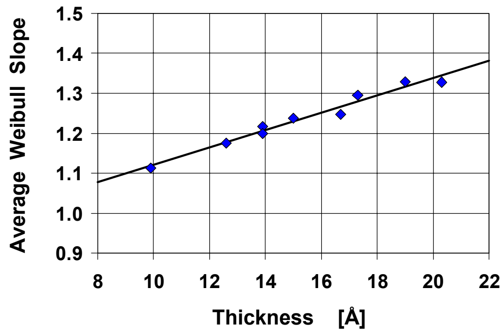

Figure 11. Enlarged view of the TDDB Weibull slope in Figure 12 for $t_{OX} < 20$Å.

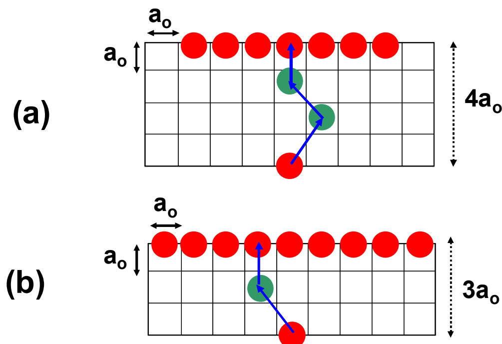

Figure 13. Schematic for percolation involving both interface and bulk traps for (a) $t_{OX} = 4a_o$. (b) $t_{OX} = 3a_o$. This model is consistent with V_G dependence (Fig. 3), temperature dependence (Fig. 7), and t_{OX} dependence (Fig. 11).

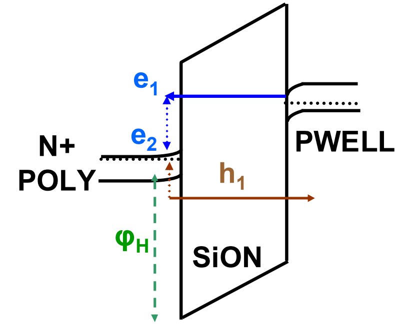

Figure 8. Band diagram at low V_G for majority ionization in depleted NMOS poly with the device stressed in inversion.

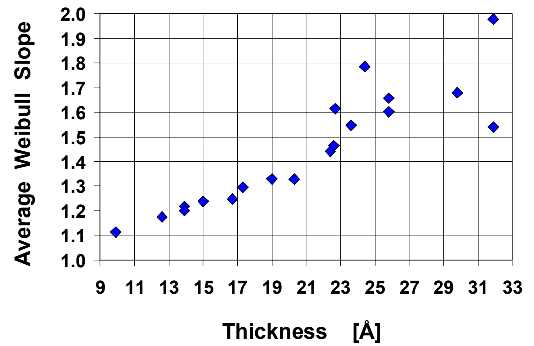

Figure 10. TDDB Weibull slope vs. thickness.

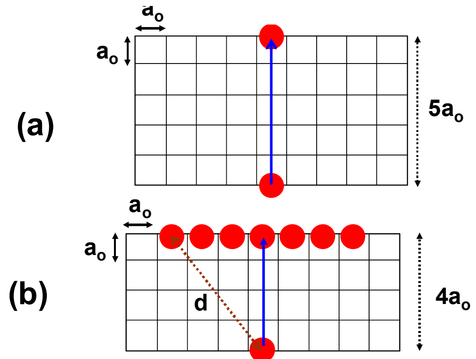

Figure 12. Schematic for 2-trap percolation involving only interface traps for (a) $t_{OX} = 5a_o$. (b) $t_{OX} = 4a_o$ with $d = 5a_o$. This model does **NOT** explain the t_{OX} scaling of β in Fig. 11.

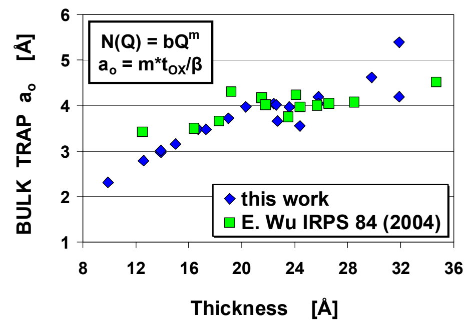

Figure 14. Bulk trap diameter vs. t_{OX} using the cell based approach. For m = 0.26 [10], the asymptotic value of a_o at large thickness is about 4Å.