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A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator

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A Brief Roadmap

- Motivation for Low-Power SC Σ-Δ Modulators
- Review of Basic Σ-Δ Modulators
- Proposed Topology
- Integrated Circuit Design
- Test Results

Motivation for This Work

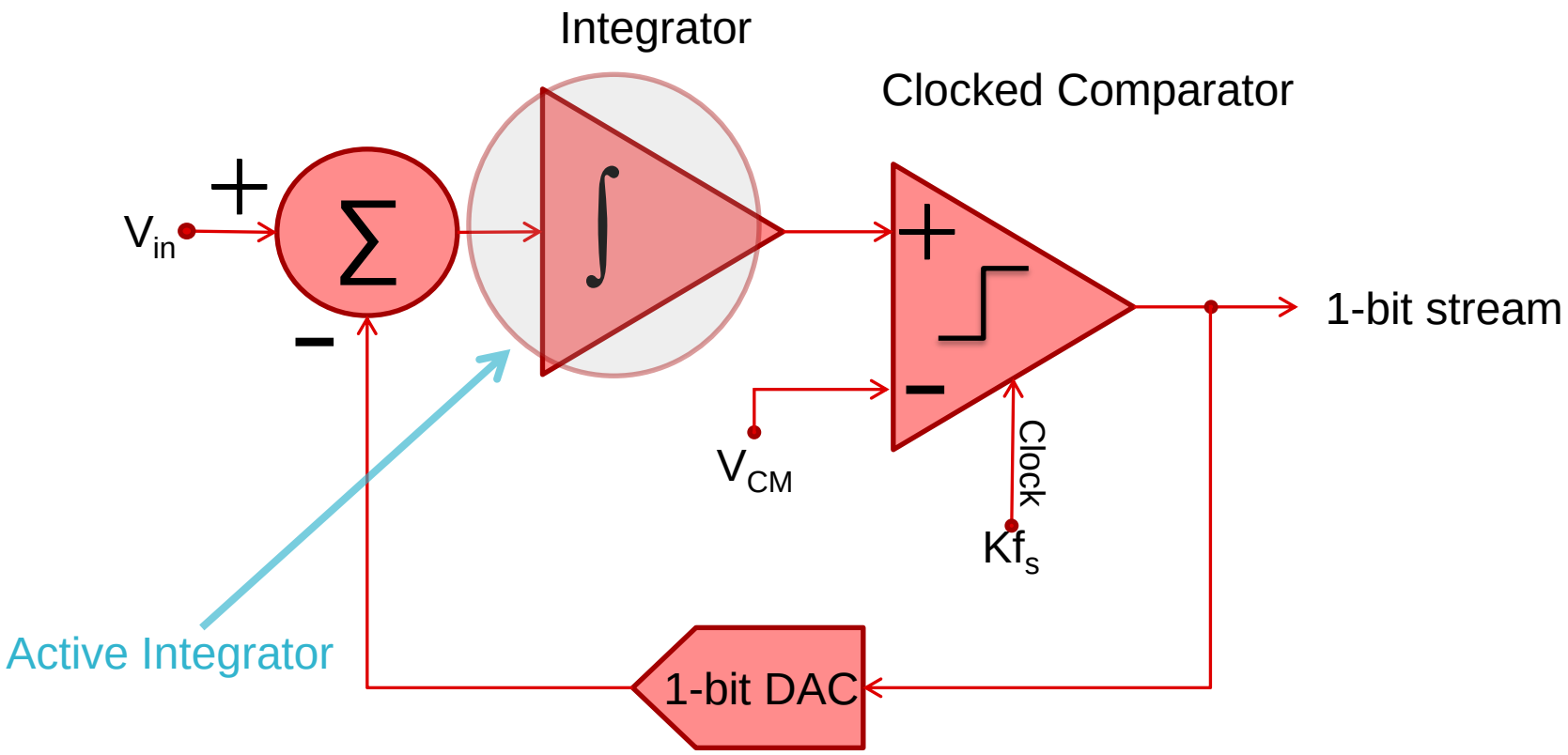
Market Need for Low Power ∑-Δ ADCs

- IoT and Mobile Devices
- ∑-Δ ADCs on the Newest Processes May Need to be Passive

Support for Older CMOS Processes

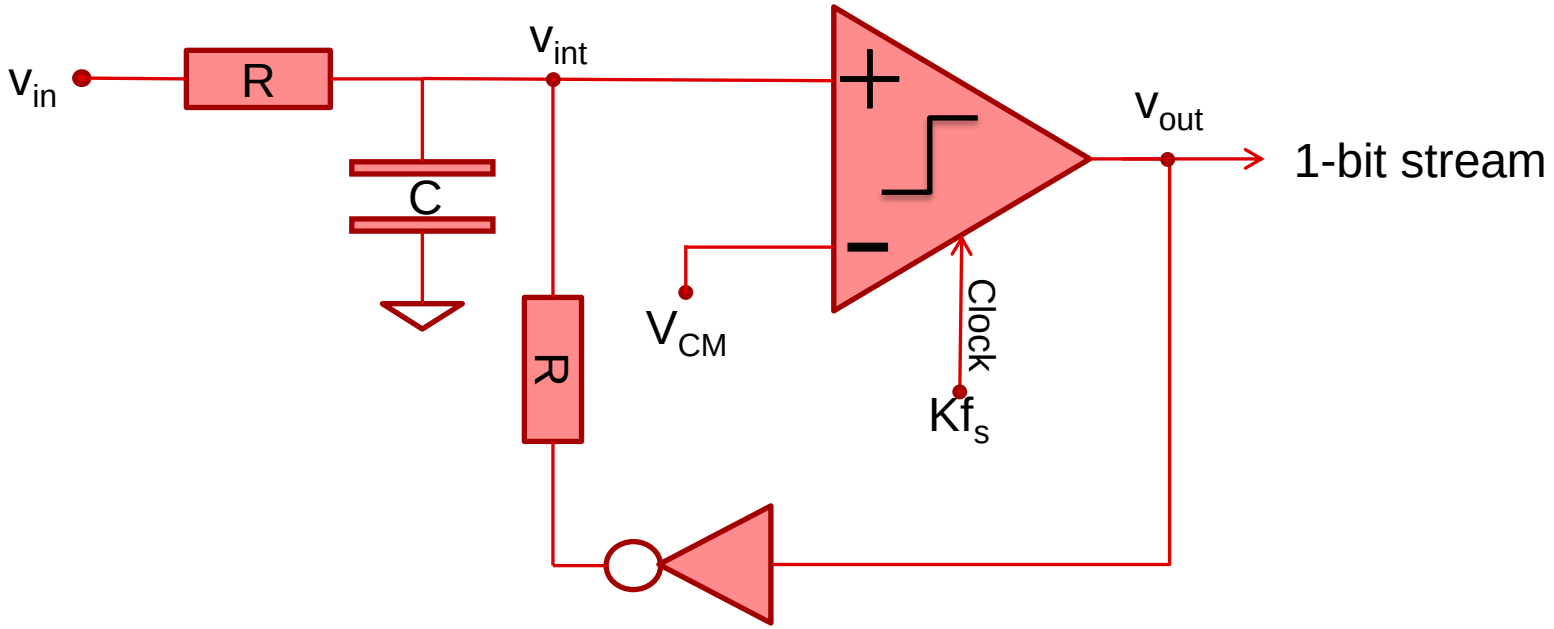
- This ∑-Δ Modulator is Implemented in 500 nm CMOS
- Still Room for Improvement in Older Processes
- Older Processes are Popular for Medical and Automotive Applications

Review of Basic Σ-Δ Modulators



Generally, ∑-Δ modulators use an active integrator to keep the voltage swing on the integrator's input to a minimum (ideally zero).

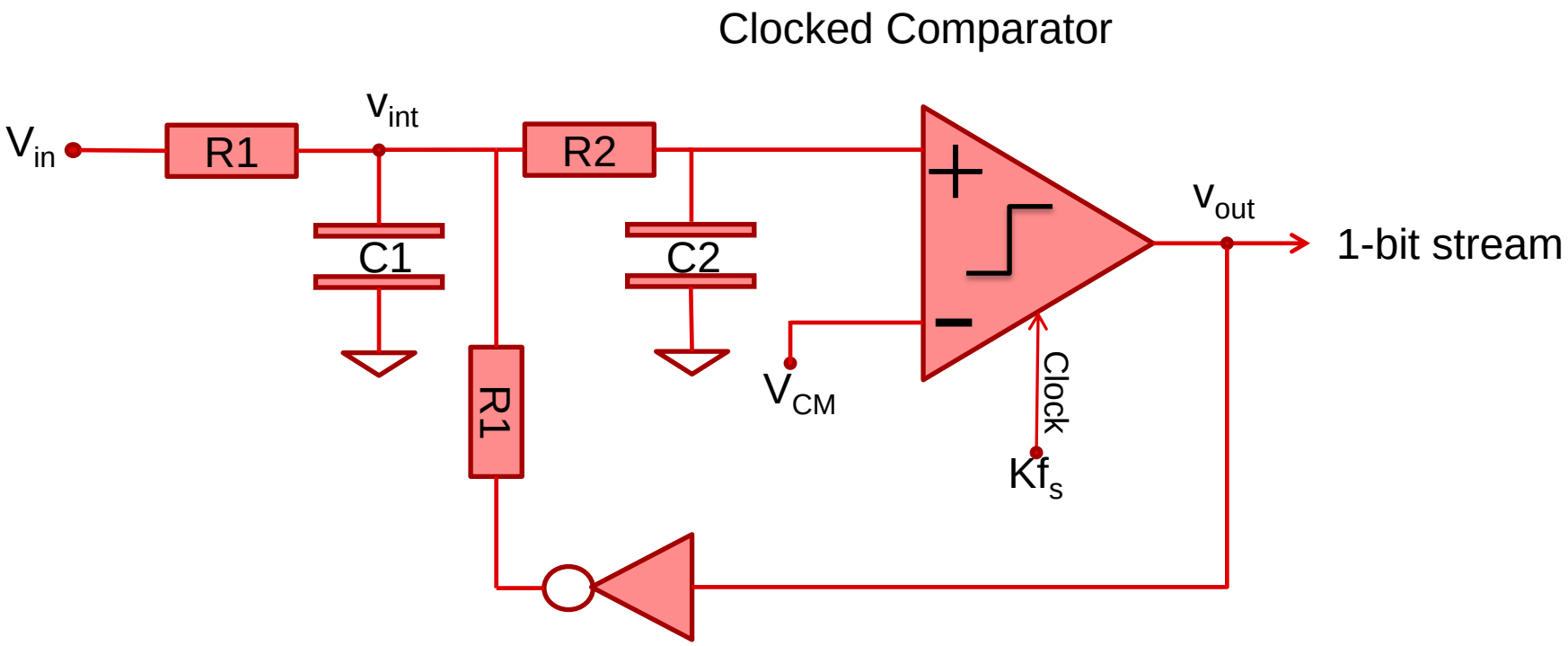
Simplest 1st Order Σ-Δ Modulator



STF NTF DT (distortion term)

$$v_{out} = \overbrace{\frac{1}{1+sRC}}^{\text{STF}} \cdot v_{in} + \overbrace{\frac{sRC}{1+sRC}}^{\text{NTF}} \cdot V_{Qe} + \overbrace{\frac{-2}{1+sRC}}^{\text{DT}} \cdot v_{int}$$

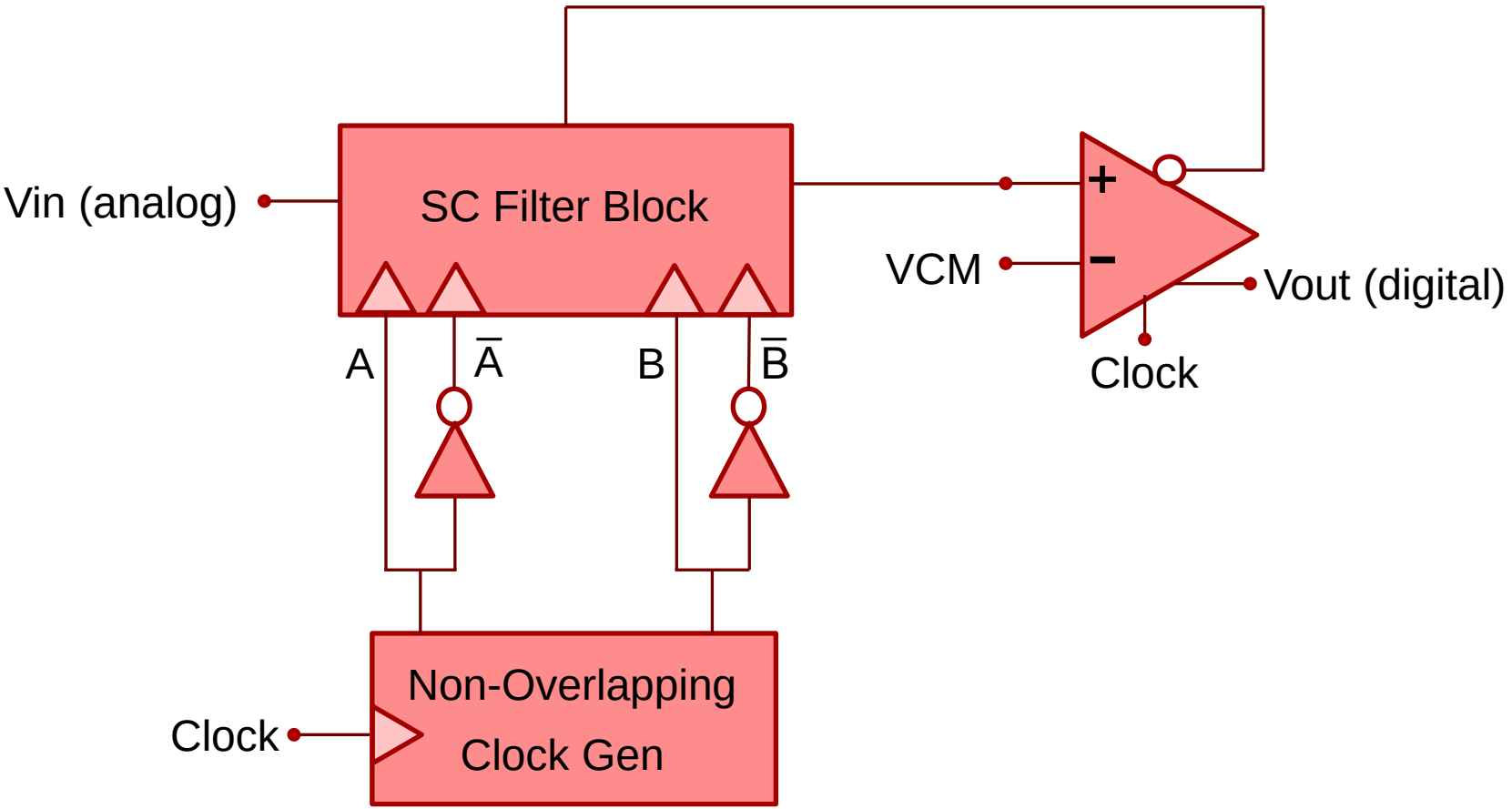
Proposed 2nd Order Σ-Δ Topology



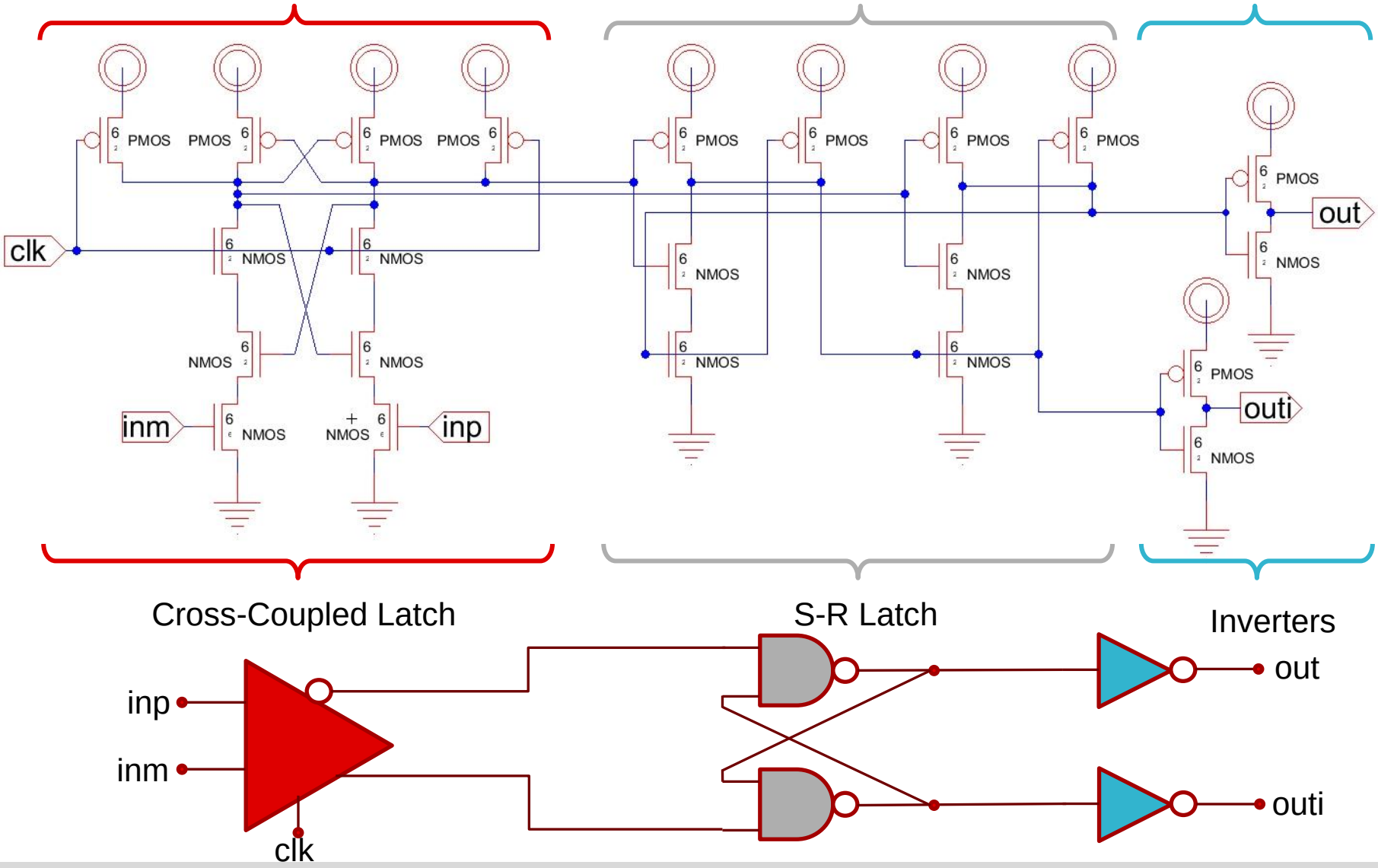
STF NTF DT (distortion term)

$$v_{out} = \frac{1 + sR_2C_2}{1 + sR_2C_2 + sR_1C_1} \cdot v_{in} + \frac{s(sR_1C_1R_2C_2 + R_1C_1)}{1 + sR_1C_1 + s^2R_1C_1R_2C_2} \cdot V_{Qe} + \frac{1}{1 + sR_1C_1 + (1 + sR_2C_2)} \cdot v_{int}$$

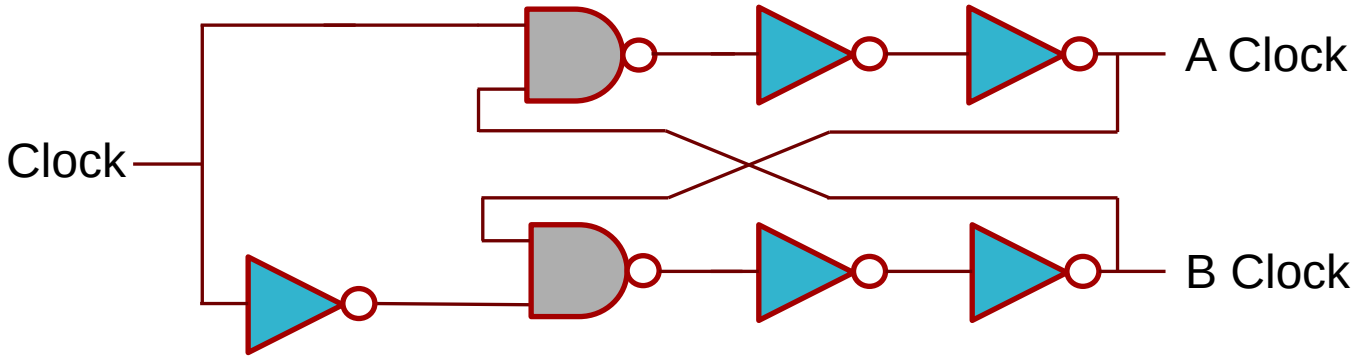
Integrated Circuit Implementation Block Diagram

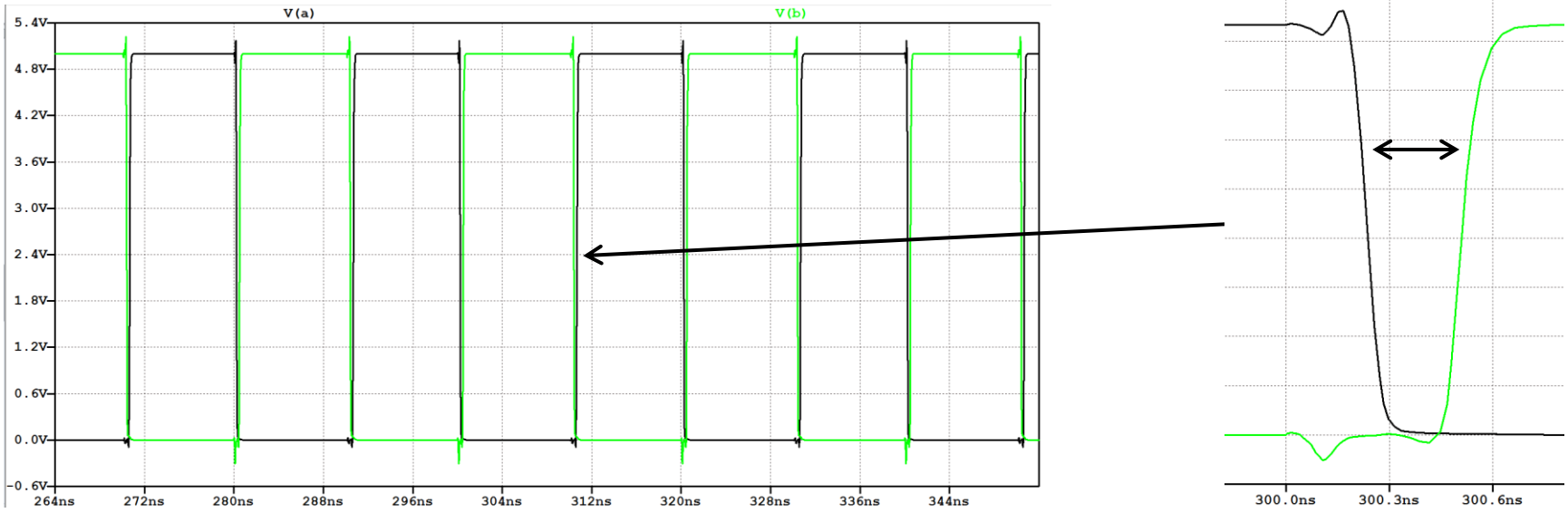


Low Power Comparator Design

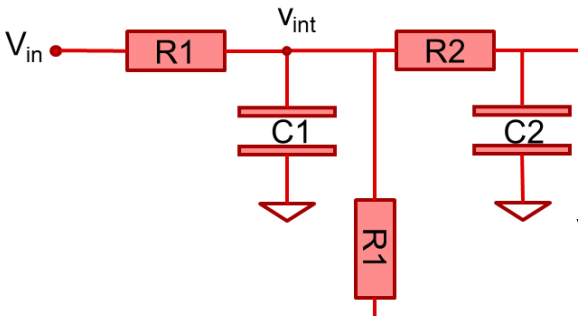


Design of Non-Overlapping Clock Generator

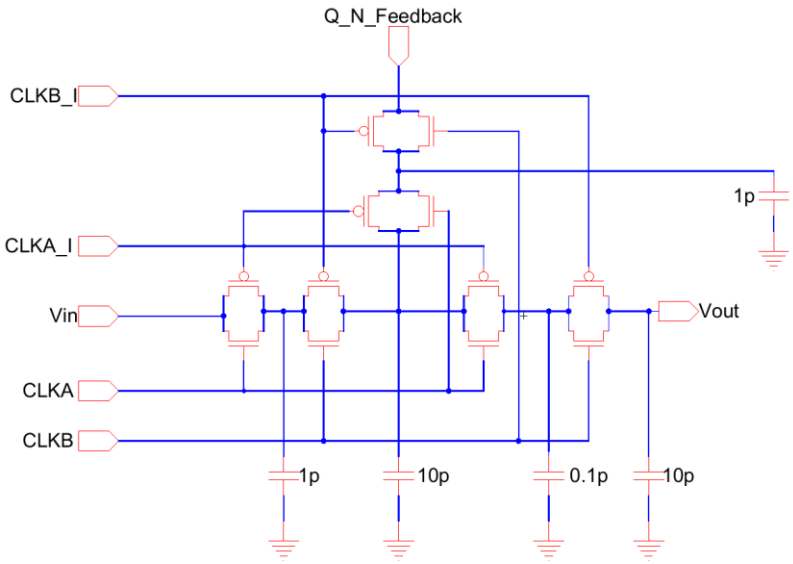




Switched Capacitor Filter



CT to SC



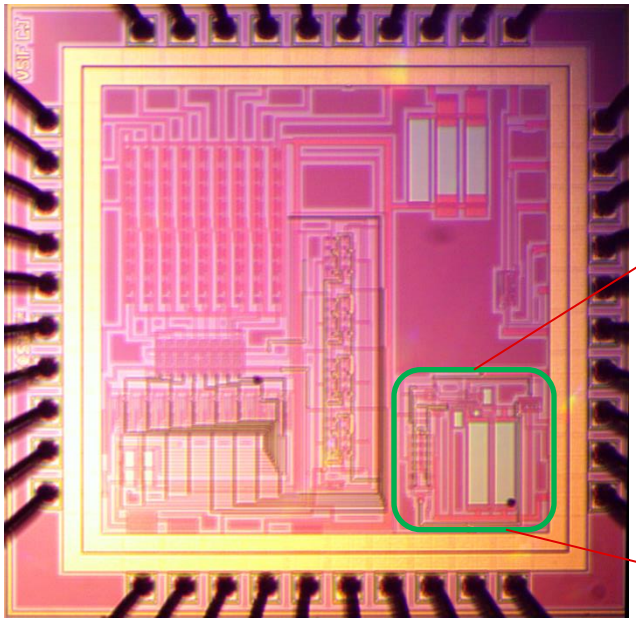
Transmission Gates Used as Switches

- NMOS and PMOS Devices are Minimum Size
- $^{W}/_{L} = {}^{1.8u}/_{0.6u}$

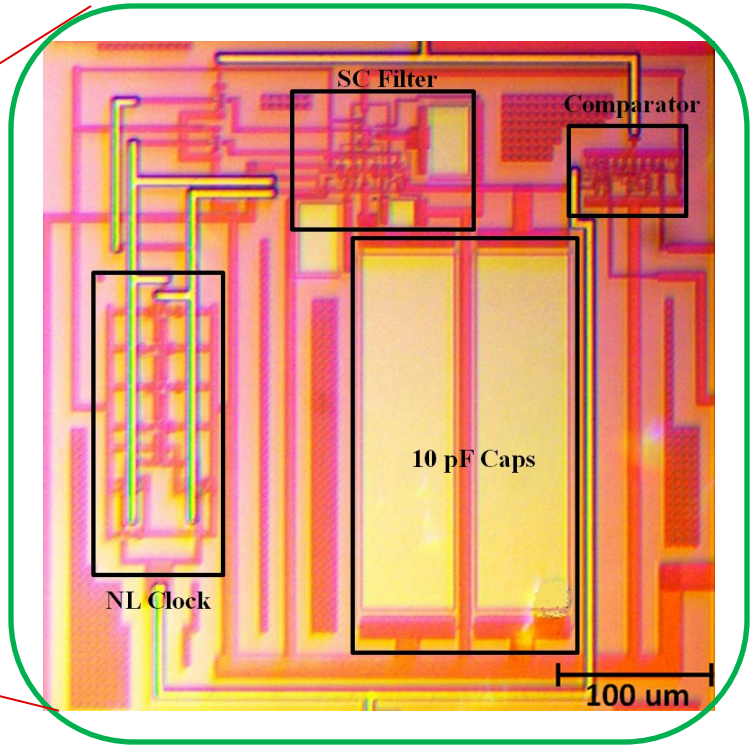
Design is Parasitic Sensitive

- Slight Gain Error Introduced
- Trade Off for Lower Power

Fabricated Chip in 500 nm C5 Process



Complete Chip with
Multiple Test Structures

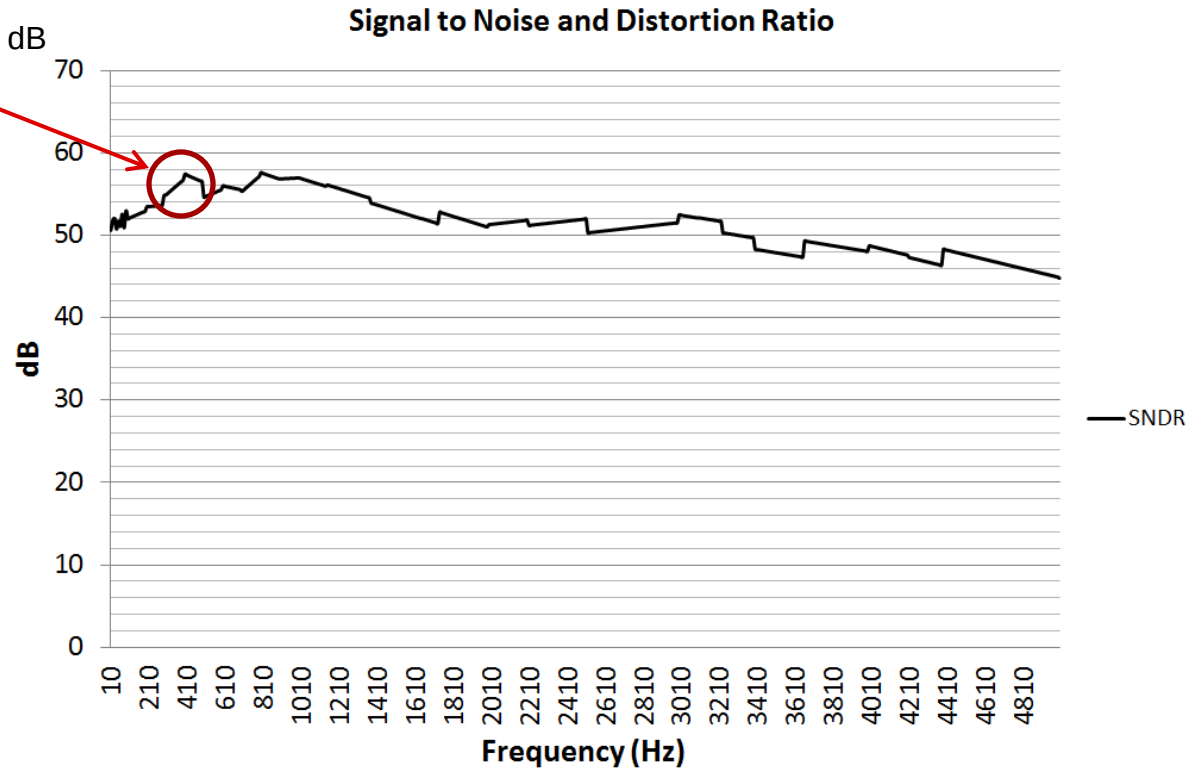


Proposed Σ-Δ Modulator

Chips were Fabricated with the MOSIS Service

Test Results

Peak SNDR of 57.6 dB



6.75 uW
2.5V VDD
2.7 uA
@ 1 MHz Clock

Test Conditions

- Digital output was filtered using a 2nd order passive RC filter.
- For each test point filter bandwidth was set to 6X input frequency.
- Clock frequency was adjusted to maintain the same OSR.

Comparison to Other Works

Parameter	Proposed 2nd-Order SC ∑-Δ Modulator (this work)	2nd-Order SC ∑-Δ Modulator in [4]	3rd-Order SC ∑-Δ Modulator in [5]
Process	500 nm	90 nm	130 nm
Resolution (ENOB)	9.3 bits	10.48 bits	12.3 bits
Signal Bandwidth	3 KHz	10 KHz	20 KHz
Clock Frequency	1.024 MHz	1.28 MHz	3.2 MHz
Power Consumption	6.75 µW @ 2.5 V	17.14 µW @ 1 V	63 µW @ 0.4 V
FOM	1.78 pJ/step	0.60 pJ/step	0.31 pJ/step

[4] Hsu, C. H., Tang, K. T., "A 1V Low Power Second-Order Delta-Sigma Modulator for Biomedical Signal Application," *Engineering in Medicine and Biology Society (EMBC), 2013 35th Annual International Conference of the IEEE, pp.2008-2011,*, July 2013

[5] Yoon, Y., Choi, D., Roh, J., " A 0.4-V 63-µW 76.1-dB SNDR 20-kHz Bandwidth Delta-Sigma Modulator Using a Hybrid Switching Integrator," *IEEE Journal of Solid-State Circuits, vol. no.99, pp.1-12*