The Roles of Hydrogen and Holes in Trap Generation and Breakdown in Ultra-thin SiON Dielectrics

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Abstract

We show for the 1ST time that trap generation and breakdown in ultra thin SiON gate dielectrics are triggered by the release of **two** hydrogen species (H^+ and H^0) from the anode during TDDB stress.

Introduction

Technology scaling necessitates ongoing advancements in the understanding of dielectric breakdown to meet state-of-the-art reliability requirements. In particular, additional insight is needed to support implementation of the aggressive power law model for TDDB, where $t_{BD} = aV_G^{-N}$ [1]. Trap generation and breakdown result from the processes that thermalize electrons that tunnel into the anode. Proposed mechanisms include injection of anode hot holes over the barrier (AHI) [2] or the release of hydrogen (AHR) [3] into the dielectric. There is considerable experimental support for both AHI and AHR models and it is plausible that both holes and hydrogen are involved in trap generation and breakdown [4].

Reliability models for the NMOS on-state are of particular interest because in an inverter, the entire gate oxide area is stressed. However, at very low stress voltages, while impact ionization in the anode may occur, there is insufficient energy for AHI in NMOS devices with $+V_G$ applied because only majority ionization [2] is operative in the poly space charge region. Accordingly, hydrogen is expected to play a central role in breakdown at low voltages, and it has been proposed that the TDDB power law arises from anode hydrogen release [5]. However, neither the reaction leading to AHR nor the hydrogen species released from the anode have been fully elucidated. One reason for this is that in NMOS stressed at $+V_G$, it is difficult to characterize the poly-SiON anode interface where the degradation process initiates. In this work, we initiate the reaction at the readily characterized Si-SiON interface by stressing NMOS devices in inversion with a back-bias applied to induce the desorption of cathode hydrogen by substrate hot electrons (Figure 1). No n+ injector is used to avoid both uncontrolled flooding of the dielectric with the cathode species and high level injection of hot electrons into the anode. We will show that reaction-diffusion theory [6] applies to NMOS trap generation and use the cathode hydrogen species released to probe the anode reaction mechanisms. We analyze the trap generation kinetics resulting from the interaction of the cathode hydrogen with the hydrogen species released from the anode to deduce the nominal degradation processes.

Experiment

1.2nm EOT PNO films from a 90nm full-flow CMOS process [7] are stressed with V_G from +2.3V to +2.4V and V_{BB} from 0V to -6V. Time-0 I-V characteristics are shown in Figure 2. The devices remain in strong inversion at stress and the increase in I_B from band-to-band tunneling is < 2μA (20A/cm^2) below 6V $|V_{BB}|$. As the maximum kinetic energy of electrons at the cathode (prior to inelastic scattering) is $E_{CATH}(max) \approx qV_{BB} + 2q\varphi_S(inv)|_{Vbb=0V} - q\varphi_S(inv)|_{Vbb}$, the hydrogen desorption energy of ~ 5eV [3] is attained. Interface traps are monitored by LV-SILC [8], C-V, ΔV_T, and ΔI_{DLIN}. Bulk traps are sensed by SILC [9]. C-V sweeps are at 25°C on 1x10^{-6} cm^2 gate areas; all other measurements are at 105°C on 1x10^{-7} cm^2 gate areas. t_{BD} is determined from the noise variance [10]. Statistics are based on 45 devices per stress condition.

Results

Stress induces a single LV-SILC peak near VFB in SiO_2 due to interface traps [8]. Two LV-SILC peaks appear in SiON after PMOS NBTI [11] and are also observed for NMOS SiON under $+V_G$ stress (Figures 3, 4). V_{BB} increases the generation of both states but is more pronounced for the peak at -1V sense. Forward and reverse C-V sweeps for -6V V_{BB} (Figure 5) show little hysteresis or VFB shift, indicating insignificant charge trapping. The two trap peaks are also seen in the C-V sweeps. The area under the ΔC vs. V_G curve in Figure 6 equals charge. As the sum of the charge $Q_1 + Q_2 \approx Q_{\Delta VT}$, both states are acceptor-like (negatively charged or neutral). Because hole cracking of Si-H bonds creates only donor traps [12], AHI is not the probable mechanism for cathode interface trap generation.

Trap generation follows a power law in fluence, $N(Q) = bQ^m$ [9]. Reaction-diffusion theory relates the hydrogen species released to the trap generation power law exponent "m" when the system is in quasi-equilibrium, where the net trap creation rate is small because both forward reaction (trap generation) and reverse reaction (recovery) are operative [6]. If measurable recovery effects are present, a delay time between stress and sense will result in a larger trap generation power law exponent [13]. The trap generation power law exponent "m" resultant from the hydrogen species released

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(compiled in [14]) is shown in Figure 7. We only consider the dissociation of Si-H bonds because N-H bond breaking in PNO has not been observed by ESR [15].

Figure 8 shows that the interface trap generation "m" increases slightly with V_{BB} from 0.33 to 0.38. Our model for the reaction steps for V_{BB} = -6V that give rise to acceptor interface traps with m ~ 1/3 is shown in Figure 9. The reactants $(Si\text{-}H)^a$ and $(Si\text{-}H)^b$ represent precursors that could have the same or different local atomic environments. The 1/3 power law is driven by the desorption of H^- and H^0 from Si-H bonds by cathode hot electrons, with H^- and H^0 possibly combining to form H_2^-. Note that the steps leading to the final product H_2^- in Figure 9 are an "effective" reaction, as our simulations (not shown) indicate that the 1/3 power law can arise from either H_2^- or equal amounts of H^- and H^0. "m" slightly larger than 1/3 may be due to a slightly higher desorption rate for H^- over H^0. The existence of one form of charged H_2 in SiO_2 (H_2^+) has been proposed [16].

In Figure 10, bulk trap "m" increases from 0.26 (0V V_{BB}) to 0.51 (-6V V_{BB}), indicating a change in the reaction that creates bulk traps. The bulk trap generation pre-factor "b" (the y-intercepts in Figure 10) is lower at -6V V_{BB}, indicating that the -6V V_{BB} cathodic species (H^-) suppresses nominal 0V V_{BB} bulk trap generation through a reaction that depletes the anodic species. Accordingly, nominal bulk trap creation is due to the release of a positively charged anode species.

Quasi-equilibrium is confirmed by the effect of interrupted stress (5 second delay between stress and sense) in Figures 11-14. The differences in "m" are due to the reverse reaction, which is slow for 0V V_{BB} but pronounced for -6V V_{BB}. Hole de-trapping, which increases with oxide field [17], is not the cause for the larger "m" for interrupted stress since the field is periodically shut-off. Power law parameters are shown for all V_{BB} in Figure 15. Note the sharp changes near the 5eV hydrogen desorption energy. The TDDB Weibull slope also increases with $|V_{BB}|$ (Figure 16), showing that our trap generation power laws are tracking the traps that cause breakdown. While breakdown is "softer" with back bias due to lower inversion charge [18], we are still able to accurately detect the 1^{ST} breakdown event at -6V V_{BB}, as our noise variance trigger (Figure 17) captures gate current jumps < $8x10^{-7}$ Amps (empirically shown to be a reliable indicator of SBD) [19] as seen in Figure 18. The V_{BB} dependence of the Weibull slope (which is a geometric quantity) rules out transmission of substrate hot electrons (dashed horizontal arrow in Figure 1b) into the anode as the primary contribution for the higher trap generation rates. Figure 16 implies that the traps that cause breakdown at -6V V_{BB} may not be the same traps that cause breakdown at 0V V_{BB}.

Our model for the nominal (0V V_{BB}) anode interface reactions is presented in Figure 19. The reactants $(SiH)^c$, $(Si\text{-}H)^d$, and $(Si\text{-}H)^f$ in Figure 19 represent precursors that could have the same or different local atomic environments. Desorption of these precursors creates interface traps at the anode. Bulk traps are generated in the dielectric by H^+ or H_2^+ following the desorption of Si-H bonds by anode hot holes. The hot holes originate through impact ionization of electrons tunneling into the anode. An anodic reaction releasing H^0 is also needed to account for nominal (V_{BB} = 0V) cathodic acceptor interface trap creation, because only neutral or positive charged species can be released from the anode into the dielectric and H^+ is not highly reactive at device grade $Si\text{-}SiO_2$ interfaces [16]. Moreover, a positive species creates donor traps, but acceptor states are still the dominant traps at the cathode for 0V V_{BB} stress (Figure 20). Indeed, the large differences in the V_G dependence (see equations in Figure 21) between SILC and LV-SILC in Figure 22 indicate that bulk and interface trap generation are not triggered by the same anode reaction. Our experiments cannot differentiate whether anodic H^0 is desorbed by holes (Figure 19a) or electrons (Figure 19b). Although H^0 might be liberated from bulk trap creation (m ~ 0.25; see Figure 7), this would not be the sole source of H^0 since the generation rate is higher for interface traps than bulk traps (Figure 23).

Summary

We have shown that reaction-diffusion theory applies for $+V_G$ TDDB stress of ultra-thin NMOS SiON films. Trap generation has measurable recovery effects, showing that quasi-equilibrium exists for NMOS TDDB under substrate injection conditions. At low voltages, holes are involved in the desorption of anode hydrogen during TDDB stress and create interface traps at the anode interface. Two different hydrogen species, H^+ and H^0, are released from the anode and generate bulk and cathode interface traps respectively. Only acceptor-like interface traps are created at the cathode interface. These findings provide a framework for further advancements in the physics behind the TDDB power law.

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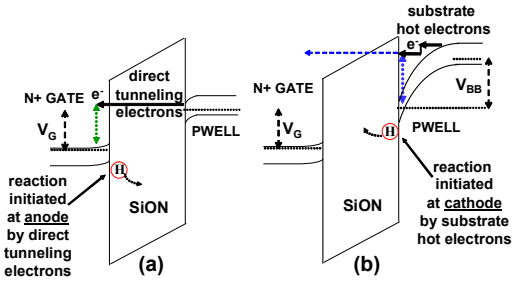

Figure 1. Band diagram for stress. Reaction initiated: (a) At anode, drawn at 0V V_{BB}; (b) At cathode, $|V_{BB}| > 0V$. Dashed horizontal arrow in (b) denotes transmission through the barrier.

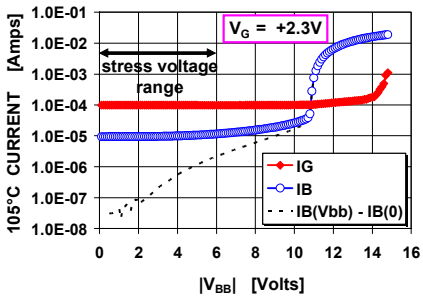

Figure 2. Time-0 gate and substrate currents vs. V_{BB}. The increase in I_B is < 2μA below 6V $|V_{BB}|$.

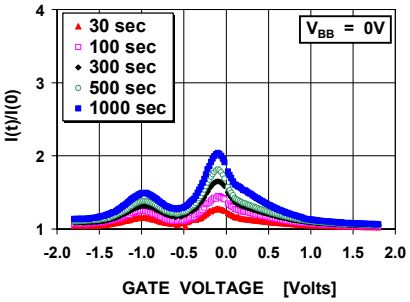

Figure 3. LV-SILC for V_G = +2.32V, V_{BB} = 0V stress. The 2 peaks are due to interface traps.

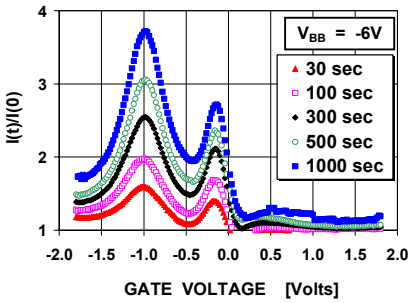

Figure 4. LV-SILC for V_G = +2.32V, V_{BB} = -6V stress. Back-bias increases interface trap generation rates.

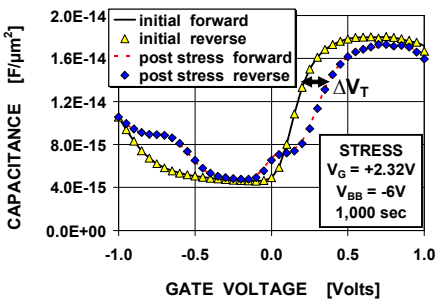

Figure 5. Pre and post stress forward and reverse C-V characteristics. The stress voltages were V_G = +2.32V, V_{BB} = -6V.

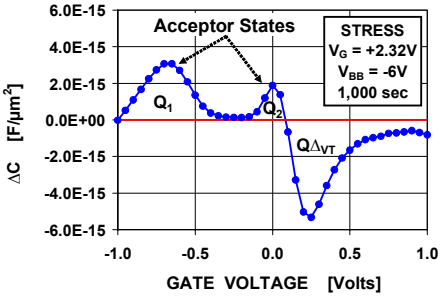

Figure 6. Change in capacitance ΔC (from data in Fig. 5) after stress at V_G = +2.32V, V_{BB} = -6V. The 2 trap peaks are acceptor states.

reaction product	m
H_2	1/6
H^0	1/4
H_2^+	1/3
H_2^-	1/3
H^+	1/2
H^-	1/2

Figure 7. Reaction-diffusion trap generation power law exponents. After ref. [14].

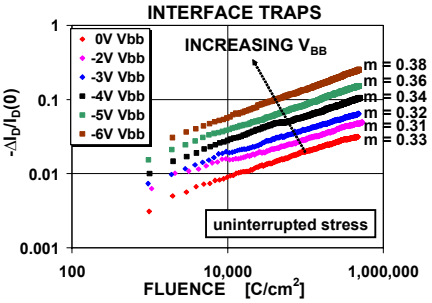

Figure 8. Interface trap generation power laws (from ΔI_{DLIN}) as a function of V_{BB}.

V_{BB} = -6V Cathode Interface Reactions
m ~ 1/3

$(Si\text{-}H)^a + e^- \leftrightarrow Si^- + H^0$ (1)

$(Si\text{-}H)^b + e^- \leftrightarrow Si^0 + H^-$ (2)

$Si^0 + e^- \leftrightarrow Si^-$ (3)

$H^0 + H^- \leftrightarrow H_2^-$ (4)

$(Si\text{-}H)^a + (Si\text{-}H)^b + 3e^- \leftrightarrow 2Si^- + H_2^-$ (5)

Figure 9. Model for cathode reactions for acceptor interface trap creation at -6V V_{BB} stress. (5) is the effective net reaction.

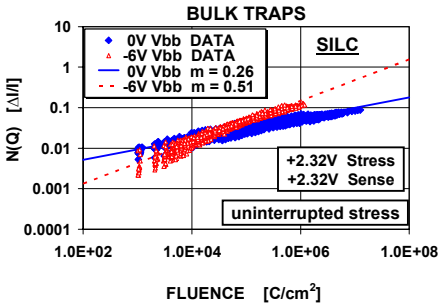

Figure 10. Bulk trap generation power laws (from SILC) for stress with V_G = +2.32V and V_{BB} = 0V or V_{BB} = -6V. The sense voltage is V_G = +2.32V. Lines are statistical fits to the data.

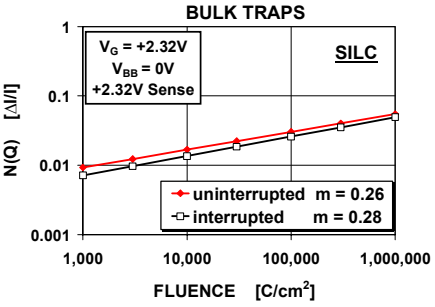

Figure 11. Statistical fits for bulk trap generation power laws from SILC (sensed at +2.32V) for interrupted vs. uninterrupted stress at V_G = +2.32V and V_{BB} = 0V. The larger "m" for interrupted stress is due to recovery effects.

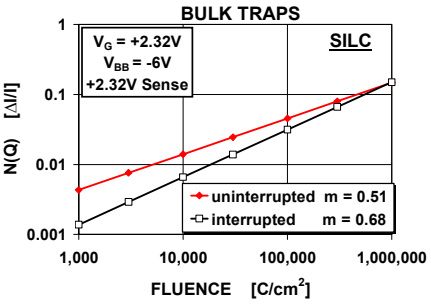

Figure 12. Statistical fits for bulk trap generation power laws from SILC (sensed at +2.32V) for interrupted vs. uninterrupted stress at V_G = +2.32V and V_{BB} = -6V. The larger "m" for interrupted stress is due to recovery effects.

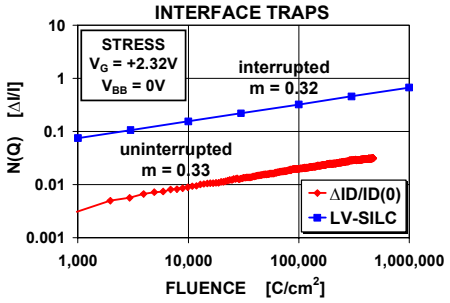

Figure 13. Interface trap generation power laws from LV-SILC (sensed at -1V) and ΔI_{DLIN} for interrupted vs. uninterrupted stress respectively. Stress was at V_G = +2.32V and V_{BB} = 0V. Interface trap recovery was NOT observed for V_{BB} = 0V.

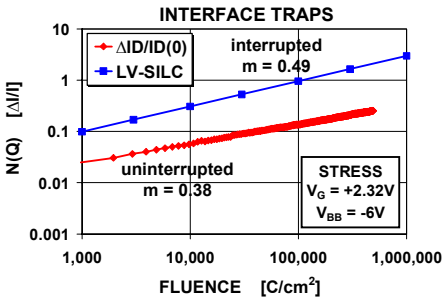

Figure 14. Interface trap generation power laws from LV-SILC (sensed at -1V) and ΔI_{DLIN} for interrupted vs. uninterrupted stress respectively. Stress was at V_G = +2.32V and V_{BB} = -6V. The larger "m" for interrupted stress is due to recovery effects.

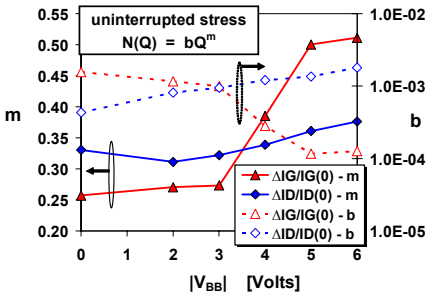

Figure 15. Power law parameters for all V_{BB} stress conditions. $\Delta I_G/I_G(0)$ and $\Delta I_D/I_D(0)$ represent bulk and interface trap generation respectively.

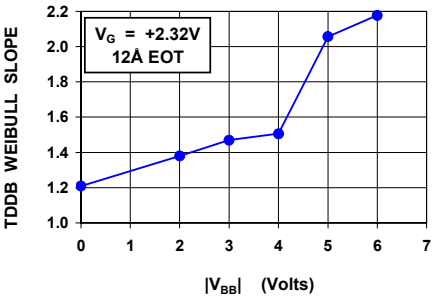

Figure 16. TDDB Weibull slope vs. $|V_{BB}|$ for 12Å EOT films stressed at +2.32V V_G.

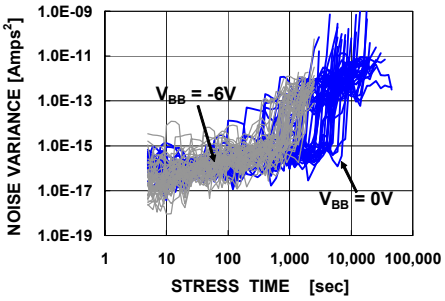

Figure 17. Noise variance during TDDB sensed at V_G = +1.0V. The stress conditions were V_G = +2.32V at 0V V_{BB} (blue) and -6V V_{BB} (gray).

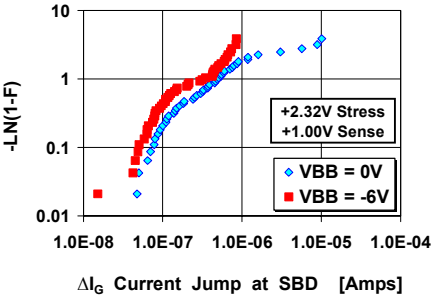

Figure 18. Current jump sensed at V_G = +1.0V corresponding to the onset of the permanent increase in noise variance shown in Fig. 17.

Nominal Anode Interface Reactions – (a)

$(Si\text{-}H)^c + h^+ \leftrightarrow Si^0 + H^+$ (6)
$(Si\text{-}H)^d + h^+ \leftrightarrow Si^+ + H^0$ (7a)
$H^0 + H^+ \leftrightarrow H_2^+$ (8)
$(Si\text{-}H)^c + (Si\text{-}H)^d + 2h^+ \leftrightarrow Si^+ + Si^0 + H_2^+$ (9a)

or:

Nominal Anode Interface Reactions – (b)

$(Si\text{-}H)^c + h^+ \leftrightarrow Si^0 + H^+$ (6)
$(Si\text{-}H)^f + e^- \leftrightarrow Si^- + H^0$ (7b)
$H^0 + H^+ \leftrightarrow H_2^+$ (8)
$(Si\text{-}H)^c + (Si\text{-}H)^f + h^+ + e^- \leftrightarrow Si^- + Si^0 + H_2^+$ (9b)

Figure 19. Models for nominal (V_{BB} = 0V) anode reactions: (a) Only hole desorption mechanisms operative. (b) Both electron and hole desorption mechanisms operative. (9a) or (9b) is the effective net reaction. Our experiments cannot resolve whether H^0 is desorbed by holes (7a) or electrons (7b) at the anode.

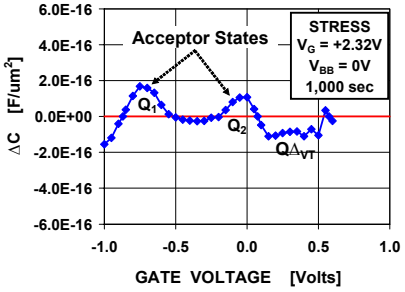

Figure 20. Change in capacitance ΔC after stress with V_{BB} = 0V. The 2 acceptor trap peaks are also seen after 0V V_{BB} stress.

N(Q)	=	bQ^m	(1)
AF	=	$-\partial \ln Q/\partial V_G$	(2)
$AF_{N(Q)}$	=	$(1/m)\partial \ln b/\partial V_G$	(3)
$\partial N(Q)/\partial Q$	=	mbQ^{m-1}	(4)

Figure 21. Equations used in Figures 22 and 23. (1) is the trap generation power law, (2) defines the voltage acceleration factor, (3) is the voltage acceleration factor for trap generation, (4) is the trap generation rate.

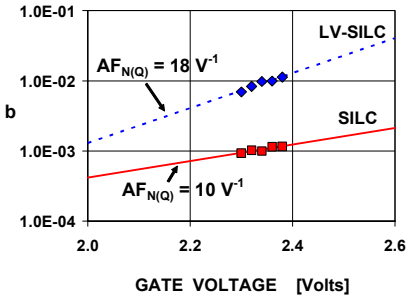

Figure 22. V_G dependence of LV-SILC (interface traps) and SILC (bulk traps). Sense voltages are -1.0V and V_{STRESS} respectively. V_{BB} = 0V during stress and sense.

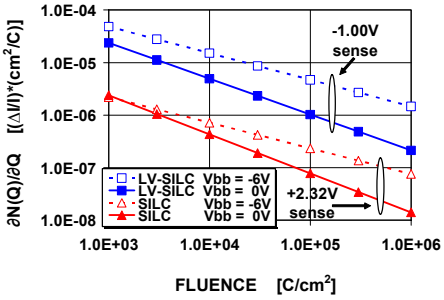

Figure 23. Comparison of bulk trap (SILC) and interface trap (LV-SILC) generation rates from statistical fits of the data. The gate voltage during stress was +2.32V.