Improved Performance of Communication Sub System of System-on-Chip

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Abstract—System on Chip (SoC) has provided many advantages, but also many design challenges. Network on Chip (NoC) has developed to solve the problems associated with communication requirements in SoC. Contribution of power dissipation of communication requirements is much greater than the remaining requirements of the SoC. As technology scales down, interconnects are becoming more power hungry in NoC. The power dissipation of interconnects is directly proportional to switching activity factor of interconnects, capacitance, operating voltage and frequency. Operating voltage, frequency and capacitances are technology dependent. Switching activity is the one, which is technology independent. Switching activity of interconnects only depends on data patterns which are travelling on interconnects. Hence, in this paper an attempt has made to reduce the switching activity of interconnect using data encoding techniques. The proposed data encoding techniques are general and transparent with respect to the underlying NoC fabric. Experiments have been carried out with 8-bit, 16-bit, 32-bit and 64-bit data sizes to study the performance of the proposed data encoding techniques. Experimental results show that the proposed data encoding techniques have provided better performance efficiency in terms of Energy, Delay and Energy-Delay-Product (EDP) with less area overhead.

Keywords— Switching activity, Data encoding, Low power, System on Chip (SoC).

I. INTRODUCTION

Recent trends in ultra-deep submicron meter era have resulted in high performance and power efficient logic blocks, but less performed and high power consuming interconnects [11]. In fact, interconnects are consuming the 50% of the total dynamic power dissipation in current technologies, and this expected to rise to 65%-80% over the next several years [21]. Global interconnect length does not scale with smaller transistors and local wires. Chip measure remains generally steady in light of the fact that the chip work keeps on expanding and RC delay increments exponentially. SoC design methodologies are providing the ability to integrate more and more cores in single silicon die, but the same ability of SoC has faced the challenge as to provide the reliable communication among the number of cores [28]. Network on Chip (NoC) is emerging as a design paradigm to address the scalability and reliability issues of SoC [4].

In recent times, the on-chip communication problems are as more relevant as, and in some instances greater relevant than, the computational associated problems [4]. In fact, the communication subsystem increasingly more influences the conventional design goals, along with cost, performance, power dissipation, energy consumption and reliability. As technology shrinks, an ever more tremendous fraction of the whole power budget of the complex many-core SoC is because of the communication subsystem.

In this paper, we focus on strategies aimed toward lowering the power dissipated with the aid of the network links. In reality, the power dissipated through the network links is as applicable as that dissipated by routers and network interfaces (NIs) and their contribution is predicted to boom as generation scales [14]. Particularly, we present a set of data encoding schemes working at flit level and on an end-

to-end basis, which permits us to limit both the self-switching activity and the coupling switching activity on interconnects of the routing paths traversed by the packets. The proposed data encoding schemes are transparent to router implementation. Moreover, data encoding techniques have assessed by using simulation on various flit sizes. The evaluation takes into consideration numerous factors and metrics of the design, including overhead area and delay of proposed data encoding techniques, efficiency in terms of switching activity, energy consumption, and delay of interconnects. The outcome shows that the proposed data encoding techniques have provided better performance.

The rest of this paper has organized as follows. We briefly discuss the related works in section II, while section III provides detailed description of the proposed data encoding schemes. In section IV, the results for the proposed data encoding schemes in all aspects and those have analyzed and compared with different techniques. Eventually, this paper has concluded in section V.

II. RELATED WORKS AND CONTRIBUTIONS

Within the subsequent several years, the provision of chips with one thousand cores is foreseen [29]. In these chips, a significant fraction of the entire system power dissipation is via interconnection networks. Consequently, the design of power-efficient interconnection networks have been the point of interest of many works published within the literature handling NoC architectures. These works give attention to the unique components of the interconnected networks inclusive of routers, NIs, and links. Due to the fact that the point of interest of this paper is on decreasing the power dissipated by means of the links, in this section, we briefly evaluating a number of the works within the vicinity of link power reduction. These encompass the strategies that employ shielding [27], [10], growing line-to-line spacing [16], [1], and repeater insertion [3]. All of them increase the chip area. The data-encoding scheme is some other approach that employed to reduce the link power dissipation. The data encoding techniques have classified into two categories. In the first category, encoding techniques give attention to reducing the power because of self-switching activity of individual bus lines, even as ignoring the power dissipation due to their coupling switching activity. In this category, bus invert (BI) [25] and INC-XOR [22] were proposed for the case that random data patterns are transmitted through these lines. On the other hand, gray code [26], T0 [5], working-zone encoding [17], and T0-XOR [9] have advised in the case of correlated data patterns. Application-specific techniques have additionally been proposed in [6], [7], [2], [24], [31].

This category of encoding is not always appropriate to be carried out within the deep sub-micron meter technology nodes where the coupling capacitance constitutes a main part of the entire interconnect capacitance. Due to this reason, the power consumption because of the coupling switching activity to come to be a massive fraction of the overall link power consumption, making the fore mentioned strategies, which ignore such contributions, inefficient [19]. The works within the second category concentrate on decreasing power dissipation via the reduction of the coupling switching [1], [31], [19], [15], [20], [13], [23], [12], [30], [8]. Among those schemes [1], [15], [20], [13], [23], [12], the switching activity has decreased the use of many extra control lines. As an instance, the data bus width grows from 32 to 55 in [15]. The strategies proposed in [30] and [8] have a smaller quantity of control lines, however the complexity in their decoding logic is excessive. The approach defined in [30] is as follows: first, the data are each odd inverted and even inverted, after which transmission has carried out the usage of the sort of inversion that reduces greater the switching activity.

The scheme provided in [13] handled decreasing the coupling switching. On this approach, a complicated encoder counts the wide variety of Type I transitions with a weighting coefficient of one and the number of type II transitions with the weighting coefficient of two. If the quantity is greater than 1/2 of the link width, the inversion can do. Further to the complicated encoder, the approach most effective works at the patterns whose full inversion results in the link power reduction at the same time as not thinking about the patterns whose full inversions may additionally cause higher link power consumption. Consequently, the link power reduction done through this approach is not always as large as it is able to be. This scheme has based totally at the hop-by-hop approach. In another coding technique provided in [20], bunches of 4 bits are encoded with five bits. The encoded bits had been isolated the use of shielding wires such that the incidence of the patterns “101” and “010” had been avoided. These manners, no simultaneous type II transitions in two adjacent pair bits have triggered. This approach successfully

reduces the coupling switching activity. Despite the fact that the approach reduces the power consumption significantly and it will increase the data transfer time, hence the link energy consumption. This is because of the reality that for each 4 bits, six bits are transmitted which will increase the communication traffic. This approach also based on the hop-by-hop technique. A coding approach that reduces the coupling switching activity by taking the benefit of end-to-end encoding for wormhole switching has provided in [19] and it decreases the coupling switching activity by removing only type II transitions. In [18], three schemes presented based on power models of normal data, odd inverted data, even inverted data and fully inverted data.

In this paper, we proposed three data encoding schemes which are named as Normal/Odd inversion by considering the Self and Coupling transitions (NOSC), Full/Normal/Odd inversion by considering the Self and Coupling transitions (FNOSC) and Odd/Even/Full/Normal inversion by considering the Self and Coupling transitions (OEFNSC).

III. PROPOSED ENCODING SCHEMES

In this section, we present the Overview of the proposed data encoding techniques and detail description of the proposed encoding scheme whose intention is to reduce power dissipation by means of minimizing the coupling transition activities at the links of the interconnection network.

A. Overview of the proposed data encoding techniques

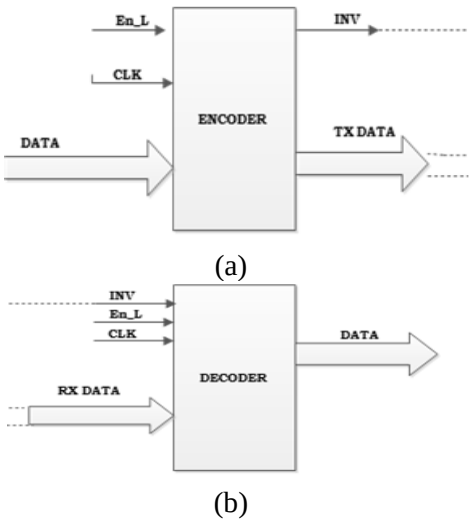


Fig.1 (a) Encoder (b) Decoder

Self and Coupling switching activities are the main source for power dissipation of interconnects. Therefore, proposed data encoding schemes aimed to reduce both the self and coupling activity factors. Fig.1 shows the general encoder and decoder blocks. Let us first depict the power model that contains distinctive elements of energy dissipation of interconnects. The dynamic power dissipation by the interconnects is

$$P_{dyn} = \frac{1}{2}\{\alpha_S(C_S + C_L) + \alpha_C C_C\} * V_{DD}^2 * F_{CLK} \quad (1)$$

Where α_S is the self-switching activity, α_C is the coupling switching activity, C_S is substrate capacitance, C_L is load capacitance, C_C is the coupling capacitance between two adjacent interconnects, V_{DD} is the supply voltage , and F_{CLK} is the operating clock frequency. Coupling transitions have classified as Type-I, Type-II, Type-III, and Type-IV in two wire models [13]. Type-I coupling transitions are happening when one of the interconnect switches and other interconnect remains same. Type-II coupling transitions are happening when two interconnects are switched simultaneously in opposite. Type-III coupling transitions are happening when two interconnects switched simultaneously on it. Type-IV coupling transitions are happening when two interconnects are not switches. The effective switched capacitance between the two adjacent interconnects varies from type to type, and hence the coupling switching activity α_C is a weighted sum of different types as shown in eqn (2)

$$\alpha_C = W_1T_1 + W_2T_2 + W_3T_3 + W_4T_4 \quad (2)$$

Where W_1 is the weight of the Type-I coupling transitions and it is equal to one , W_2 is the weight of Type-2 coupling transitions and it is equal to two, W_3 and W_4 are the weights of Type-III and Type-IV respectively and these equal to zero. Hence, Equation 2 becomes

$$\alpha_C = T_1 + 2T_2 \quad (3)$$

Therefore, Equation 1 becomes

$$P_{dyn} = \frac{1}{2}\{\alpha_S(C_S + C_L) + (T_1 + 2T_2)C_C\} * V_{DD}^2 * F_{CLK} \quad (4)$$

C_L is negligible as compared to C_S, so Equation 4 becomes

$$P_{dyn} = \frac{1}{2}\{\alpha_S C_S + (T_1 + 2T_2)C_C\} * V_{DD}^2 * F_{CLK} \quad (5)$$

Therefore $P_{dyn} \alpha \{\alpha_S C_S + (T_1 + 2T_2)C_C\}$. Here, three schemes named as Normal/Odd inversion by considering the self and coupling transitions (NOSC), Full/Normal/Odd inversion by considering the self and coupling transitions (FNOSC) and Odd/Even/Full/Normal inversion by considering the self and coupling transitions (OEFNSC).

B. NOSC data encoding technique

NOSC data encoding techniques is modified version of scheme-I that proposed in [18]. In this technique, first we have calculated self transitions and coupling transitions for normal data pattern and odd positional inverted data pattern to be transmitted. Pattern which gives the less number of transitions has selected to transmit.

C. FNOSC data encoding technique

FNOSC data encoding techniques is modified version of the scheme-II that proposed in [18]. In this technique, first we have calculated self-transitions and coupling transitions for normal data pattern, odd positional inverted data pattern to be transmitted and fully inverted data pattern to be transmit. Pattern which gives the less number of transitions has selected to transmit.

D. OEFNSC data encoding technique

OEFNSC data encoding techniques is modified version of scheme-III that proposed in [18]. In this technique, first we have calculated self-transitions and coupling transitions for normal data pattern, odd positional inverted data pattern to be transmitted, even positional inverted data pattern to be transmitted and fully inverted data pattern to be transmit. Pattern which gives the less number of transitions has selected to transmit.

IV. RESULTS

In this section, performance of proposed data encoding schemes is analysed in terms of the average efficiency of self-transition, Type-I coupling transition, Type-2 coupling transition, total coupling transition, total transition, energy of interconnects, delay and energy delay product. 1000-input vectors, 2000-input vectors, 5000-input vectors and 10000-input vectors with different data sizes as the 8-bit, 16-bit, 32-bit and 64bit are considered to analyse the performance of proposed data encoding schemes. Table 1 show the Type-1 and Type-2 Coupling transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit. Table 2 shows the Self and Total transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit.

Fig.2(a) describes the average self-transition efficiency. NOSC data encoding scheme provides average self-transition efficiency as 9.66%, 6.07%, 11.12% and 3.92% , FNOSC data encoding scheme provides average self-transition efficiency as 23.41%, 18.29%, 11.82% and 5.07% and OEFNSC data encoding scheme provides average self-transition efficiency as 51.21%, 23.67%, 15.62% and 7.39% for 8-bit, 16-bit, 32-bit and 64-bit respectively. Fig.2 (b) describes the average Type-1 coupling transition efficiency. NOSC data encoding scheme provides average Type-1 coupling transition efficiency as -14.87%, 2.06%, 6.99% and 3.05%. FNOSC data encoding scheme provides average Type-1 coupling transition efficiency as 7.17%, 8.11%, 10.76% and 5.53%. OEFNSC data encoding scheme provides average Type-1 coupling transition efficiency as 14.94%, 10.21%, 9.93% and 6.46% for 8-bit, 16-bit, 32-bit and 64-bit respectively. Fig.2(c) describes the average Type-2 coupling transition efficiency. NOSC data encoding scheme provides average Type-2 coupling transition efficiency as 83.03%, 69.78%, 58.03% and 63.62% , FNOSC data encoding scheme provides average Type-2 coupling transition efficiency as 89.66%, 72.83%, 56.98% and 64.85% and OEFNSC data encoding scheme provides average Type-2 coupling transition efficiency as 97.79%, 81.82%, 73.42% and 72.09% for 8-bit, 16-bit, 32-bit and 64-bit respectively. Fig.2 (d) describes the average total coupling transition efficiency. NOSC data encoding scheme provides average total coupling transition efficiency as 53.09%, 37.06%, 29.99% and 31.32% , FNOSC data encoding scheme provides average total coupling transition efficiency as 64.43%, 41.55%, 31.58% and 33.21% and OEFNSC data encoding scheme provides average total coupling transition efficiency as 72.45%, 47.22%, 38.53% and 37.08% for 8-bit, 16-bit, 32-bit and 64-bit respectively. Fig.2 (e) describes the average total transition efficiency. NOSC data encoding scheme provides average total transition efficiency as 43.11%, 29.97%, 25.91% and 25.33% , FNOSC data encoding scheme provides average total transition efficiency as 55.02%, 36.23%, 27.31% and 27.06% and OEFNSC data encoding scheme provides average total transition efficiency as 67.57%, 41.83%, 33.58% and 30.59% for

8-bit, 16-bit, 32-bit and 64-bit respectively. Efficiency of interconnects with proposed data encoding techniques in terms of Energy, Delay and Energy-Delay-Product (EDP) is analyzed in 45nm technology. Fig.4 describes the Energy, Delay and Energy-Delay-Product efficiency of data encoding schemes. NOSC data encoding scheme provides energy efficiency as 49.22%, 34.31%, 28.42% and 29.02% , FNOSC data encoding scheme provides energy efficiency as 60.79%, 39.49%, 29.94% and 30.85% and OEFNSC data encoding scheme provides energy efficiency as 70.56%, 45.13%, 36.63% and 34.59% for 8-bit, 16-bit, 32-bit and 64-bit respectively.

NOSC data encoding scheme provides delay efficiency as 63.36%, 46.23%, 37.09% and 39.71% , FNOSC data encoding scheme provides delay efficiency as 73.09%, 50.31%, 38.01% and 41.44% and OEFNSC data encoding scheme provides delay efficiency as 81.15%, 56.91%, 47.37% and 46.19% for 8-bit, 16-bit, 32-bit and 64-bit respectively. Fig.5 describes the Energy-Delay-Product (EDP) efficiency of data encoding schemes. NOSC data encoding scheme provides EDP efficiency as 81.39%, 64.68%, 54.96% and 57.21% , FNOSC data encoding scheme provides EDP efficiency as 89.45%, 69.94%, 56.57% and 59.5% and OEFNSC data encoding scheme provides EDP efficiency as 94.45%, 76.35%, 66.64% and 64.8% for 8-bit, 16-bit, 32-bit and 64-bit respectively. From the all results, we can conclude that NOSC data encoding technique has provided better performance than the Scheme-1[18], FNOSC data encoding technique has provided better performance than the Scheme-2 [18] and OEFNSC data encoding technique has provided better performance than the Scheme-3 [18]. Among the six data encoding techniques, OEFNSC provided better performance in all aspects.

Table 1(a) Type-1 coupling transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit.

METHOD	TYPE-1 COUPLING TRANSITIONS			
	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	22416	63823	150081	282236
SCH-1	37156	77069	147793	308125
SCH-2	29980	71341	146511	308730
SCH-3	22784	60968	135648	271791
NOSC	25767	62634	139775	274706
FNOSC	20819	58892	134449	267748
OEFNSC	19089	57735	135651	264910

Table 1(b) Type-2 coupling transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit.

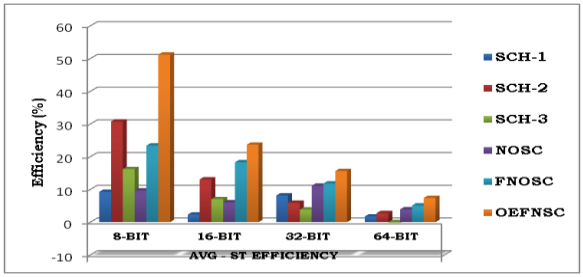
METHOD	TYPE-2 COUPLING TRANSITIONS			
	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	50868	67824	122662	245724
SCH-1	11970	30768	64932	132832
SCH-2	12604	31386	78730	136612
SCH-3	7426	23360	34924	67970
NOSC	8626	20570	52190	89162
FNOSC	5280	18534	53578	86450
OEFNSC	1146	12648	33024	68316

Table 2(a) Self transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit.

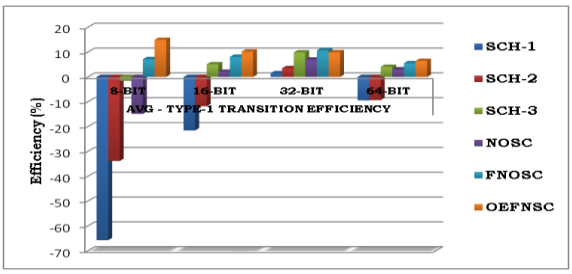
METHOD	SELF TRANSITIONS			
	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	21841	39026	75097	147492
SCH-1	19681	38113	69016	144877
SCH-2	15115	34027	70733	143740
SCH-3	18289	36223	72273	147684
NOSC	19717	36662	66762	141588
FNOSC	16712	31951	66110	140128
OEFNSC	10659	29795	63672	136956

Table 2(b) Total transitions for 10000 input vectors with data size of 8-bit, 16-bit, 32-bit and 64-bit.

METHOD	TOTAL TRANSITIONS			
	8-BIT	16-BIT	32-BIT	64-BIT
UNCODED	95125	170673	347840	675452
SCH-1	68807	145950	281741	585834
SCH-2	57699	136754	295974	589082
SCH-3	48499	120551	242845	487445
NOSC	54110	119866	258727	505456
FNOSC	42811	109377	254137	494326
OEFNSC	30894	100178	232347	470182



(a)



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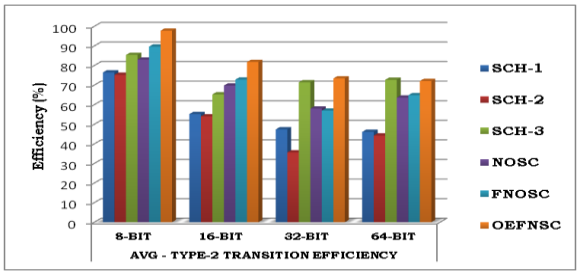

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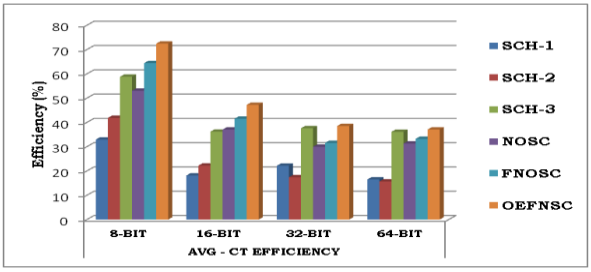

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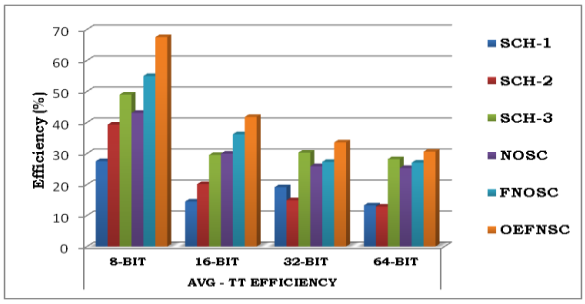

(e)

Fig.2 Average transition efficiency of various data encoding schemes for data sizes of 8-bit, 16-bit, 32-bit, and 64-bit (a) self-transition efficiency (b) Type-1 coupling transition efficiency (c) Type-2 coupling transition efficiency (d) Total coupling transition efficiency (e) Total transition efficiency.

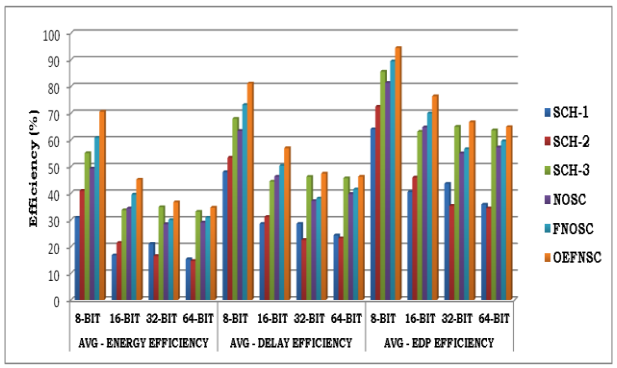

Fig.4: Energy, Delay, and Energy-Delay-Product (EDP) efficiency of data encoding techniques for 8-bit, 16-bit, 32-bit and 64-bit

V. CONCLUSIONS

In this paper, proposed data encoding techniques are independent of type of interconnect used and application handled of communication subsystem in SoC. Hence, these data encoding techniques are applicable to any type of interconnects to reduce the dynamic power dissipation of interconnects. The proposed schemes is to reduce not only the self-switching activity, but also the coupling switching activity that is especially liable for link energy dissipation in the deep sub-micron meter technology regime as compared to the previous encoding schemes proposed in the literature. An extensive assessment has accomplished to evaluate the impact of proposed data encoding schemes. Proposed data encoding techniques have provided better performance in all aspects with slight penalty of overhead.

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