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Research Article

Design of Reversible Comparator using Reversible Gates with Encoding Technique

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Abstract

Reversible logic has an alternate design technique to a conventional logic resulting in low power consumption and circuit delay. Comparators are a key element in most digital systems. In this project, 4-bit comparator based on priority encoder circuit is designed. Reversible logic gates performed the multiple operations in a single unit. This design consist mainly the feyaman gates. It is one type of reversible logic gates. The reversibility recovers bits loss from the designated input-output mapping and its applications have spread in various technologies like quantum computing nanotechnology and low power design. The 4-bit comparator using reversible gates to reduce optimization parameters like number of constant inputs, garbage outputs and quantum cost is verified by using Xilinx ISE software.

Keywords: Reversible logic; Comparators; Priority encoders; Logical delay path; Quantum cost; Low power.

Introduction

The reversible circuits (gates) that have one to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. Rolf Landauer, 1961. Whenever we use a logically irreversible gate we dissipate energy into the environment [1]. The loss of information is associated with laws of physics requiring that one bit of information lost dissipates kTln(2) of energy, where k is Boltzmann' constant and T is the temperature of the system. Interest in reversible computation arises from the desire to reduce heat dissipation [2].

Later Bennett, in 1973, showed that these kTln(2) joules of Energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits [3]. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in close proximity [4]. One of the emerging applications of reversible logic is in quantum computers.

A quantum computer consists of quantum logic gates [5]. The quantum logic gates perform elementary unitary operation on one, two or more two– state quantum systems called qubits [6]. In quantum computing qubit represents the elementary unit of information corresponding to the classical bit value 0 and 1 [7]. Any unitary operation is reversible in nature and hence quantum computers must be built from reversible logical components [8]. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates [9]. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs; also they must use minimum number of constant input [10].

Research methodology

Basic reversible gates

Reversible logic

The reversible logic operations do not erase (lose) information and dissipate very less

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heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low power CMOS design, optical computing, quantum computing and nanotechnology. The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network composed of quantum logic gates or circuits; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. The quantum networks cannot be directly deduced from their classical Boolean counterparts which are clearly irreversible. Thus, quantum arithmetic must be built from reversible logic components. The reversible logic gate or circuit is a n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this objective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits.

Reversible comparator using reversible gate

Reversible logic has the feature to generate one to one correspondence between its input and output. As a result no information is lost in reversible logic and zero power dissipation would be achieved only if the network consists of reversible gates. Synthesis of reversible logic is more complicated than irreversible one as it imposes many design constraints. A reversible circuit therefore should have the following attributes: Since garbage outputs are not used as primary outputs so any realization technique should keep garbage as minimum as possible. Each reversible gate has a particular quantum cost so any realization technique should keep the number of reversible gates as minimum as possible. Input lines that are either 0 or 1 known as constant inputs should be as minimum as possible. Various reversible comparator architectures have been proposed which are aimed at reducing the delay and the quantum cost of the circuit.

The present work proposed two new reversible designs which use the concept of priority encoding, and also modifications to the existing designs for optimizing the quantum cost and delay. The use of negative control lines in a Toffoli gate is explored in the designs; as a result the designs proposed in this work use only the standard reversible gates for which the synthesis algorithms are available in literature (Table 1). The proposed priority encoding based designs are based on the techniques described. These designs significantly reduce the delay and quantum cost when compared to the existing serial and equations based designs.

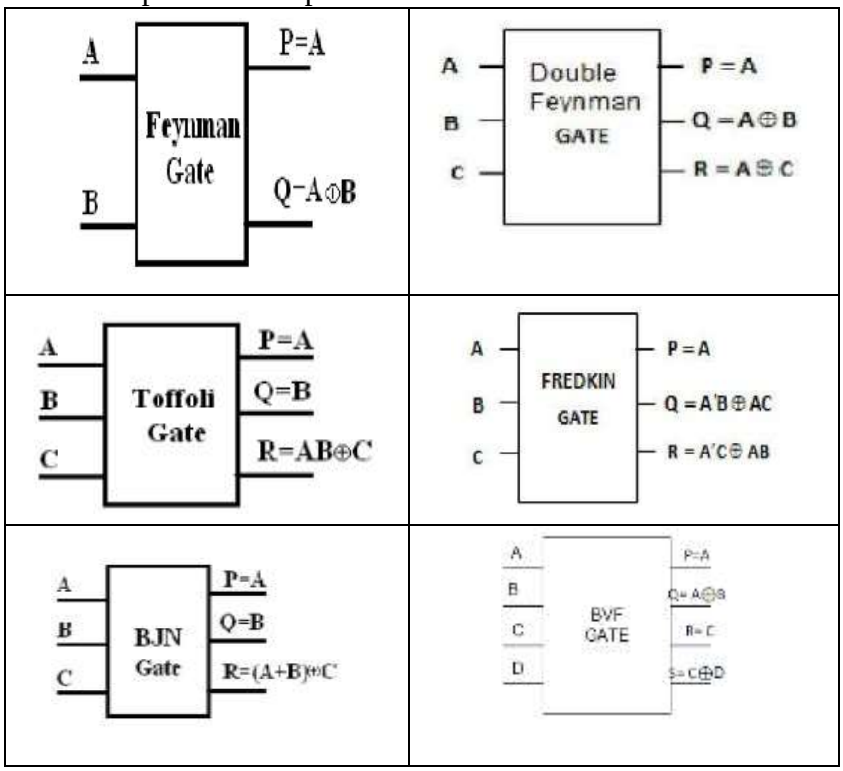

Fig. 1. Reversible gates

Priority encoder

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interupts requests by acting on the highest priority encoder. If two or more inputs are given at the same time, the input having the highest priority will take. An example of a single bit 4 to 2 encoder, where highest-priority inputs are to the left and "x" indicates an irrelevant value - i.e. any input value there yields the same output since it is superseded by higher-priority input. The output V indicates if the input is valid.

Results and discussion

4 bit Reversible comparators

Fig. 2 shows the 4 bit reversible comparators. it consist of 3 types of reversible gates BJN gates, Toffili gates, Tr gates ,this type of gates mainly used to reduce the power quantum cost and delay.

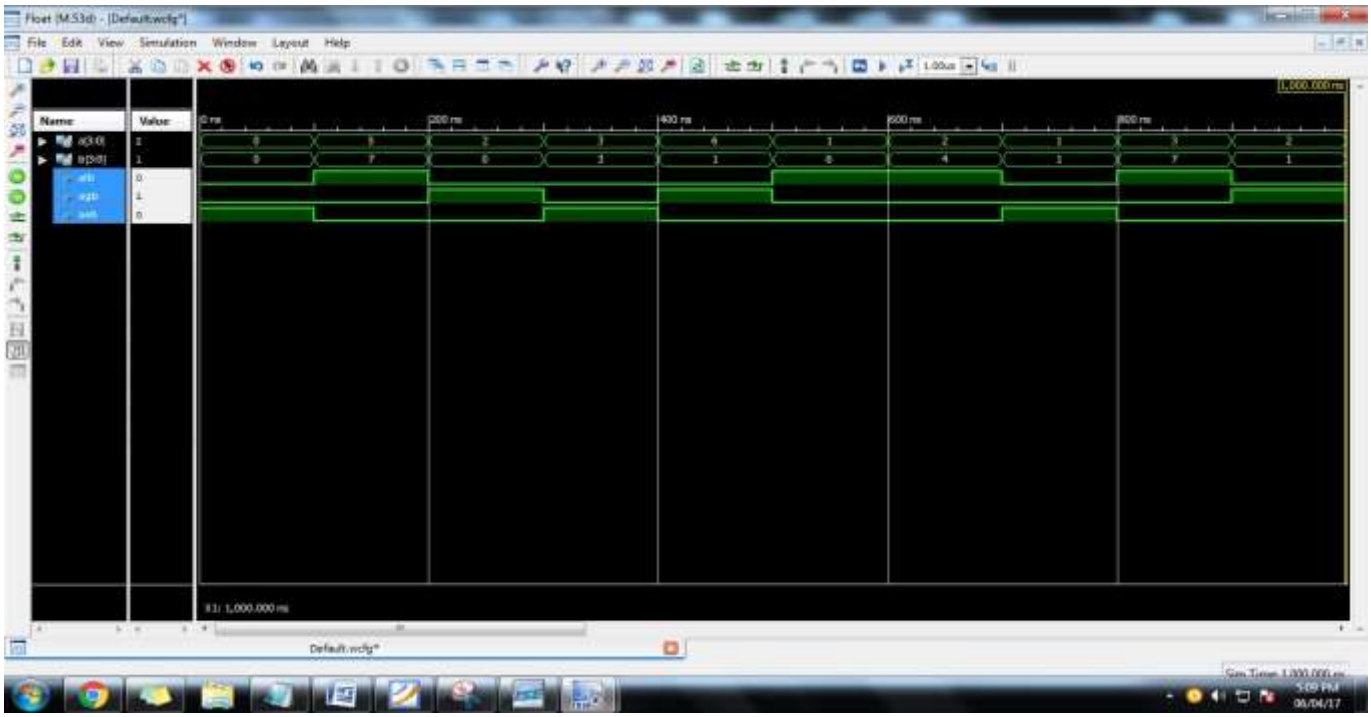

Fig. 2. Output waveform of 4 bit reversible comparator

4 bit Reversible comparator using Reversible gates using priority Encoding technique

Fig. 3 shows we propose two new reversible designs which use the concept of priority encoding, and also modifications to the existing designs for optimizing the quantum cost and delay. The use of negative control lines in a Toffoli gate, tr gate, Bvf gates are explored in the designs; as a result the designs proposed in this work use only the standard reversible gates for which the synthesis algorithms are available in literature. The proposed priority encoding based designs are based on the techniques described. These designs significantly reduce the delay and quantum cost when compared to the existing serial, clock based comparators and equation based designs.

Conclusions

The main idea of this project is to introduce the low power and high performance 4-bit reversible comparator. This 4-bit reversible comparator is based on reversible logic gates with priority encoding technique. The proposed design of reversible comparator consist of feyaman gate, toffili gate and, BJN gates. The proposed reversible comparator design compared with prior designs that result to optimized in number of constant inputs, number of garbage outputs and quantum cost, power reduction and delay. These circuits are designed in verilog and verified using xilinx ISE software. This can be used for various low power and applications.

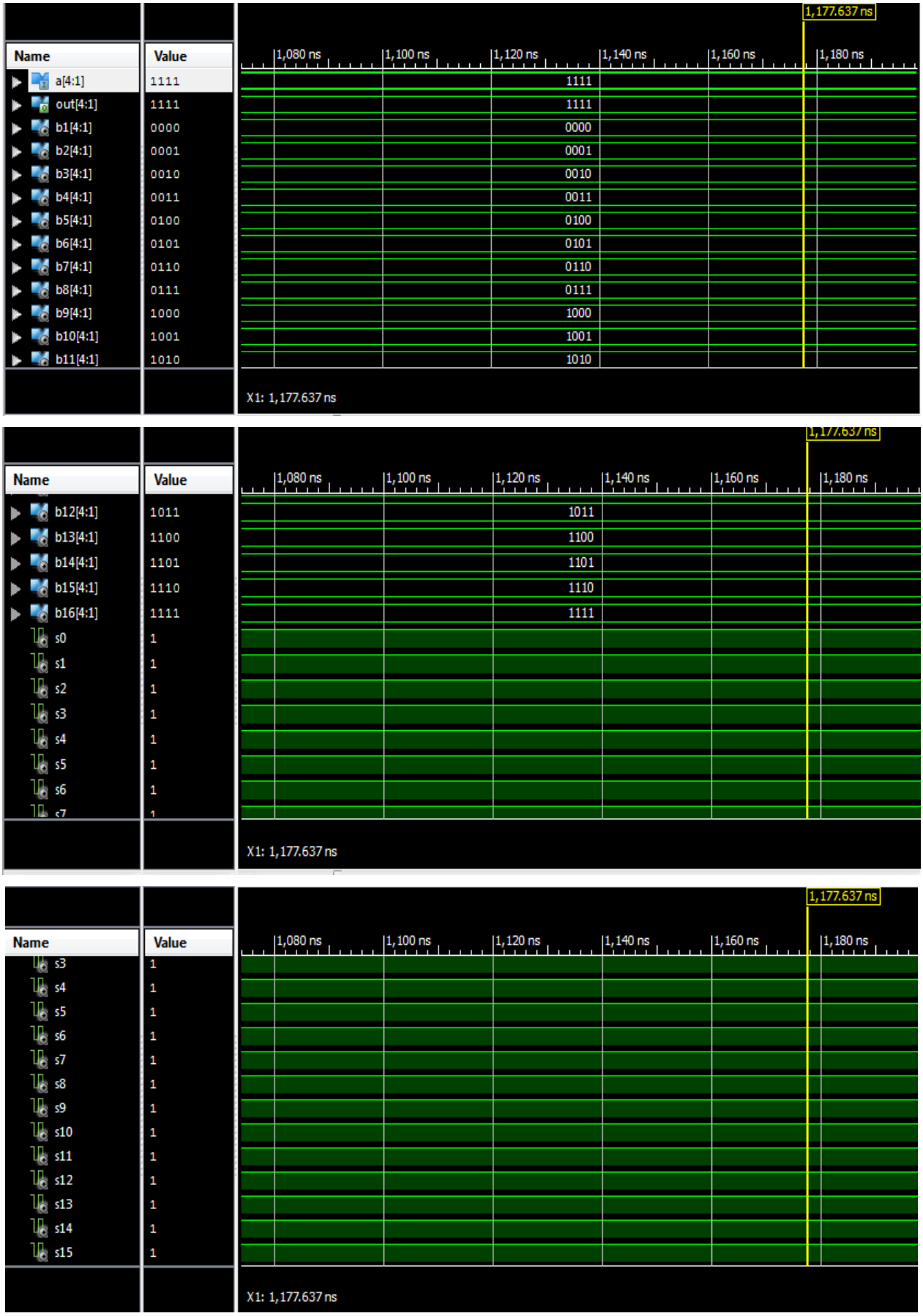

Fig. 3. Various output waveforms of reversible comparator with priority encoding technique

Conflicts of Interest

Authors declare no conflict of interest.

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