

# Hybrid CMOS and CNFET Low Pass gm-C Filters

S. B. Rahane<sup>1</sup>, A.K. Kureshi<sup>2</sup>

<sup>1</sup>*Matoshri College of Engineering and Research Center, Savitribai Phule Pune University  
Nashik, India*

*(E-mail: rahanesandip@gmail.com)*

<sup>2</sup>*Vishwabharati Academy's College of Engineering, Savitribai Phule Pune University  
Ahemadnagar, India*

*(E-mail: akkureshi@rediffmail.com)*

**Abstract**—A hybrid CMOS-CNFET low pass gm-C filters to satisfy very low frequency cutoffs for biomedical applications are proposed in this paper. A first order, second order and fifth order elliptic low pass filter structures are proposed using a hybrid CMOS-CNFET Operational Transconductance Amplifier (OTA). Realized filter circuits satisfy ultra-low power consumption requirement of wearable and implantable biomedical devices. The transistors used in the circuit operate in weak inversion to achieve ultra-low power consumption. Application of integrated deep trench capacitors and Integrated Passive Device (IPD) Technology is also discussed.

**Keywords**—Carbon Nanotube Field Effect Transistors; Operational Transconductance Amplifier; gm-C filters; Deep Trench Capacitors; Integrated Passive Devices.

## I. INTRODUCTION

Real world analog signals contain unwanted noise and interference. Analog signal processing involve systematic rejection of unwanted noise and preservation of signal of interest. Different types of filters can be employed to achieve this task. Filters can be analog or digital filters. Analog filters deals with continuously varying signals while digital filters process sampled data. Analog filters include passive filters utilizing passive components such as resistors, capacitors and inductors. Active filters utilize active devices such as operational amplifiers (OPAMPS) or operational transconductance amplifiers (OTA). Active filters include active RC filters, gm-C filters, LC filters and switched capacitor filters. Amongst them gm-C filters are suitable for a wide frequency range starting from low frequency to very high frequencies. gm-C filters are designed with OTAs as their main building block. gm-C filters have gained significant attention due to their on chip integration capability, low power consumption and simple frequency tuning. Changes in capacitors or OTA transconductance (gm) provides a simple way to do frequency tuning in gm-C filters [1]. The gm-C filters find applications in many wireless, wire line systems and biomedical signal processing. Examples include multi-standard radio receivers [1], continuous time delta-sigma modulators [2], acoustic front ends [3], cochlear prosthesis [4], Bluetooth receivers [5], neural signal processing [6], electroencephalogram (EEG) [7]. For

biomedical applications involving slow / low frequency electrical activity of the physiological signals gm-C filters are becoming the preferred analog front end circuits. In this paper we propose gm-C filters based on a hybrid CMOS-CNFET OTA.

## II. HYBRID CMOS-CNFET INTEGRATION

Hybrid CMOS-CNFET integration at nano-scale in a complementary manner to reap benefits of both the technologies still remain a challenge. However technological breakthrough successfully demonstrated by Stanford researchers in their monolithic 3-D integrated hybrid CMOS-CNFET nanosystem [8] have created a ray of hope in this direction. The researchers demonstrated the capabilities to fabricate the chip using a process that is compatible with existing silicon fabrication technology. Heterogeneous integration of CNFET gas sensors and logic, data storage (RRAM), CMOS and CNFET logic were achieved with the dense vertical interconnects on a 3-D chip. A low temperature fabrication process (maximum 200°C) enabled stacking CNFET logic and RRAM on the top of conventional CMOS [8, 9]. To utilize these technological advances up to full potential one needs to explore applicability of this technology for analog domain involving analog front end amplifiers, filters and signal processing. Especially such type of hybrid 3-D integration is a promising approach for wearable and implantable biomedical applications. Earlier several attempts have been made to investigate various hybrid CMOS-CNFET circuits and systems. An ultralow voltage regime power gating scheme involving a CMOS logic and CNFET sleep devices was proposed in [10]. The hybrid scheme achieved reduced sleep mode leakage power consumption and reduced wake up time for the power gating structure. A cascode amplifier utilizing a hybrid combination of nMOS and pCNFET was used by researchers [11] as a vehicle to demonstrate hybrid CMOS-CNFET monolithic integration.

## III. HYBRID OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Fig. 1 shows the hybrid OTA used as a gm-C filter transconductor. Hybrid topology consisting of conventional CMOS P type devices and N type CNFETS is used. The circuit simulations are carried out using HSPICE environment with PTM 32nm low power device models for CMOS transistors and Stanford University model [12,13] for CNFETs have been used. The PMOS devices has been sized with W=100 and L=2. N type

CNFETs with chiral vector (19, 0) and number of nanotubes equal to 3 have been used. As compared to CMOS devices CNFETs offer higher drive current, lesser process variations and less leakage current. The output current  $I_{out}$  of the OTA is given by expression,

$$I_{out} = gm (V_p - V_m) \tag{1}$$

Where  $gm$  is the transconductance of the OTA. The OTA acts as a voltage controlled current source with both its input and outputs as very high impedance nodes. Unlike OP-AMPS OTAs do not require output driver circuits and bias the resistive elements. This results in low power consumption making OTAs more suitable for neural amplifier ICs for electrocorticograms and electroneurograms [14]. OTAs of this kind are more suitable for driving only capacitive loads and hence can be used as building blocks of gm-C filters.

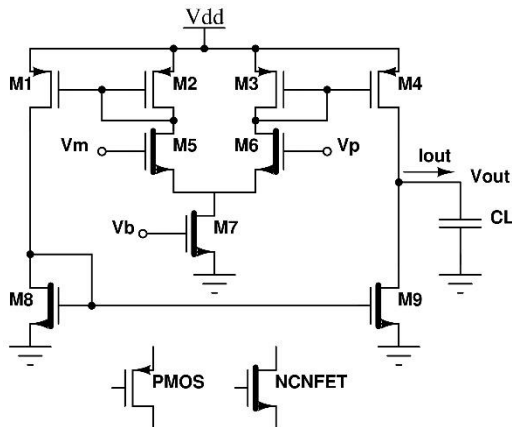
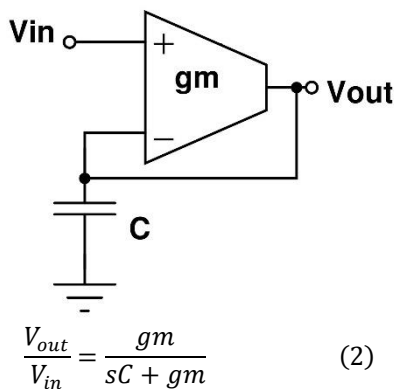


Fig. 1 Hybrid CMOS-CNFET OTA

Unlike active RC filters gm-C filters do not need resistive components and hence are better suited for on chip integration. The transistors in the proposed circuit are biased so as to force them all to operate in weak inversion. This has resulted in average power consumption of the OTA to be just 4.45μW.



$$\frac{V_{out}}{V_{in}} = \frac{gm}{sC + gm} \tag{2}$$

Fig. 2 First order low pass gm-C filter

Weak inversion or subthreshold operation of the transistors minimizes their transconductances and also improves the transconductor linearity. Proposed OTA can be used to design gm-C filters that can deal with low frequency bio-medical signals. Many of the times biomedical systems are made to be wearable or implantable with power consumption being the most important constraint.

IV. HYBRID GM-C FILTERS

A first order low pass, second order low pass and a fifth order elliptic low pass filters have been proposed to satisfy biomedical signal filtering requirements. The hybrid CMOS-CNFET transconductor shown in Fig. 1 is used as a building block for the proposed filter structures. Low pass filter is an essential requirement for biomedical applications such as Electrocardiogram (ECG), Electroencephalogram (EEG), Electrooculogram (EOG), Electromyogram (EMG), respiration and snoring monitoring. Biomedical signal processing involves very low frequency cutoff low pass filters. Typical recommendations by American Academy of Sleep Medicine (AASM) for EEG and EOG are 35Hz. Recommended cutoffs for ECG, EMG, respiration and snoring are 70Hz, 100Hz, 15Hz and 100Hz respectively [15]. Typical low pass filter cutoffs for diagnostic purpose for ECG, EEG and EMG are 150Hz, 70Hz and 500Hz respectively. Satisfying these very low cutoffs is a challenging task using conventional CMOS IC fabrication technology. To achieve such low cutoffs using gm-C filters need large capacitors. However technological advances such as embedded deep trench capacitors and Integrated Passive Device (IPD) technology has enabled usage of large value capacitors for very low frequency cutoff filters. Wide range of capacitors from pF to μF can be realized in a CMOS high density deep trench technology [16, 17]. TSMC High density deep trench capacitors have been used in latest Apple iPhone 7. IPD technology enables high density passive component integration in a CMOS chip [18].

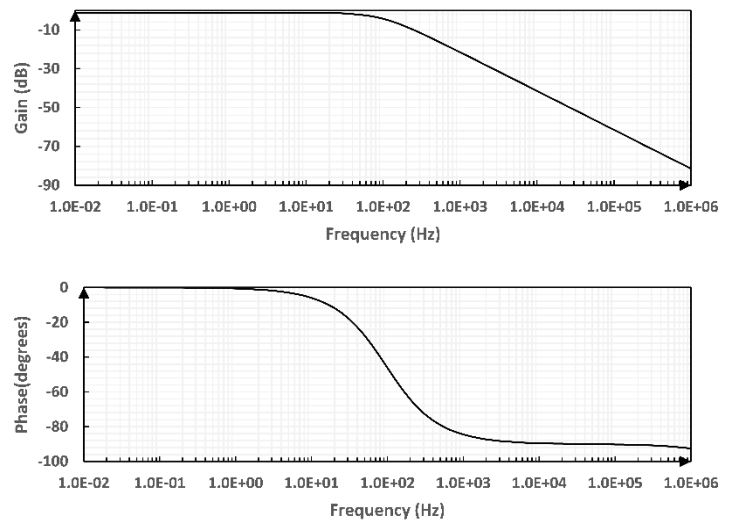
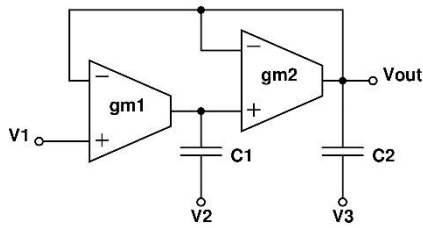


Fig. 3 Gain and phase plots for first order low pass gm-C filter



$$\frac{V_{out}}{V_{in}} = \frac{gm1gm2}{s^2C1C2 + sC1gm2 + gm1gm2} \quad (3)$$

Fig.4 Second order low pass gm-C filter

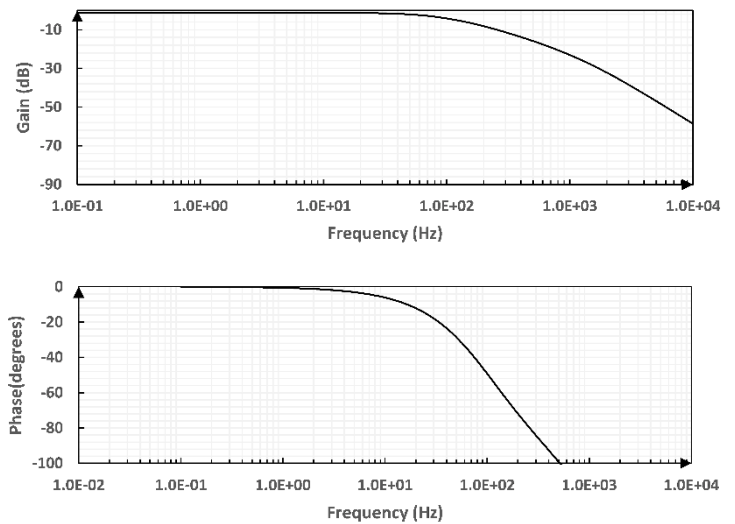


Fig.5 Gain and phase plot for second order low pass gm-C filter

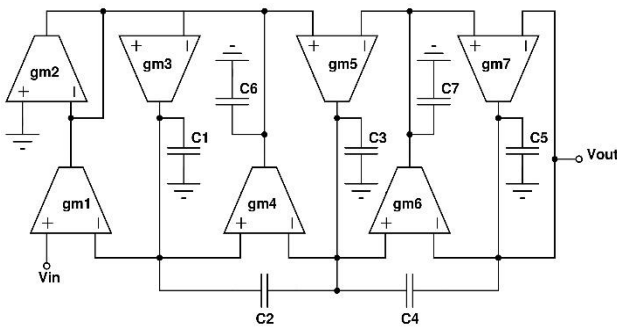


Fig. 6 Fifth order low pass elliptic filter

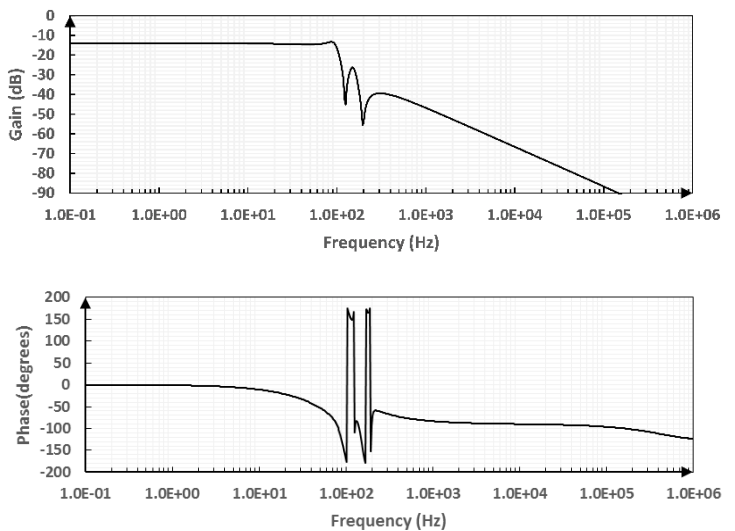


Fig. 7 Gain and phase plot for fifth order low pass elliptic filter

Fig. 2 shows a simple low pass filter realization using the proposed hybrid OTA. This type of structure offers a simple electronic tuning for the filter cutoff frequency. The cutoff frequency can be tuned either by adjusting transconductance (gm) or the capacitor value. The gm can be adjusted by varying the bias current of the OTA. The proposed design uses the approach of fixing gm and tuning the frequency by selecting proper value capacitor to satisfy cutoff frequency requirements of different biomedical signals such as ECG, EEG, EMG etc. The most power efficient approach for the design of gm-C filter is to keep bias current as low as possible. Keeping a small gm results in a lower power consumption and allows us to satisfy ultra-low power requirements of wearable, implantable and battery powered biomedical systems. The transistors are sized so as to achieve a 0.1µA bias current. This serves a dual purpose ie. Significant reduction in power consumption while satisfying very low cutoffs as required by biomedical applications. Fig. 3

shows the gain and phase plots for the proposed first order filter. A cutoff frequency of 100Hz is achieved with a capacitance value of 3000pF. The filter cutoff frequency can be tuned from 300kHz to 30Hz by choosing a capacitor between 1pF to 10000pF. The large value capacitor can be realized using deep trenching and IPD process. The average power consumed by the proposed circuit is 0.2169µW.

Fig. 4 shows the second order gm-C filter using the hybrid OTA. The circuit can be configured as either low pass, high pass, band pass or notch circuit based on inputs applied. If V1=Vin and V2 and V3 are grounded then the circuit functions as a low pass filter. The transfer function of the low pass version is given by Eq. 3. The output expression for the filter is given by,

$$V_{out} = \frac{s^2C1C2V_3 + sC1gm2V_2 + gm1gm2V_1}{s^2C1C2 + sC1gm2 + gm1gm2} \quad (4)$$

The desired cutoff frequencies can be adjusted by deciding capacitor ratios while keeping  $g_{m1}=g_{m2}=\text{constant}$ . To achieve 100Hz cutoff frequency  $C_1=3000\text{pF}$  and  $C_2=200\text{pF}$  are used. For 70Hz cutoff  $C_1=50\text{pF}$  and  $C_2=4000\text{pF}$  is used. Further even smaller cutoff frequency of 30Hz can be obtained if  $C_1=500\text{pF}$  and  $C_2=10000\text{pF}$ . The circuit consumes  $0.4336\mu\text{W}$  power.

Fig. 6 shows the fifth order low pass elliptic filter realization using hybrid OTA. Elliptic filter exhibits sharper roll-offs at the cost ripples in the pass band and stop band. The circuit achieves 100Hz cutoff frequency with  $C_1=2000\text{pF}$ ,  $C_2=2000\text{pF}$ ,  $C_3=2000\text{pF}$ ,  $C_4=2000\text{pF}$ ,  $C_5=2000\text{pF}$ ,  $C_6=2500\text{pF}$ ,  $C_7=1000\text{pF}$ . Average power consumed by the circuit is  $1.4714\mu\text{W}$ . Limiting the bias current in the OTA and weak inversion operation of the transistors allows very low cutoffs desired for biomedical signals. The gain and phase plots for the fifth order elliptic low pass filter are shown in Fig. 7.

## V. CONCLUSION

Ultra-low power gm-C filter circuits using hybrid CMOS-CNFET technology for the biomedical applications has been presented in this paper. The first order filter consumes  $0.2169\mu\text{W}$ , the second order filter consumes  $0.4336\mu\text{W}$  while the fifth order elliptic filter consumes  $1.4714\mu\text{W}$ . Desired cutoff frequencies are obtained by adjusting capacitor values while maintaining a fixed transconductance. Heterogeneous integration of conventional CMOS, CNFETs and IPDs have been proposed for the biomedical filter application.

## REFERENCES

- [1] M. S. Oliveira, P. C. de Aguirre, L. C. Severo, A. G. Girardi and A. A. Susin, "A digitally tunable 4th-order Gm-C low-pass filter for multi-standards receivers," 2016 29th Symposium on Integrated Circuits and Systems Design (SBCCI), Belo Horizonte, 2016, pp. 1-6.
- [2] J. Huang, S. Yang and J. Yuan, "A 75 dB SNDR 10-MHz signal bandwidth Gm-C-based sigma-delta modulator with a nonlinear feedback compensation technique," in IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 62, pp. 2216-2226, Sept. 2015.
- [3] K. Badami, V. R. Pamula and M. Verhelst, "A switched-capacitor degenerated, scalable gm-C filter-bank for acoustic front-ends," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 818-821.
- [4] H. C. Chu, Y. H. Huang and C. C. Hung, "Low-power CMOS bandpass filter for application of cochlear prosthesis," 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, 2016, pp. 1-4.
- [5] A. Selvakumar and A. Liscidini, "Current-recycling complex filter for bluetooth-low-energy applications," in IEEE Trans. on Circuits and Systems II: Express Briefs, vol. 62, pp. 332-336, April 2015.
- [6] V. S. Ghaderi, D. Song, J. Choma and T. W. Berger, "Nonlinear cognitive signal processing in ultralow-power programmable analog hardware," in IEEE Trans. on Circuits and Systems II: Express Briefs, vol. 62, pp. 124-128, Feb. 2015.
- [7] S. A. Gallegos and H. F. Huq, "A 128.7nW neural amplifier and Gm-C filter for EEG, using gm/ID methodology and a current reference without resistance," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, 2014, pp. 876-880.

- [8] M. M. Shulaker, et al., "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip," Nature vol. 547, pp. 74-78, 2017.
- [9] M. M. Shulaker, et al., "Monolithic 3D integration: a path from concept to reality," Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition. EDA Consortium, 2015, pp. 1197-1202.
- [10] K. K. Kim, Y.B. Kim, and K. Choi, "Hybrid CMOS and CNFET power gating in ultralow voltage design," IEEE Trans. on Nanotechnology, vol. 10, pp. 1439-1448, Nov. 2011.
- [11] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H. Wong, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," IEEE Trans. on Nanotechnology, vol. 7, pp. 636-639, Sept. 2008.
- [12] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: model of the intrinsic channel region," in IEEE Trans. on Electron Devices, vol. 54, pp. 3186-3194, Dec. 2007.
- [13] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: full device model and circuit performance benchmarking," in IEEE Trans. on Electron Devices, vol. 54, pp. 3195-3205, Dec. 2007.
- [14] K.A. Ng, E. Greenwald, Y.P. Xu, N.V. Thakor, "Implantable neurotechnologies: a review of integrated circuit neural amplifiers," in Medical and biological engineering and computing, vol. 54, pp.45-62, Jan. 2016.
- [15] M.E. Wells, "Technical corner: Low-Pass (High Frequency) filters, AAST A2zzz magazine, pp.28-29, Mar. 2010.
- [16] H. Johari and F. Ayazi, "High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage," in IEEE Trans. on Components and Packaging Technologies, vol. 32, pp. 808-815, Dec. 2009.
- [17] G. Wang *et al.*, "Scaling deep trench based eDRAM on SOI to 32nm and Beyond," 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, 2009, pp. 1-4.
- [18] C. Y. Hsiao, S. S. H. Hsu and D. C. Chang, "A compact V-band bandpass filter in IPD technology," in IEEE Microwave and Wireless Components Letters, vol. 21, pp. 531-533, Oct. 2011.



**S. B. Rahane** was born in Sangamner, MS, India in 1978. He received the Bachelor of Engineering degree from University of Pune in 2000, and Master of Engineering degree from Dr. Babasaheb Ambedkar Marathwada University, Aurangabad in 2008. He completed Post Graduate Diploma in Advanced Computing (PG-DAC) from Center for

Development of Advanced Computing (CDAC-ACTS) in 2001. He is currently pursuing Ph.D. degree in Electronics and Telecommunication Engineering in Savitribai Phule Pune University, India. His research interests include emerging nano-electronic devices, circuits and systems, carbon nanotube field effect transistors, analog electronic circuits, ultra-low power circuits and hybrid CMOS-CNFET electronic circuits. He is working as Assistant Professor in Department of Electronics Engineering, Amrutvahini College of Engineering, Sangamner, India. He has been a member, IEEE since 2010 and Life Member, Indian Society for Technical Education (ISTE). He is also a member of IEEE Circuit and Systems Society and IEEE Computer Society.



**Dr. A.K. Kureshi** was born in Beed, MS, India in 1970. He received the Bachelor of Engineering degree in 1994 and Master of Engineering degree in 2004 from Dr. Babasaheb Ambedkar Marathwada University, Aurangabad. He received the Ph.D. degree in VLSI Design from Aligarh Muslim University (AMU), Aligarh, India

in 2010. His research interest includes low power circuit design, Field Programmable Gate Array (FPGA) architecture, carbon nanotube interconnects, nanofabrication technologies and low noise amplifiers. Dr. A.K. Kureshi was a recipient of Engineering Achievement award by Institution of Engineers India (IEI) and best paper award at International Conference by Pentagram research center Hyderabad. He is author of a book on Communication Engineering and more than 40 research articles in refereed journals and conferences. He is a life member of Indian Society for Technical Education (LMISTE), Fellow Institution of Engineers (FIE) India and member of Institute of Electrical and Electronics Engineers (IEEE).