Design and Performance analysis of Adaptive-XY over N-XY and DO Routing on FPGA Platform

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***Abstract*—**Network on Chip (NoC) is an attractive alternative to bus-based technology in communication networks. The research Article proposes the NoC- based Router architectures with adaptive routing algorithm. The Normal-XY (N-XY) and Dimension order (DO) Routing are also designed for performance analysis purpose. It consists of the input register, priority encoder, packet formation, and different routing algorithms. The input registers store the data information from IP Cores via a Network interface (NI); then the priority encoder provides the select line to the corresponding input. Packet formation is done based on the packets received through the encoder. The Adaptive-XY (A-XY) Routing algorithm is based on the adaptive nature of XY Flow direction. The two dimensions are in X, and Y flow with less number of routing nodes are processed, and packets are assists to the destination with less congestion. The performance analysis of proposed router and 2X2 Mesh NOC with Adaptive –XY Routing algorithm over Normal-XY (N-XY) and Dimension order (DO) Routing is improved with hardware constraints which include Chip area, Operating Frequency, and Power consumption on FPGA platform. Factors for further improvements have been suggested.

***Keywords*—** *Adaptive –XY; Dimension order; FPGA; Mesh network; Normal-XY; NOC; priority Encoder; Packet; Router.*

I. INTRODUCTION

The multi-core System-on-chip (MC-SoC) is complicated to perform high-performance operations. The suggested alternative is Network on Chip (NoC). These architectures mainly include routers, network interfaces, and adapters. New router architectures are built by using topology designs - bus, star, ring, and mesh. NoC router consists of I/O Buffers with FIFO module, switching element, arbitration and routing modules. The Routers are interconnected to IP-Cores and Processing Elements (PEs) via the network interface. The general architecture of NoC-router using different topology include mainly The IP-Cores, PEs, and processors, with application modules like audio, video codec and specific modules. The communication and memory modules are also part of the NOC Based MPSOC. Routing algorithms like classical routing, adaptive routing, and deterministic routing techniques are used [1] to perform routing operations. Switching techniques like a store and forward, virtual channel, and worm-hole switching are used to transport the data packets between the source and destination nodes. FPGA Based system supports the flexible, transparent and performance oriented NoC routers in communication networks. Every NOC implementation has specific requirements to meet with performance metrics which includes the low latency, high throughput, and Low power consumption. The NOC Modules meets with flexible, scale and reprogrammable architectures. Our designed NoC router architecture incorporates input register, priority encoder, packet (flit) formation, and Different routing algorithms. The worm-hole switching technique is adopted for packet flit formation. A priority-based encoder is used to select the prior inputs out of five input ports.

In this research work, a cost-effective, optimized Router for NOC Based MPSOC using Adaptive –XY Routing algorithm Over N-XY and DO Routing algorithms. The existing research work of the Different Routers with algorithms will be elaborated with research gaps in section II. The part III describes the complete proposed Router design with hardware architectures for NOC with routing algorithms are explained in detail. Section IV explains the performance metrics of the recommended router and mesh 2X2 NOC design using Adaptive –XY Routing algorithm over N-XY and DO routing algorithms results in detail. Section V concludes with the clues on overall design with improvised constraints.

II. RELATED WORK

In this section, we discuss the existing router architecture concerning the NoC platform. Freitas et al. [1] have presented a programmable NoC router architecture for multi-Clusters. A router includes clusters of cores, input buffers, hypercube topology based reconfigurable cross Switch (RCS) and arbiter, decoder, buffers. They are interconnected to programmable NoC, which in turn provides the routing and packet switching. Area occupation and power consumption details for high signal and low signal transition are analyzed. Ranjana et al. [2] explains about the router design for MPSOC implementation. It contains the input port with FSM controller and crossbar switch with XY Routing. The synchronous frequency of the router is calculated, and the message throughputs are analyzed. The scalability issues of round-robin arbiters for NoCs have discussed in Maher et al. [3] The different arbiters include acyclic, Multi fixed priority arbiter, a programmable priority encoder (PPE), fully combination logic circuit (FCLC) arbiter, Resource sharing PPE are explained. Methodologies to check the scalability issues and overcome the performance

shortcomings have been analyzed. To enhance the parallel computation of multi-core systems Duoli et al. [4] have presented the Dual-port NoC architecture. Each router can communicate one at a time in a duplex way. The router module includes the I/O port FSMs encoder, decoder and arbitration process along with 6x6 crossbar switch. Analyzing the hardware resource consumption along with throughput and latency concerning the traditional 2d-mesh router is intriguing. Sudhir et al. [5] have presented the high throughput, low-latency NoC module for computation systems. The switch is explained in detail with packet switching flow. Interface Bridge is provided through wishbone bus to NOC. 2X2 Mesh router is designed and analyzed with performance parameters like Slices, LUT's, latency and maximum operating frequency of the selected FPGA device. The verification of a 5-port router is analyzed in Choudhari et al. [6] for NoC. The router module contains register, demultiplexer, FIFO module, and FSM controller. FSM Controller is used to controlling the data packets. The indicated results show marked improvements with previous versions of five port router. Kashwan et al. [7] present the optimized novel NoC router with round-robin arbitration process. To find out the routing path they have used Optimal Address Based Router (OABR). The power, area, and delay of the router are estimated and tabulated.

Chen et al. [8] present pipelined router design with buffer configuration approach. To improve the pipelined routing, they have split the router operation into two logic operations. Buffering technique is used to achieve low delay between routing. Analysis of mesh, ring and Torus Router NoC are designed and compared in Arpit et al. [9]. The design consideration, topology selection, FPGA synthesis and results of a simulation are explained for 256 X 256 topology network. K.swamy et al. [10-11] have presented the optimized NoC design using random arbiter. The router includes with priority encoder, random arbiter and crossbar switch with XY routing. 2x2 and 4x4 NOC architectures are compared with previous architectures with area improvements. Mayank et al. [12] present the FPGA Based router architecture which includes the FIFO buffers, multiplexers, and fixed arbiter complete one single router. All these references have been thoroughly analyzed concerning their pitfalls. In our implementation, we tried to overcome these drawbacks.

III. PROBLEM STATEMENT

It has been noticed from the literature reviews, the significant works carried on NOC based Router with different routing algorithms are based on the software approaches are quite good. But very less amount work for hardware approaches on Router design for NOC Based MPSOC. The relevant and research issues which are yet to carry of hardware-based approaches. The research gaps from the previous works are identified and explained. Most of the Router design works done on frequently used Network simulator tools. As per hardware modeling concern, Most of the work towards on router design is conventional approaches. Very less emphasis on benchmark router to refer for NOC based MPSOC for real-time usage. Lack of optimizations routing algorithms in the existing works of a router to improve the performance over NOC. The most of the current NOC Routers are involved which is facing less cost effective solutions over SOC platform. In research point view, very few works on NOC Based Router with best routing algorithm in hardware viewpoint. Hence a novel optimized, cost-effective solution is required to fulfill the above research gaps with better outcomes. The next section describes the proposed design with the methodology to address the deficiencies.

IV. PROPOSED ROUTER DESIGN

To improve the hardware complexities in NOC based MPSOC applications, a cost-effective router architecture is designed using Adaptive XY Routing and to analyze the performance metrics with the Normal-XY and Dimension order (DO) Routing algorithms are developed. The proposed single router internal architecture is as shown in figure 1. The single router mainly consists of four blocks namely- input register, priority encoder, packet (flit) formation block, and Adaptive XY-routing algorithm. The single router has 5- input ports along with 5-bit congestion input and 5-output ports. The input ports are named as 16-bit local input (li), east (ei), west (wi), south (si), north (ni) and 5- bit congestion. Output ports are 8-bit local output (lo), 16-bit east (eo), west (wo), south (so) and north (no) outputs. The input register is used to receive and store the information data from the other routers and the network interface (as local inputs) as well. The stored information packets act as input to the priority encoder. The priority encoder works based on the input with the highest priority will take precedence. The priority encoder outputs are fed to packet formation block. In packet formation, the packets are formed based on the destination address of X and Y and priority output. Once packet formation is completed, they are performing according to the Routing algorithm. From the routing algorithms, router outputs are generated as packets from the source to the destination routing node.

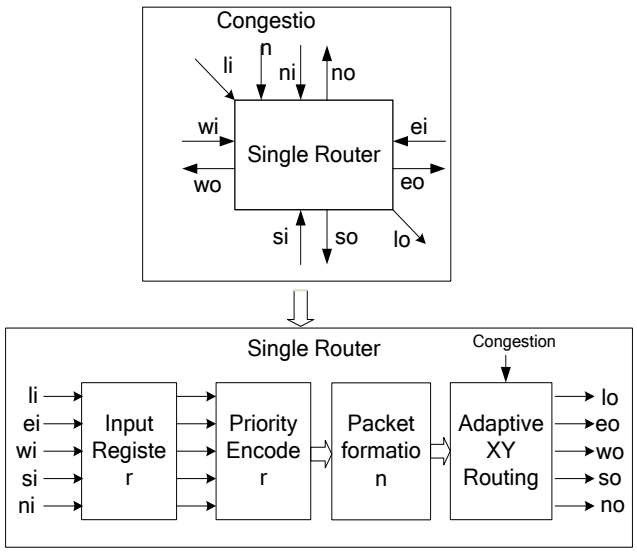

Fig.1 Proposed Block diagram of Single Router using Adaptive-XY Routing

The priority encoder has five inputs each 16-bits, they are drawn from input registers. The priority of each of these inputs (to the encoder) is decided by the prior select line. The prior choose line which is framed by using five input ports MSB bit

(15th Bit) to form is 5- bit signal. If the prior select line is 0, 1, 2, 3, and four then local input, east, west, south and north input data of the priority encoder will be selected respectively. The encoded packets are used in packet formation.

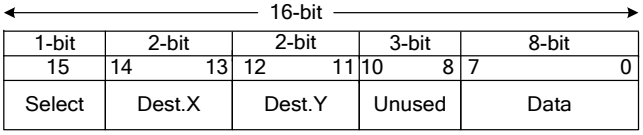

Fig.2 Packet formation

The packet formation of the proposed router is represented in figure 2, and it applies to any network topology format. The packet mainly contains mainly 8-bit data from any of the five different inputs (local, east, west, south, and north), 3-bit data unused data and used in future purpose. The 2-bit destination Y address followed by 2-bit destination X address and finally 1-bit select line provides the priority efficiently. The flit formation for 2x2, mesh network has a 16-bit packet - in that 8-bit [7:0] is port data, 3-bit [10:8] are unused data. More requests or acknowledge control signals can be accommodated in future. The 2-bit [12:11] for destination Y address, 2-bit [14:13] for destination X address and the 15th bit for the select line information of which, the five-port inputs has to perform the routing algorithm.

The NOC Routing computation is performed based on the topology which supports Routing algorithms Includes Normal XY routing, Dimension order, and Proposed Adaptive XY routing algorithms. In Normal XY routing, the packet is first to assist to X- direction until it reaches the same destination column and then supports to the Y- direction to reach its final destination. In Dimension order routing, the packets always move to the dimension with greater differences value of current and destination XY address. In the adaptive XY routing, it is the adaptive version of the normal XY routing. The 1st one dimension in X-direction and other in Y-direction with less number of routing nodes is confirmed then the packet is assisted to the dimension with less congestion. The routing algorithms are essential to reach the destination port without any congestion traffic from the source port. The three routing algorithms are designed which includes i) normal-XY Routing ii) Dimension Order Routing III) Adaptive Routing Algorithm is presented with flow diagram in below section.

A. Normal- XY Routing

In normal-XY routing algorithm, first forwards the packet to X- direction until it reaches the same column destination and then forward to Y- Direction to the final destination. The Normal XY Routing algorithm is designed based XY flow direction is as represented in following steps.

- For each router, the current X and Y address is defined by the user. If the user destination is same as packet destination then routing algorithm flows starts either in X or Y direction. The Difference X (Diff_X) is a difference between destination X address (Des_X) and current X address (Cur_X).
- Similarly, The Difference Y (Diff_Y) is a difference between destination Y address (Des_Y) and current Y address (Cur_Y). If both the Diff_X and Diff_Y is equal to zero. Then Local port will be selected.
- If Diff_Y is greater than zero, then south port else north port will be chosen.
- Otherwise, If Diff_X is greater than zero, then the east port else west port will be selected to route the packet information.

B. Dimension Order Routing

The dimension order routing effective operation includes, the packet is always forward to the dimension with greater difference value. The flow diagram of dimension order routing is represented in in following steps.

- First define the Current address for X (Cur_X) and Current address for Y (Cur_Y) of the router network and similarly set the destination address for X (Des_X) and destination address for Y (Des_Y). Find the dimension order.
- A greater difference (X_G), for Both X and Y directions. For X dimensions, The X_G is set, when Des_X is greater than Cur_X. For lower dimension order in X- direction (X_low) defined when the X_G is set to one; the Cur_X is selected otherwise Des_X. Similarly for higher dimension order in X- direction (X_High), when the X_G is set to one, the Des_X is chosen. Otherwise, Cur_X is higher order dimension. The difference value of X- dimension (Diff_X) is a difference between higher order dimension (X_High) and lower order dimension (X_low).
- Similarly for the dimension order greater difference (Y_G), for Y directions, The Y_G is set, when Des_Y is greater than Cur_Y. For lower dimension order in Y-direction (Y_low) defined when the Y_G is set to one; the Cur_Y is selected otherwise Des_Y. Similarly, for higher dimension order in Y- path (Y_High), When the Y_G is set to one, the Des_Y is chosen otherwise Cur_Y is higher order dimension. The difference value of Y- dimension (Diff_Y) is a difference between higher order dimension (Y_High) and lower order dimension (Y_low).
- If both the Diff_X and Diff_Y is equal to zero. Then Local port will be selected.
- If not, the Diff_X is greater than Diff_Y, and greater difference (X_G) is greater than zero, East port else west port will be selected.
- If the Diff_X is lesser than Diff_Y and greater difference (Y_G) is greater than zero, south port else north port will be chosen.

C. Adaptive-XY Routing

The adaptive XY routing is an adaptive form of the normal XY routing. The first dimension in X-flow and the second dimension in Y-flow with less number of routing nodes is performed then the packet is forwarded to the destination dimension with less congestion. The adaptive XY- Routing is

fully routed with less congested. The shortest route is the best one, which set alternative congestion free routing. The typical flow diagram of adaptive XY routing is represented in in following steps

- First define the Current address for X (Cur_X) and Current address for Y (Cur_Y) and similarly set the destination address for X (Des_X) and destination address for Y (Des_Y) of the router network.
- Set the congestion between the ports. Define the congestion (Cong) between alternative routing nodes with East versus south (E_S) set to zero, East versus north (E_N) set to one, west versus south (W_S) set to two and west versus north (W_N) set to three.
- The Diff_X is a difference between Des_X and Cur_X, and Similarly, Diff_Y is a difference between Des_Y and Cur_Y. If both the Diff_X and Diff_Y is equal to zero. Then Local port will be selected.
- If the Diff_X is greater than zero and Diff_Y is greater than zero, then Cong (E_S) is zero, the east port is selected, else south will be selected. If Cong (E_N) is one, the east port is selected, else north will be chosen.
- If the Diff_X is less than and Diff_Y is greater than zero, then Cong (W_S) is two, the west port is selected, and else south will be selected. If Cong (W_N) is three, the west port is selected, else north will be chosen.

The Physical implementation of 2X2 NOC Router using Mesh topology is represented in figure 3. Once router design is done individually for all four routing node, then instantiation for all the 4 routers into 2x2 NoC module. For all the routers R1-R14, local input and local output are the default and shown.

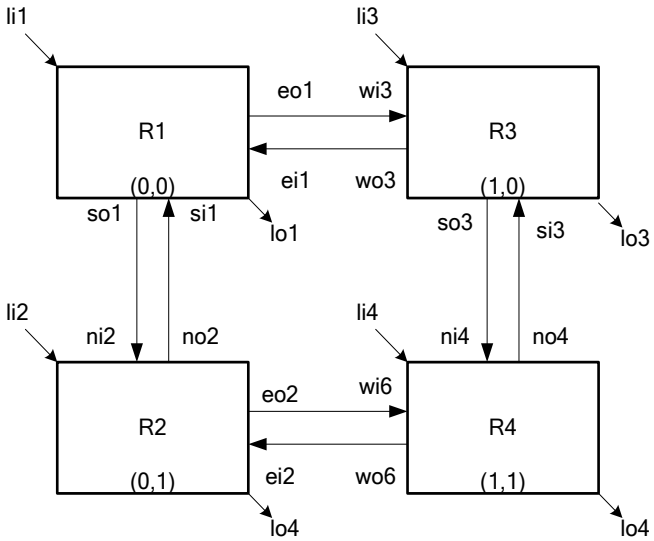

Fig.3 Hardware Implementation of Mesh 2X2 NOC

The Router (R1) is with local in (li1) and local output (lo1) and similar for Routers R2, R3, and R4. For each router, an identity of current address X and Y have to be fixed. For example, Router-1 (R1) the current address of X and Y is (0, 0) similarly For R4, Current XY address is (1, 1). R1 has 2-port input, default local input along with east input (ei1) which comes from west output (wo3) of R3 and south (si1) input comes from the north output of R2. Similarly, all the individual routers are interconnected, to form 2x2 NOC router. The 2-input ports are used in R1, R2, R3 and R4 router.

V. RESULTS AND ANALYSIS

The simulation results of the mesh 2x2 NOC is represented in figure 4. The 2x2 NOC design is based on the provided flit information with adaptive XY-Routing algorithm outputs. It contains the global clock, asynchronous reset, 5-bit congestion input, and four different 16-bit local inputs like pin1, pin2, pin3, and pin4. The outputs are four local packet outputs includes p_out1, p_out2, p_out3 and p_out4 output ports. Based on the adaptive-XY routing algorithm packets; they have processed in adaptive nature either X or Y direction. The packet (p_in1) is set to 16'h87aa as per packet format with congestion 5'd0, and the 8-bit local packet output 8'haa is generated after one and a half clock cycles. Similarly, other router inputs are performed with similar local packet outcomes.

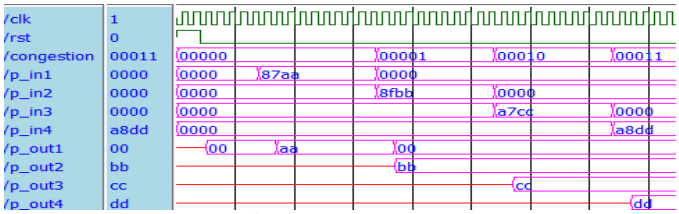

Fig.4 Simulation results of Mesh-2X2 NOC using Adaptive XY Routing

Once the design is synthesized on Xilinx platform, the chip area utilization is generated for a single router and 2x2 Mesh NOC with Proposed Adaptive XY routing (A-XY) over Normal XY (N-XY) and dimension order (DO) Routing. The Adaptive XY Routing consumes less amount of Slice Registers, LUT's and LUT-FF-Pairs than N-XY and DO-Routing as shown in table1. The A-XY routing for utilized less area overhead an average with 17 % for a single router and 16 % for mesh 2x2 NOC over N-XY and DO-Routing. The graphical representation is in the figure 5.

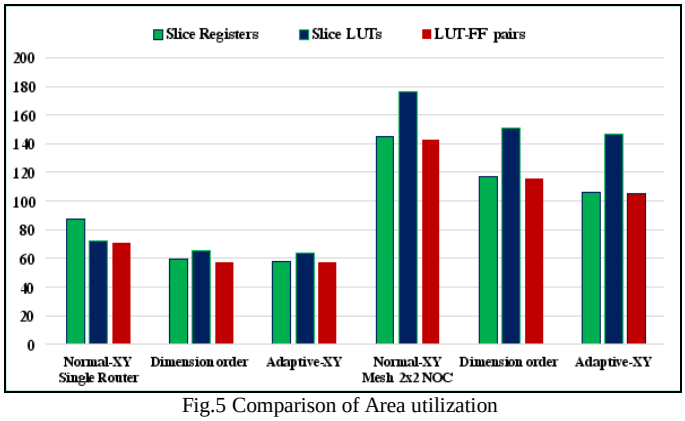

Fig.5 Comparison of Area utilization

The Adaptive XY Routing works at high frequency than N-XY and DO-Routing as shown in table 2. The Adaptive-XY routing for speed overhead improved with an average with 4 %

for a single router and 7 % for mesh 2x2 NOC over N-XY and DO-Routing.

Table.1 Area utilization of Single and 2X2 mesh NOC with different routing Algorithms

Area Utilization	Single Router			Mesh 2x2 NOC		
	N-XY	*DO*	*A-XY*	*N-XY*	*DO*	*A-XY*
Slice Registers	88	60	58	145	117	106
Slice LUTs	72	66	64	176	151	147
LUT-FF pairs	71	58	58	143	116	105

Table.2 operating frequencies of the Router and Mesh 2X2 NOC for different routing algorithms

Max. Frequency (MHz)	Single Router	Mesh 2x2 NOC
Normal-XY	597.086	564.079
Dimension order	602.555	541.126
Proposed Adaptive-XY	623.519	594.424

Once the design is implemented with place and route, after synthesis on Xilinx platform, the power utilization is generated using Xilinx X-Power analyzer tool. The clock frequency of the design is set to 100 MHz. The Adaptive XY Routing consumed less amount of total and dynamic power than N-XY and DO-Routing as shown in table 3 and represented in figure 6. The Adaptive-XY routing for utilized less power overhead an average with 10 % for a single router and 13 % for mesh 2x2 NOC over N-XY and DO-Routing.

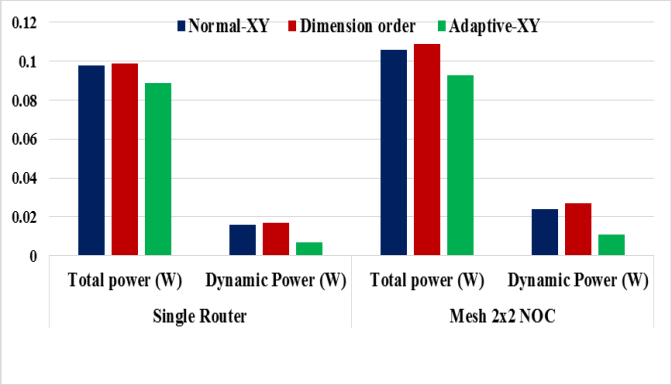

Fig.6 Power Analysis Comparison

Table.3 Power consumption of the Single Router and Mesh 2X2 NOC for different routing algorithms

Power Utilization (W)	Single Router		Mesh 2x2 NOC	
	Total power	*Dynamic Power*	*Total power*	*Dynamic Power*
Normal-XY	0.098	0.016	0.106	0.024
Dimension order	0.099	0.017	0.109	0.027
Adaptive-XY	0.089	0.007	0.093	0.011

VI. CONCLUSION

The NOC Routing Computation is performed based on topology along with Routing Algorithms. In this article, the design of efficient Router Architecture with Adaptive XY Routing algorithm is implemented, for the comparative analysis purpose, The Normal-XY and dimension Order Routing is designed. With the help of Router design, The Mesh 2x2 NOC Module is constructed using three routing algorithms. The efficient router consists of Input resisters, Priority encoder; Packet formation flowed by the Routing algorithms. By using Adaptive XY routing, a set of alternative routing is done, with congestion free best path. The performance of the proposed router and mesh 2x2 NOC using adaptive-XY routing over Normal-XY and Dimension order routing is analyzed. From the results, For single router using Adaptive -XY routing algorithm, consumed less area overhead with an average of 17 %, the speed overhead is improved with an average of 4 % and utilized less power overhead with an average of 10 % over N-XY and DO-Routing. For mesh 2x2 NOC using Adaptive -XY routing algorithm, employed less area overhead with an average of 16 %, the speed overhead is improved with an average of 7 % and utilized less power overhead with an average of 13 % over N-XY and DO-Routing.

In future, using the Proposed router with adaptive –XY routing, The fault-free routing and secure routing between Different secure IP Cores for NOC Based MPSOC is designed. The designs are verified with different traffic generation with various loads to analyze the latency and throughput.

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