Ku-band low noise amplifier design approach using HEMT device

Kamaljeet Singh[1], AV Nirmal[1] and Deepak Bhatnagar[2]
[1]*ISRO Satellite Center, Bangalore,*
[2]*Department of Physics, University of Rajasthan, Jaipur*

Abstract: This article details the design of low noise amplifier using HEMT which is potential unstable at Ku band. Instead of having standard approach of putting resistors at the input port (gate) or output port (drain side) to improve stability, resulting in the degradation of transistor gain and noise figure, an alternative approach of using bias resistor is presented in this article. Applying this approach on a single stage transistor, minimal degradation in noise figure without affecting the gain performance is achieved. Additionally, stability and matching of the transistor improves a lot using bias resistor. As single stage gain is not enough for the required application, so cascading of two stages using the above mentioned approach has been implemented to achieve desired specification. Dual stage analysis gives around 14 dB gain with a noise figure better than 2 dB at Ku-band. At Ku-band frequencies, major factor which governs the overall performances are parasitic encountered in assembly and non-accurate model parameters at the desired frequency range which results in frequency drift. Class A operation has been used with gate voltage of 2 V and drain current of 10 mA. The simulated input and output return loss is more than 10 dB at 17 GHz with noise figure of less than 2 dB. This article demonstrates simulation behavior with the resistor approach along with consideration of parasitics encountered due to ribbon bonding and using non-linear HEMT model. This way the results become more predictable taking the simulation near to the measured value. The adopted approach along with non-linear modeling of HEMT device is detailed in this article.

Keywords*: Low noise amplifier; noise figure; high electron mobility transistor (HEMT); resistor; non-linear modeling]*

I. INTRODUCTION

Low noise amplifier is the key component in front-end receiver, which dictates its dynamic range. This is achieved by low noise and high gain of the first stage of receiver i.e. low noise amplifier. The main consideration in design of low noise amplifier is the tradeoff between two important parameters namely noise figure and VSWR. Low noise amplifier design minimizes the noise figure of its active device by presenting an optimal source reflection coefficient '$\Gamma_{s,opt}$' while output is designed for flat gain and overall stability of the circuit. Standard technique such as inductance feedback, using resistor at gate or drain, parallel feedback [1,2] etc not only increases the circuit complexity due to incorporation of grounding using ribbon [3] but also compromises the input VSWR for getting desired noise figure. If the device is potentially unstable, the main consideration is to make device stable at the operating frequency which is generally done by incorporating a resistor which increases gain and noise figure. Further, it increases circuit complexity and needs extensive optimization. The present simulation study is carried out using high electron mobility transistor (CFY-67-08, Infineon) device. High electron mobility transistor is preferable as it has lower noise figure and higher gain due to high transition frequency f_T. Main requirement of designed low noise amplifier is power gain of more than 10 dB with noise figure 2 dB along with input and output matching better than 10 dB. The main application of targeted low noise amplifier is for telemetry and tele-command (TTC) application primarily for satellite communication.

II. CRITERIA OF NOISE FIGURE

An arbitrary source load, 'Γ_s ', device yields a noise figure given by:

$$F = F_{\min} + \frac{r_n}{g_s}\left|Y_s - Y_o\right|^2 \qquad (1)$$

where *Ys* ($= g_s + jb_s$) is the source admittance, *Yo* ($= g_o + jb_o$) is the source admittance for minimum noise figure and r_n ($= R_n / 50$) is the equivalent noise resistance usually provided with the noise parameters by the device manufacturer. The noise figure of linear two port amplifier can be formulated as a function of four parameters namely (i) F_{min}, the minimum noise figure of the device (ii) Γ_{opt}, the optimum source reflection coefficient for achieving F_{min}, (iii) R_n, the device noise resistance and (iv) Z_s, the actual source impedance applied to the input of the device. Three of these four parameters are fixed constants that are determined by the device characterization at a given frequency; therefore only one parameter can be modified to achieve the desired specifications. If $\Gamma_s = \Gamma_{s,opt}$, then above equation changes to $F = F_{min}$. Designing of low noise amplifiers with good input match is the main challenge as there is only one load impedance, Z_L that will provide a conjugate output match for a device terminated at the input for minimum noise. However Z_{in} is selected such that with Z_{opt}*(generally $Z_L \neq Z_{opt}$*) and mismatch occurs at the input port. Therefore a feedback mechanism or change of Z_{in} is required to make it closer to Z_{opt}* to have minimum noise figure with better matching. In present design, instead of employing standard inductive feedback, a lumped resistor in bias line is introduced. This alleviates problem of incorporating resistor or inductor at source (for stability) which has to be grounded

either using via (Printed through hole) or quarter wave-length open stub, eventually increasing circuit size and complexity. It also improves input matching without degrading overall gain.

III. NON LINEAR MODELLING

Modeling process includes three steps: Characterization, parameter extraction and modeling. Accuracy of any device model depends upon the accuracy by which the model parameters are determined. Data based approach (also known as measurement based) has been used having series of DC and S-parameter measurement has been performed over a large combination of gate and drain characteristics. The DC data of five transistors are measured (to take into account for device to device variation) which gives first order estimation of device performance characteristics. The major DC parameters effecting I-V curve are found out to be V_{TO}, Alpha(α),Beta(β),Rg and Rs. RF characterization and parameter extraction is done with the selection of equivalent circuit topology (in our case 'Materka') which is estimated using combination of DC parameter extraction and RF measurement. Large signal characterization is accomplished using either load pull or by large signal S-parameter extraction. This paper reports latter approach measuring gain compression, saturated power, efficiency and harmonic distortion of the sampler circuits like amplifiers and triplers. From the above measured values the AC parameters of the model namely Gamma(characterizing Vds dependence on the transconductance), Tau(characterizing transit time delay), Cds,Cgs have been optimized. The parasitics has been substituted by equivalent lumped elements to account for accurate characterization. Model is fine tuned in line with the measured data. The modeling used the lumped sparse bias approach along with the harmonic balance for circuit analysis. The parameters V_{TOAC}(zero bias threshold), C_{DSO} (output capacitance), $G_{AMMAXAC}$ (peak transconductance), were fine tuned to have steady state convergence[4] .

IV. ANALYSIS

Single stage of low noise amplifier is designed using high electron mobility transistor device [4]. As device is potentially unstable in the operating range, therefore to make it stable some feedback mechanism is required. In the present case, inductance (parasitic) due to leads of device as marked by dotted circle in Fig 1 makes a positive feedback path thus the stability of device increases. The value of inductance is modeled before incorporating in circuit simulator. Further to increase stability of proposed design, resistance in gate bias is introduced [5, 6] which gives dual advantage of high stability with improved matching. Both gate and drain bias circuits are connected closely to HEMT. This is done for keeping matching circuit away from bias circuit interference. Bias is adjusted to have Class A operation permitting nearly 10 mA current in the drain side. Bias circuitry uses radial stub due to its broadband characteristics and low insertion loss. Harmonic balance analysis is carried out [7] and it is observed that a single section is not enough to achieve the desired specification of high gain. To enhance gain of transistor, cascaded two stage design is carried out using the standard technique [8]. Figure 2 shows the cascaded two stage design of the proposed low noise amplifier at Ku-band. Same technique is again used in second stage and inter-stage matching concept is implemented to have higher power gain. Further input and output parasitic inductance (0.1 nH) which comes out due to assembly has been modeled and implemented in simulation.

V. SIMULATION RESULTS

Simulated results of above mentioned topology are shown in figure 3. The results achieved are as per specifications. Further there is minimal degradation in gain but resulting stability and return loss is much higher than achievable values using standard techniques. The observed input and output return loss is more than 14 dB, stability is around 2.4 with noise figure of 1.872 at 17 GHz, which shows that resistor incorporation has not compromised the circuit performance.

A low noise amplifier design using a HEMT device has been shown in this paper. Resistor incorporation in the gate bias circuit shows better stability and input match and high gain. Further it improves the stability of the transistor and makes it unconditionally stable. This alleviates the incorporation of input isolator which is traditionally used to improve input matching.

VI. CONCLUSION

Low noise amplifier is one of the critical components in front end design and at higher frequency the accurate prediction of the results is important due to associated losses. This article details the design approach to have good compromise between noise and gain performance at Ku-band along with the modeling approach.

ACKNOWLEDGMENTS

Authors are grateful to DD,SPA and Director, ISAC for their continuous support and encouragement.

VII. REFERENCES

[1] Inder Bahl and Prakash Bhartia, "Microwave Solid State circuit Design," Second Edition, Wiley Interscience

[2] D M Pozar *Microwave Engineering*, Second Edition, Wiley Interscience, 1990

[3] Y.Y Wei, P.Gale and E. Korolkiewicz, "Effects of grounding and bias circuit on the performance of high frequency linear amplifiers," Microwave Journal, Vol.46, No.2, Feb 2003, pp 98-106.

[4] Kamaljeet Singh & R. Ramsubramanian, "Simplified Non-Linear HEMT Modeling and Validation," CON-E3.1, Mathematical Techniques: Emerging Paradigms for Electronics and IT Industries (MATEIT-2006), Delhi-2006

[5] Y.Park, C.H Lee, J.D Creesler, and J.Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation," IEEE-MT Trans, Vol.54, April 2006, pp 1687-1697.

[6] Z. Yang, T. Yang, J. Xie and R . Xu, "The design of a Ka-Band Monolithic Low Noise Amplifier," Asia-Pacific Microwave Conference-China 2005, VolII, pp904-906.

[7] Advanced Design System, Agilent Technologies

[8] Gullimero Gonzalea, "*Microwave Transistor Amplifiers Analysis and Design*," Prentice Hall, New Jersey 1984

Dr Kamaljeet Singh has obtained M. Tech (Microwaves) from Delhi University in 1999 and awarded PhD in 2010.He worked in the area of Geo- receiver at C-band and initiated developments of various RF components. He was posted in 2006 to Semi-conductor Laboratory, Near Chandiagrh in 2006 where he worked in the area of RF-MEMS. Initiated development of various sensors and productionized physical sensors along with re-establishment of 6" MEMS fabline . Presently working at ISRO Satellite centre and involved in product ionization of S-band TT &C transponders. He is fellow of IETE, Life member of ASI & Punjab Academy of sciences and member of IEEE. He has published more than 80 articles in various journals/conferences and reviewer of many journals. He is recipient of young scientist awards from INAE,IETE & ISRO. His book titled *'RF principle and its application in RF-MEMS switch* 'is under publication. A patent is also filed on liquid level sensor using MEMS technology.

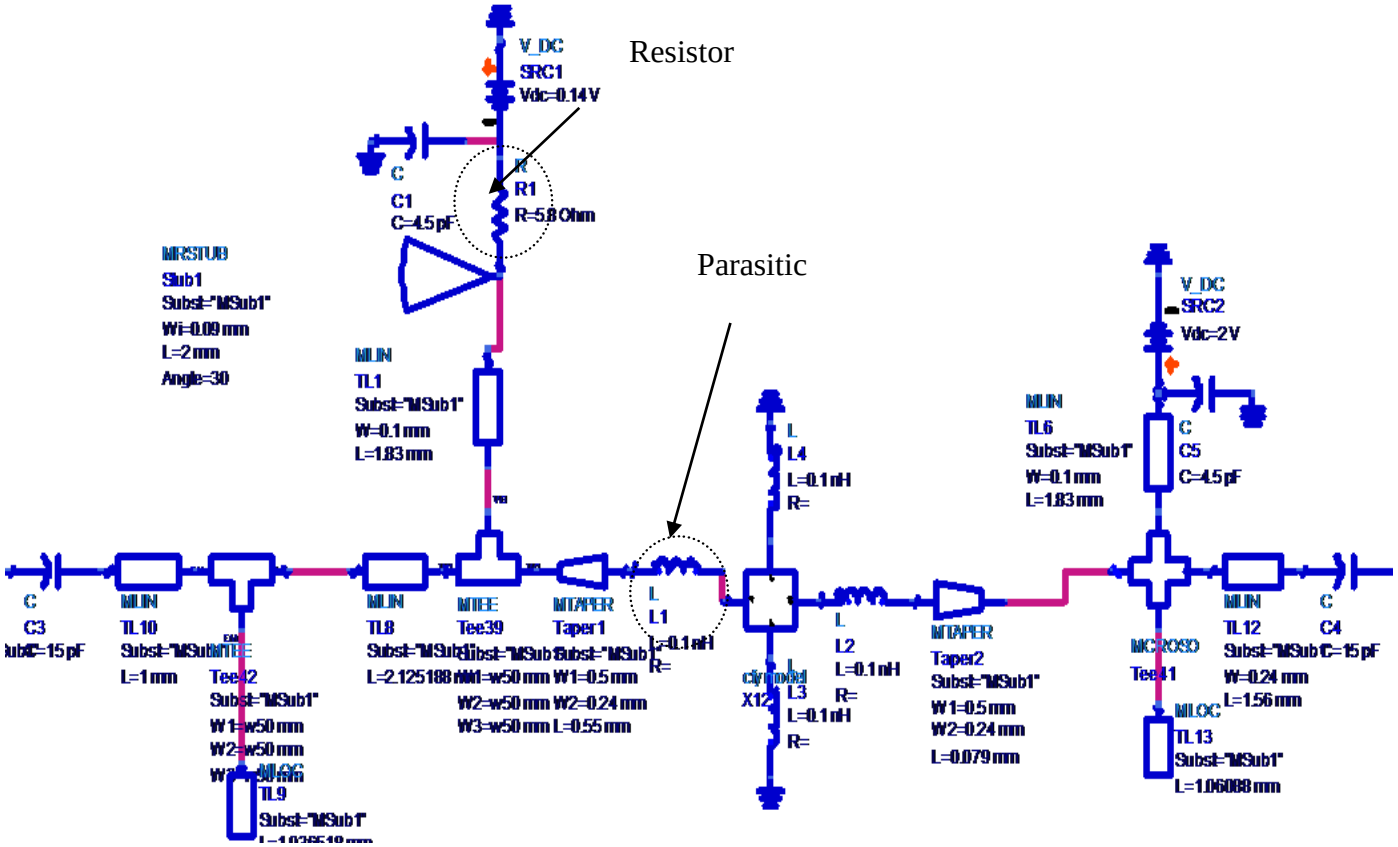

Fig.1: Circuit schematic of single stage low noise amplifier

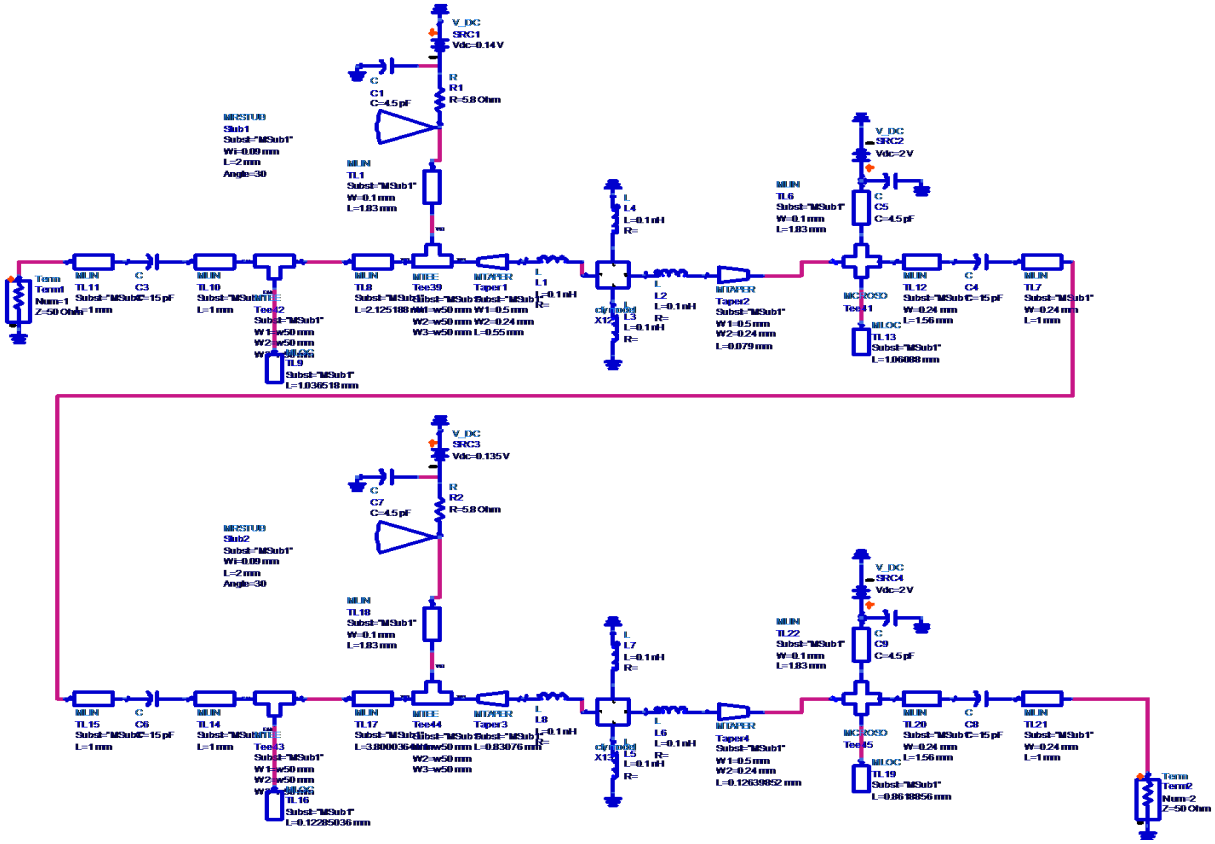

Fig.2: Circuit schematic of cascaded low noise amplifier

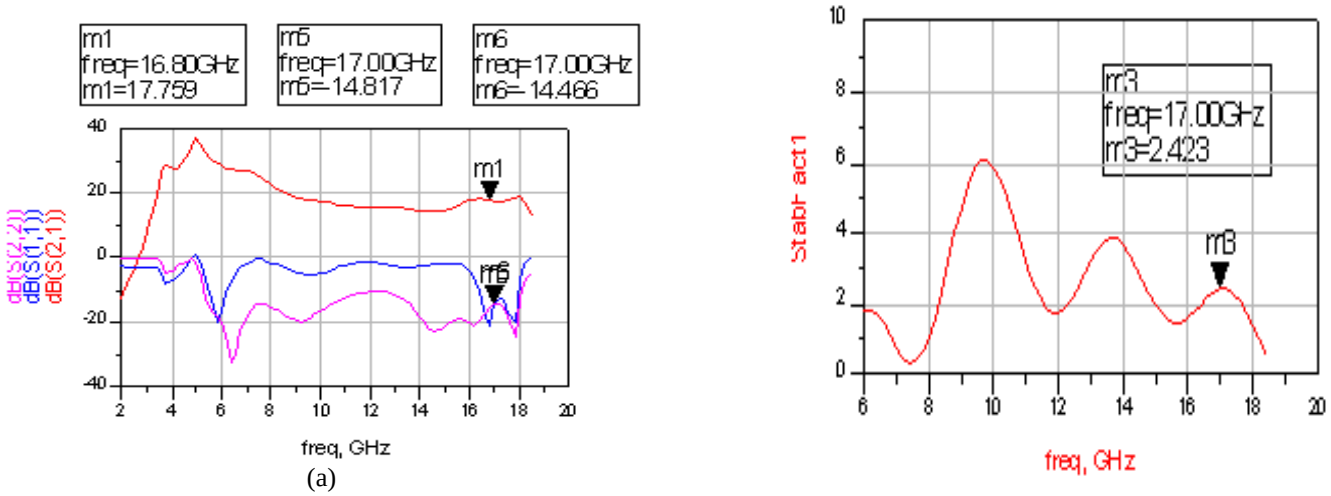

Fig.3: Simulated gain, two stages low noise amplifier