Optimization of SRAM Cell using FINFET Technology in 32nm

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Abstract- In this paper, a different configurations of SRAM cells are designed and implemented using FINFET technology to improve their power and speed. A 2 bit and 4 bit SRAM is also implemented. Also a comparative study for various performance parameters like average power and delay is also presented in this paper. It can be concluded that the FINFET technology can effectively reduce power and current of logic gates. Hence it can be used in number of portable electronics devices applications which requires limited amount of power.

Keywords- FinFET, SRAM, 32nm

I. INTRODUCTION

Mass CMOS advancements have been the foundation of semiconductor gadgets for a considerable length of time. Moore's law rouses the innovation scaling to enhance the execution highlights, for example, speed, control utilization and zone. [1][2]While circuit and frameworks take the upsides of unavoidable downsizing the innovation, the impact of undesired highlights, for example, short channel effects (SCEs) and affectability to process varieties has been expanded. CMOS circuits are furthermore straightforward and modest to make yet the constant scaling of conventional mass CMOS transistor has put outrageous containments on additionally scaling. [7][4]Scaling of MOS ends up being widely troublesome for innovation underneath 32 nm, where the proximity of source and drain cut downs the control of the entryway. [3][5]

Noteworthy diminishment in control utilization (half more than 32nm) in FINFET over MOSFET and a Faster exchanging speed also there is Effective speed/control exchange off is conceivable with multi-Vt in FINFET. [7] Despite the fact that the advantages are extraordinary, the main disadvantage is self-warming. [2] Furthermore, it is said that there will be there are two noteworthy contenders for the new transistor design: FINFETs and completely drained silicon-on-cover. We can state that the time has touched base to begin investigating the design exchange offs did conceivable by change to FinFETs. [10]

II. PROPOSED SRAM DESIGN USING FINFET

A new device can replace bulk CMOS because of the numerous advantages it offers over bulk CMOS. Along these lines, FinFET SRAM comes as the other option to substitute Si-bulk SRAM. FinFET because of two gates have better control over OFF current is used in memory array.In present scenario, memories occupies a huge part of SOC and mobile applications.[3] However, design of SRAM became more challenging in deep technology. We have leakage mainly from big memory arrays in idle state and it is because of the process variations of the device and SECs.The Si bulk CMOS in deep nanometer is no longer stable and also not able to meet the design standards. Stability and leakage power are more significant factors in deep scaling. [9]In this paper FinFET devices schemes are assessed and compared. Also, different types of FinFET SRAM schemes are evaluated and compared. It's ended that none of the evaluated devices and SRAM schemes will optimize all parameters along. There is always an exchange among power, performance, and stability which makes the cell style more difficult and a lot of sophisticating.

The simulations were performed on HSPICE Synopsys software tool on 6T, 8T and 10T SRAM cell. Using SRAM 10T cell a 2 bit SRAM and 4 Bit SRAM is designed. 6T SRAM cell is most broadly utilized as a part of installed memory due to its quick access time and generally little region. 6T cell configuration includes complex tradeoffs between different factors to be specific limiting cell region, great delicate blunder invulnerability, high cell read present, low spillage present, great cell security with least voltage and least word line.[3]The full CMOS 6T SRAM bit cell configuration is shown in Fig1.

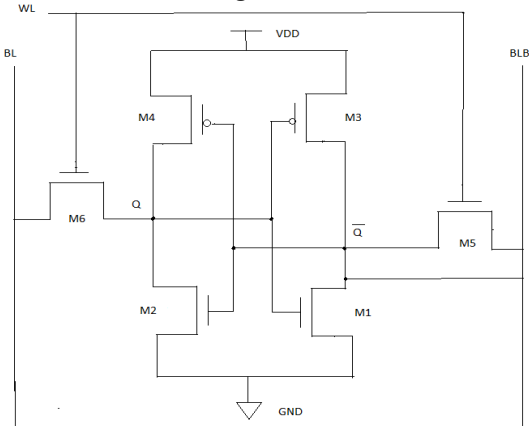

Fig.1: SRAM 6T

The schematic diagram of 8T SRAM cell is shown in Fig 2. Due to the stability limitations of 6T SRAM cell at low supply voltages, 8T SRAM is suitable for multimedia applications [4]. New signals here are RBL and RWL which improve power consumption.

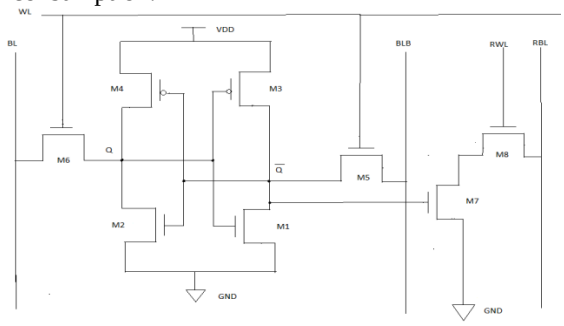

Fig.2: SRAM 8T

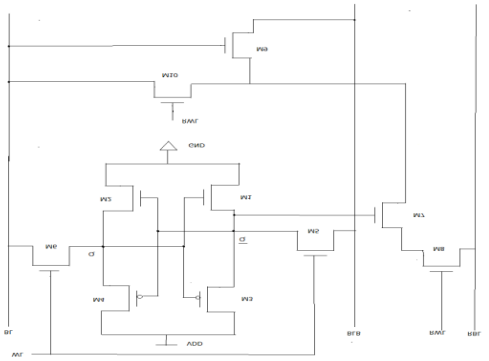

Fig.3: 10T SRAM cell

The proposed 10T SRAM bit cell is shown in Fig. 3. It contains 10 transistors. M1-M3 and M2-M4 form a pair of cross coupled inverters. M5 & M6 are access transistors; M7 & M8 constitute a separate path for read operation. M9 & M10 act as switches to conditionally connect the read path to any one of the write bit lines depending upon the last written data.[4]Figure 4, Figure 5 and Figure 6 represent the SRAM cell for 6T, 8T and 10T using FinFET in short gate mode.

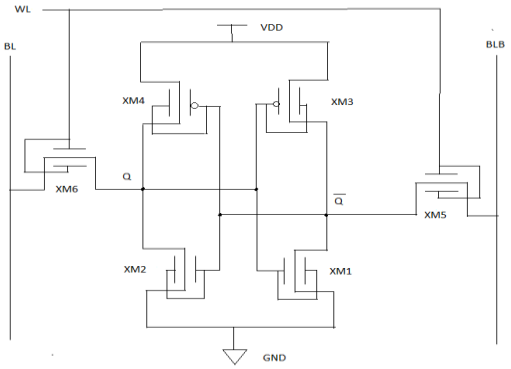

Fig.4: 6T SRAM FinFET

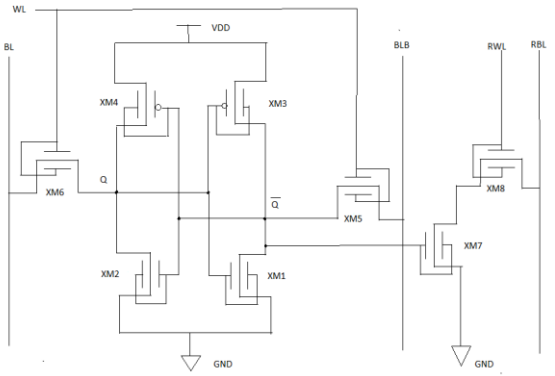

Fig.5: 8T SRAM FinFET

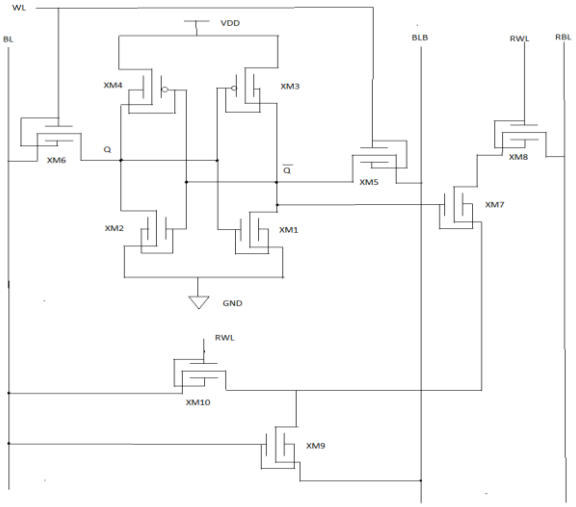

Fig.6: 10T SRAM FinFET

Figure 7 and 8 represent circuits of MOSFET base 2 bit and 4 bit SRAM using the 10T configuration.

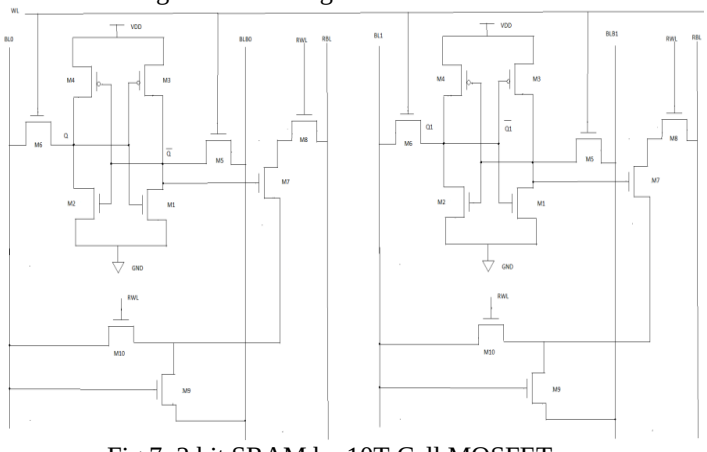

Fig.7: 2 bit SRAM by 10T Cell MOSFET

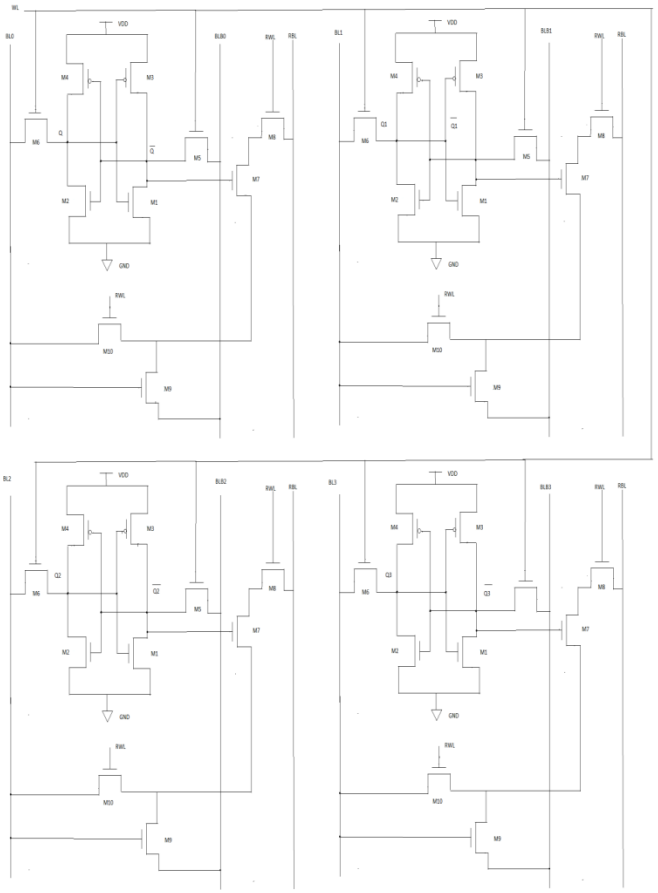

Fig.8: 4 bit SRAM by 10T Cell FinFET

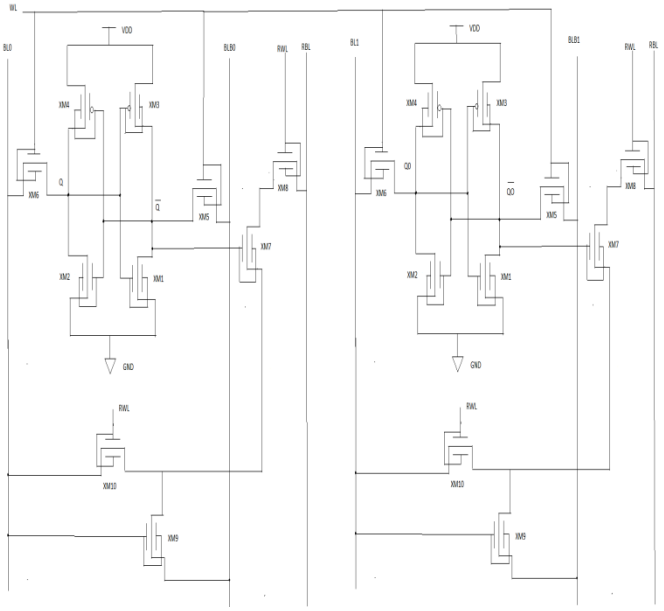

Fig.9: 2 bit SRAM by 10T Cell FinFET

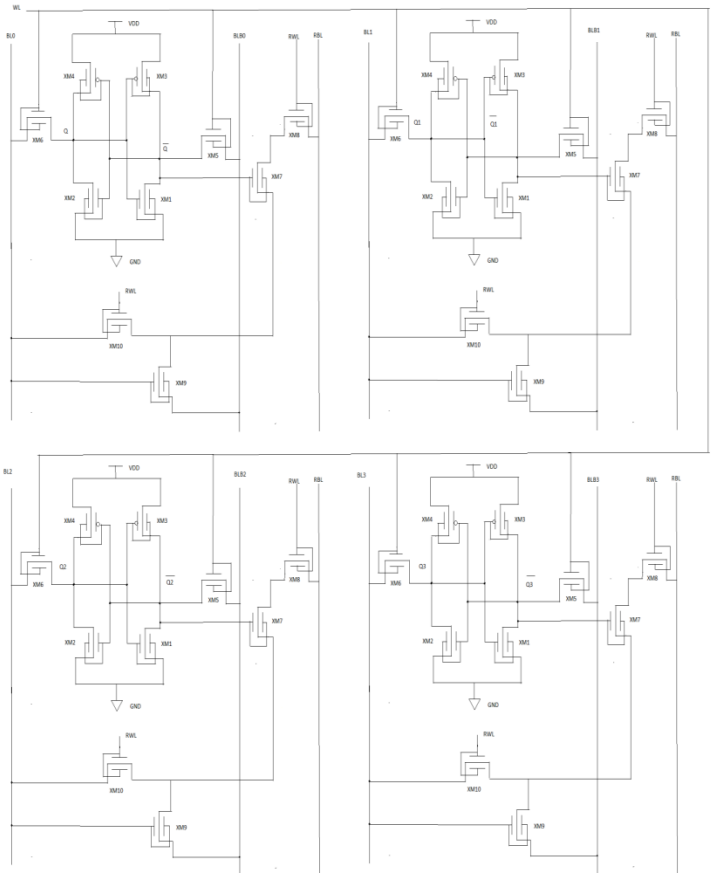

Fig.10: 4 bit SRAM by 10T Cell FinFET

III. SIMULATION RESULTS AND ANALYSIS

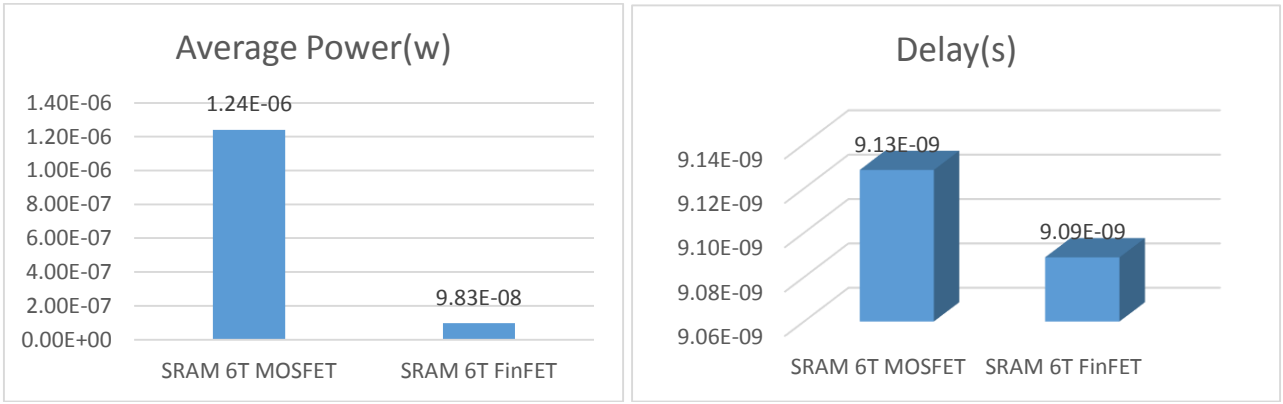

Fig.11: Comparison of SRAM 6T MOSFET with FinFET

Figure 11 shows average power and delay comparison for SRAM 6T in MOS and Fin Technology.
Figure 12 shows average power and delay comparison for SRAM 8T in MOS and Fin Technology and similarly for Figure 13 in SRAM 10T.

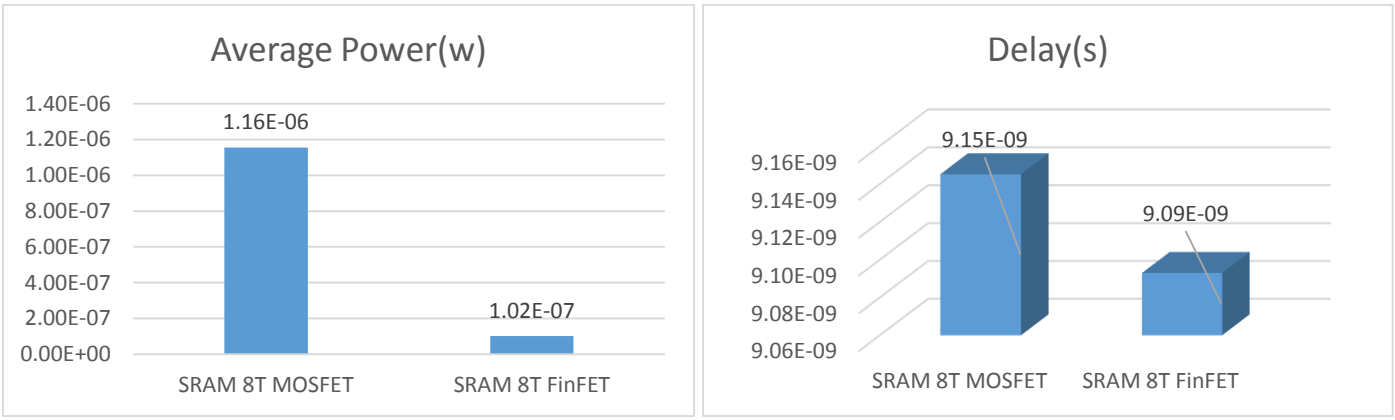

Fig.12: Comparison of SRAM 8T MOSFET with FinFET

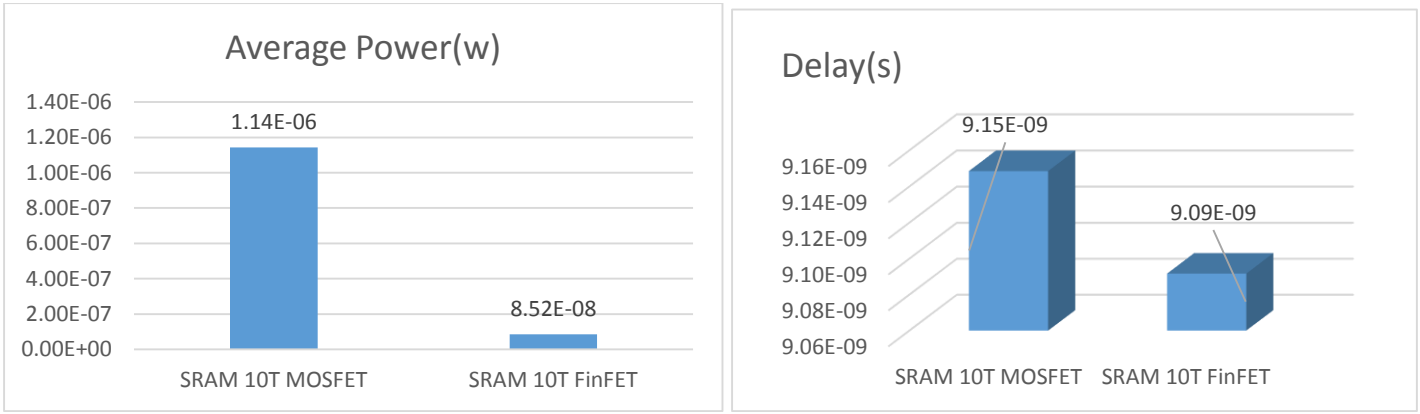

Fig.13: Comparison of SRAM 10T MOSFET with FinFET

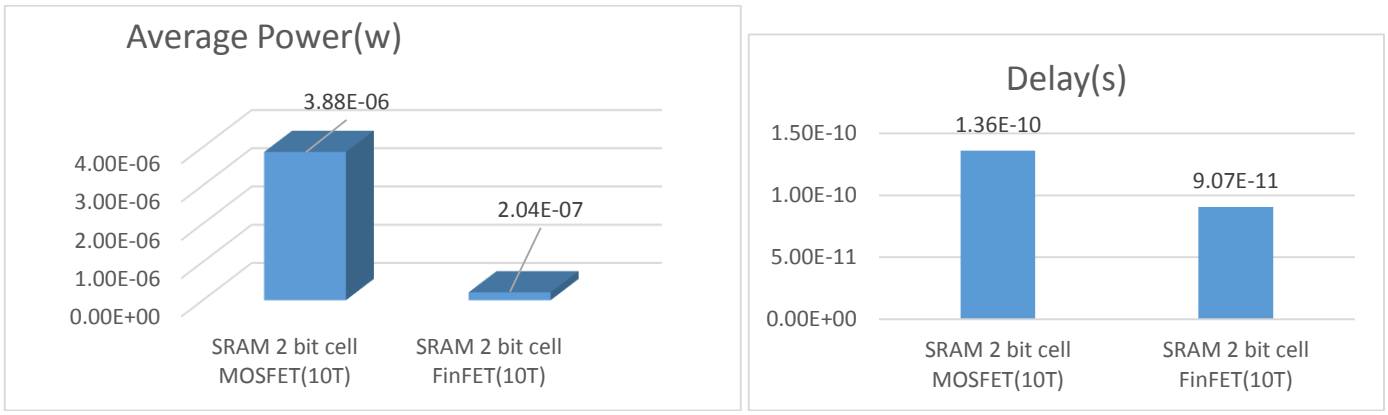

Fig.14: Comparison of 2 bit SRAM (10T) MOSFET with FinFET

Figure 14 and 15 shows Average Power consumption and delay of SRAM 10T in 2 bit and 4 bit SRAM respectively.

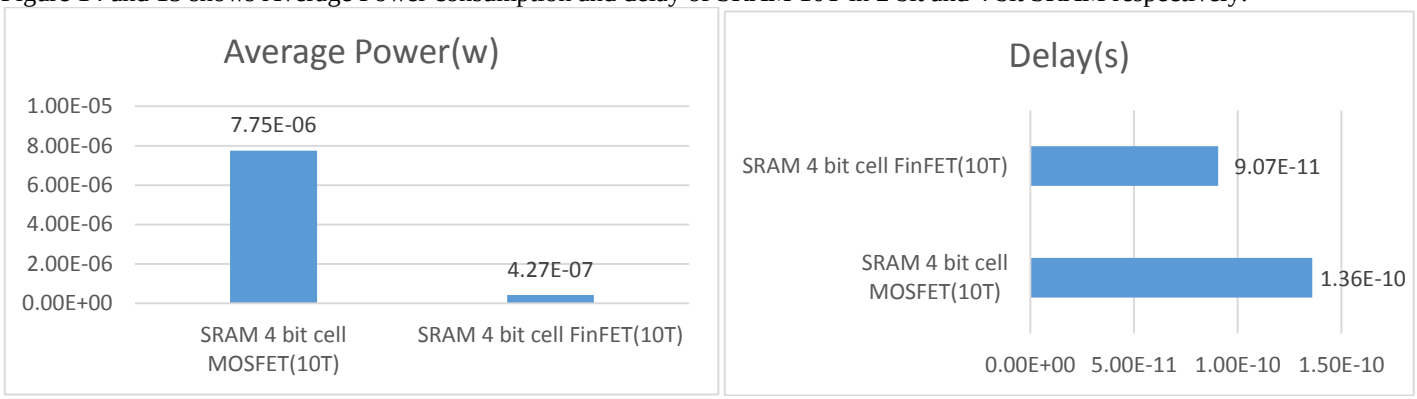

Fig.15: Comparison of 4 bit SRAM (10T) MOSFET with FinFET

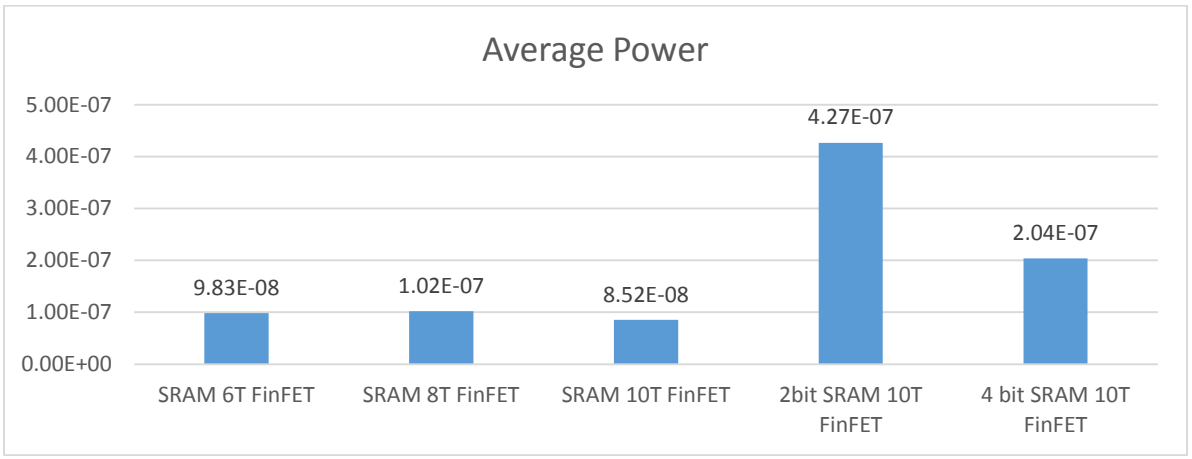

Fig.16: Average Power Consumption for all circuits in FinFET

Figure 16 chart shows comparison Average Power Consumption of all circuits using FinFET and Figure 17 shows for MOSFET circuits.

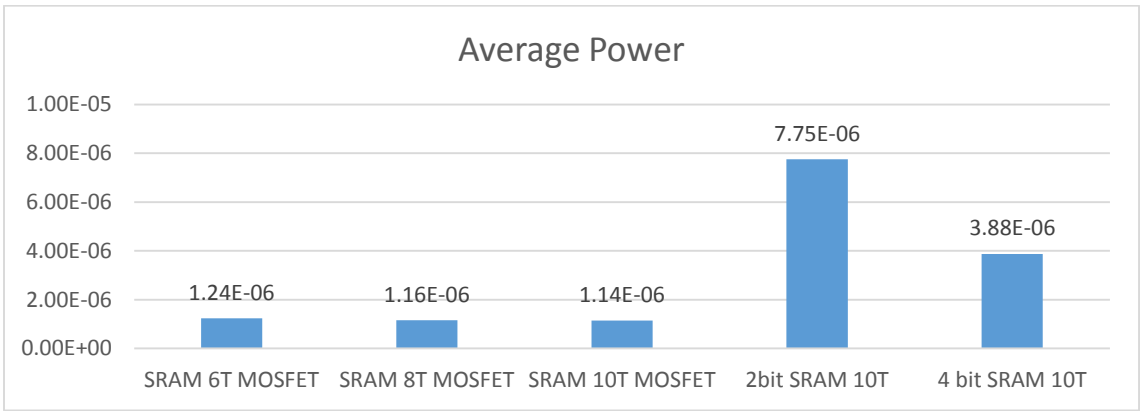

Fig.17: Average Power Consumption for all circuits in MOSFET

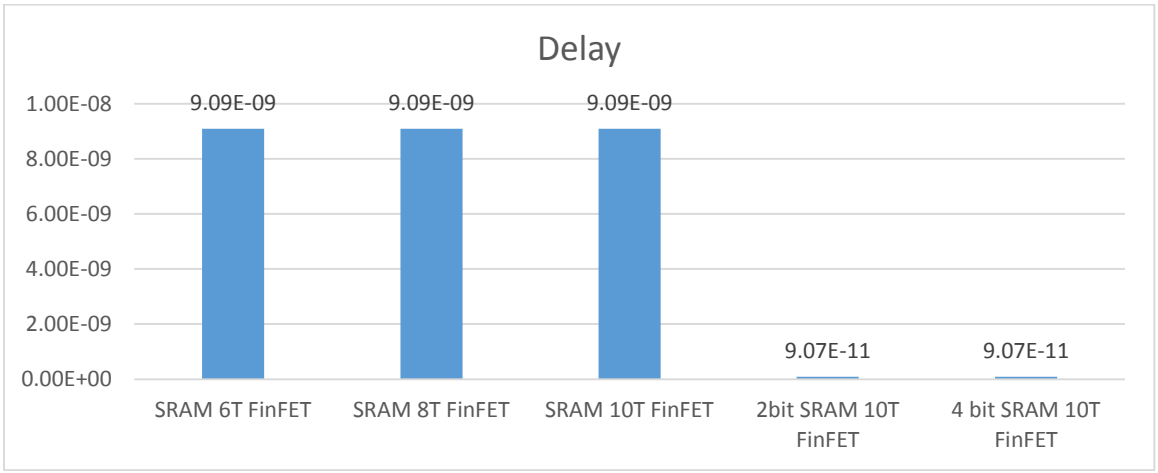

Fig.18: Delay for all circuits in FinFET

Figure 18 and 19 represent the delay of all circuits using MOSFET and FinFET.

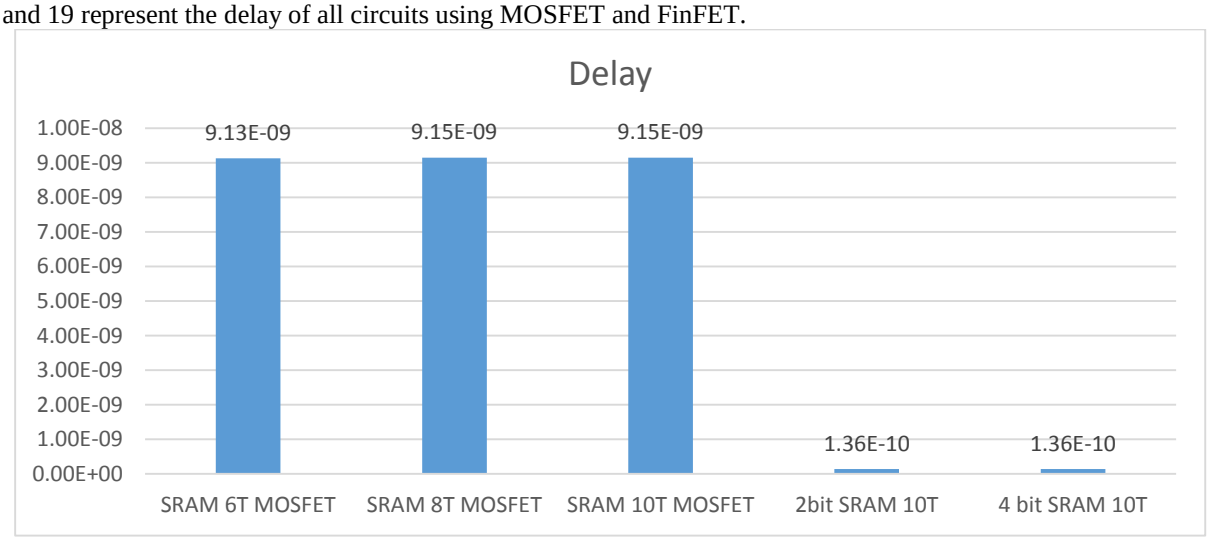

Fig.19: Delay for all circuits in MOSFET

In table 1, all data for Average power and Delay in all MOSFET and FinFET based circuits are mentioned in tabular form.

Table 1: Average Power Consumption and Delay for all circuits

	SRAM 6T MOSFET	SRAM 6T FinFET
Average Power(w)	1.24E-06	9.83E-08
Delay(s)	9.13E-09	9.09E-09
	SRAM 8T MOSFET	SRAM 8T FinFET
Average Power(w)	1.16E-06	1.02E-07
Delay(s)	9.15E-09	9.09E-09
	SRAM 10T MOSFET	SRAM 10T FinFET
Average Power(w)	1.14E-06	8.52E-08
Delay(s)	9.15E-09	9.09E-09
	SRAM 2 bit cell MOSFET (6T)	SRAM 2 bit cell FinFET (6T)
Average Power(w)	4.03E-06	2.81E-07
Delay(s)	1.31E-10	9.10E-11
	SRAM 4 bit cell MOSFET (6T)	SRAM 4 bit cell FinFET (6T)
Average Power(w)	8.06E-06	5.69E-07
Delay(s)	1.31E-10	9.10E-11
	SRAM 4 bit cell MOSFET(10T)	SRAM 4 bit cell FinFET(10T)
Average Power(w)	7.75E-06	4.27E-07
Delay(s)	1.36E-10	9.07E-11
	SRAM 2 bit cell MOSFET(10T)	SRAM 2 bit cell FinFET(10T)
Average Power(w)	3.88E-06	2.04E-07
Delay(s)	1.36E-10	9.07E-11

IV. CONCLUSION

Simulation results show that 10T SRAM in 2 bit and 4 bit mode have improved speed and a lower consumption of average power. The average power and delay is improved by 94.7 % and 33% respectively for 2 bit SRAM 10T MOSFET and FinFET. For 4 bit SRAM 10T, the FinFET SRAM 4 bit is improved by 99.4 in Average Power and in Delay it is improved by 33.8%.With FinFET Technology we can accomplish low power and decreased short channel effects so the FinFET based SRAM can be utilized as a part of low power VLSI applications. In view of the utilization of FinFET innovation we can decrease the postponement altogether so this FinFET based SRAM can be utilized as a part of planning recollections with no short channel effects beneath 32nm and furthermore in fast applications proficiently.

V. REFERENCES

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