Design and Analysis of Phase Frequency Detector for Digital PLL

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ABSTRACT
This paper presents design and analysis of various PFD designs for Low Phase Noise Digital PLL. The most common application is generating a higher speed on-chip clock than is practical or power-efficient for off-chip distribution. PLLs are also used to reduce the input clock to- data output delay of ICs—the PLL advances the on-chip clock so that delayed output data signals are re-aligned with the input clock edges. A delay-locked loop (DLL) is sometimes used for this purpose too. Often, PLLs are almost literally the heart of an IC, and faults in the PLL can impact many or most performances of the IC. The simulations are carried out for Phase Frequency Detector in 0.18um TSMC and 90nm generic technology. PFD is simulated using different gates like AND gate, NOR Gate and NAND gate. Also implement modified PFD using D Flip-Flop. Different Charge Pump Circuits are simulated and one of them taken to combine with PFD block. Also integrate three blocks PFD, Charge Pump and Loop Filter and take results of them. Implement Current-Starved VCO and simulate it.

Keywords:
Phase Locked Loop, Delay-Locked Loop (DLL), Voltage Controlled Oscillator (VCO), Low-Pass Filter (LPF), Phase Frequency Detector (PFD

I. INTRODUCTION

Mostly digitally synchronous ASIC plans necessitate clock source to provide timing reference for information signals which are transferred among functional blocks in the design. That clock source will be determined from an on-chip crystal oscillator for comparatively small and simple ASIC circuit designs. Commonly crystal oscillators and crystals can achieve up to 30 MHz without too much trouble. PLL is a useful circuit for ASIC designers, which gives time flexibility to them. An order of magnitude, cancel out clock distribution delays, adjust setup and hold times, correct clock duty cycles and minimize clock skew all that parameters are multiplied an inexpensive low-frequency crystal by PLL. Although what is inside a PLL circuit is high-speed digital circuitry, the gluttons of the PLL include analog circuits that require understanding for placement within the ASIC floor plan. Phase Locked Loop is one of extensively used circuits for fast clocks in digital circuits. Predictably PLL was made using analog building block. Using a PLL in a digital noisy System on Chip that affects environmentally complicated integrating and interfacing issues. Recent CMOS processes in nanometer scale which offers constrained voltage gap and poor analog extensions, proved to be inadequate for integration of practical analog & digital functions.

DCO dominates significant performances of PLL, for example, consumption of power and dissipation, jitter noise and hence is critical factor like clocking circuits. Since DCO inhabits more than 50% consumption of power in PLL, power consumption of DCO should be reduced for save overall power dissipation to meet requirement of low power requirements in SoC designs.

Phase Locked Loop is feedback circuit that gives comparative results of its phase of an incoming reference signal with output phase and adjusts itself until both are coordinate, i.e., the PLL output's phase is "locked" to that of the input reference. Once the phase difference between the output and the input signals is very close to zero means the loop is locked then the frequency of the output signal is a multiple (integer or fractional) times of the frequency of input signal.

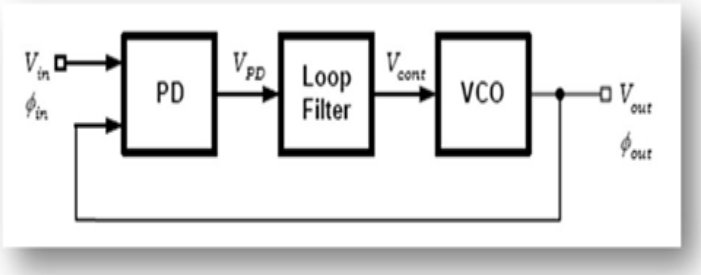

Figure 1. The block diagram of a general PLL

Some major modules for PLL are oscillator, which must be simulated as analog component for perfect evaluations of its performance. Simulating PLL is more difficult than simulating

an oscillator due to absence of nonlinear close loops. Simple block diagram of general PLL as shown in Fig. 1, which isolated into phase detector, loop filter, oscillator and frequency divider. Design procedure used for this digitally controlled PLL is to transform the components. The reference scale current is generated based on PLL control that specifics certain PLL characteristics such as loop damping and loop bandwidth. So, reference current can be competently optimized for changing PLL operating conditions, in addition to compensating for variable VCO gain.

Now days in high speed data communication world PLL is mostly and extensively used. So, in current year, low jitter for PLL designing for different application has become one of extreme challenges in high performance very large scale integration design. For numerous applications like clock-data recovery and synthesizing frequency Phase-Locked Loop (PLL) produces appropriate on-chip clocks. Elementary perception locking of phase has persisted the same since its invention in the 1930s. However, design and application of PLLs continue to be interesting as design requirements of a PLL such as clock timing uncertainty, power consumption and area becomes more stringent. PLL also multiplies a low frequency reference clock, to produce high frequency o/p clock. As the name infers, persistence of PLL is to produce signal in which the phase is the same as the phase of a reference signal, this is recognized as the lock mode. Afterward this process, PLL continues to equate two signals but since they are in lock mode, the PLL output is persistent.

II. EXISTING ARCHITECTURES OF PLL

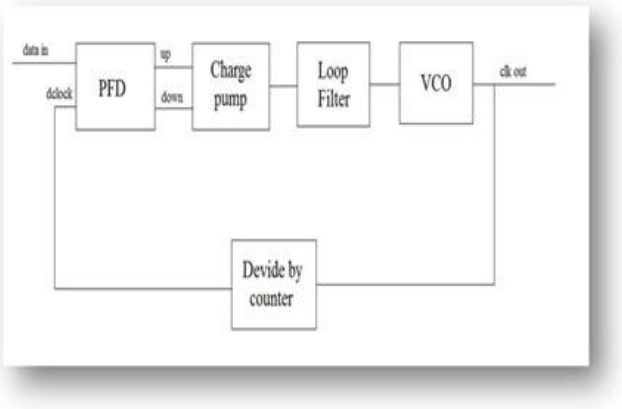

Figure 2. A Basic Block Diagram of Phase Locked Loop

An error generated by PFD based on phase differences between phase of i/p reference data in and feedback clock as shown in figure 2. If nearby difference of phase appeared between two signals, it produces an error signal. This error signal drives the low pass filter, which increases or decreases the control voltage. VCO is receive controlled voltage as the input. In figure 3 diagram of PFD is shown. O/p of the PFD depends on both phase as well as frequency of the inputs. That type of phase detector is known as sequential detector. PFD is digital circuit which detects phase or frequency difference between reference clock and voltage controlled oscillator (VCO) clock / feedback signal and generates output signal with increasing and decreasing frequency of VCO. At reset input a high signal will force Q low as reset signal is applied. Lastly, a rationally high on both output causes resetting of both FFs. Output signal depends not only on the phase error but correspondingly on frequency error.

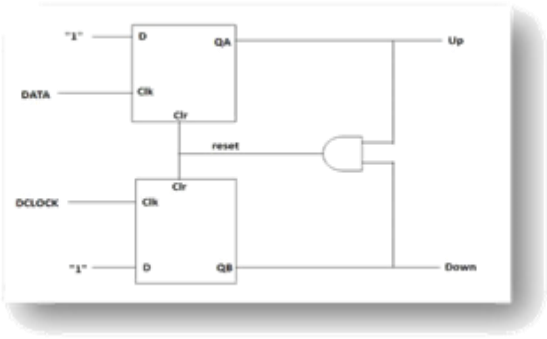

Figure 3. A Basic Block Diagram of Phase Frequency Detector

III. PHASE FREQUENCY DETECTOR

The first block of PLL which is Phase Frequency Detector. This design represents High-Speed PFD application. The main objective is to implement the circuit using 1GHz clock frequency. The architectures of the PFD have been implemented using 0.18µm CMOS technology using power supply 1.8V and 90 nm generic technology using power supply 1V.

3.1 Phase Frequency Detector Using AND Gate

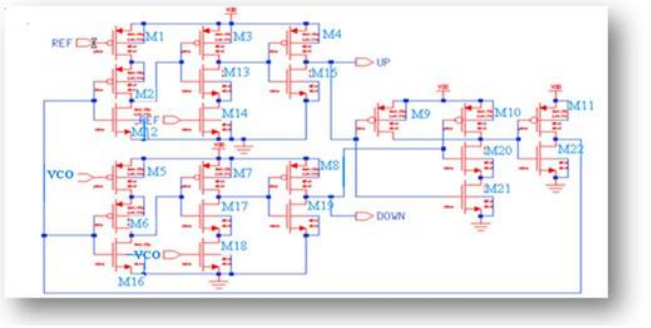

Figure 4. PFD using AND GATE schematic

It is implemented by two D-FF and an AND logic gate. Each D-FF has eight CMOS transistors and the AND gate has got six

ones. So, this design consists of 22 transistors. The implementation is using CMOS 180nm technology as shown in figure 4.

3.2 Phase Frequency Detector Using NOR Gate

In NOR gate based PFD, the reset path is changed using nor gate, as shown in the figure 5. There is NOR gate in the reset path, so it contains less transistor as compared to and gate in the reset path so dead zone less also reduce jitter.

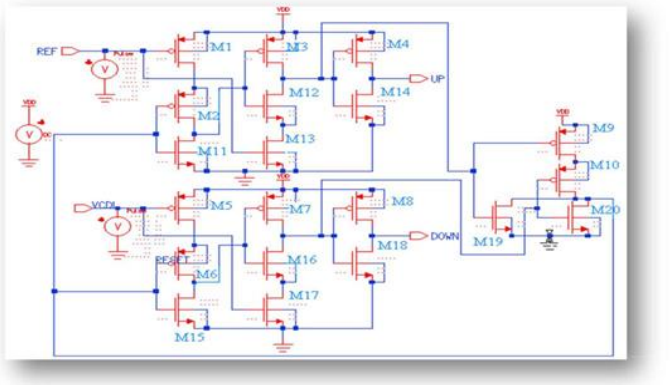

Figure 5. PFD using NOR GATE schematic

3.3 Phase Frequency Detector Using NAND Gate

The basic Phase Frequency Detector is composed by two D-FF and a NAND logic gate. In this circuit, there are two resettable and edge triggered D flip flops with their D inputs tied to logic 1 and a NAND Gate at the reset path. First, the UP and DOWN signals are reset too low. In addition, the data frequency waveform is slightly leading form the d clock waveform. When a falling edge occurs on the data input, the high signal on the D input is transmitted to the Q output.

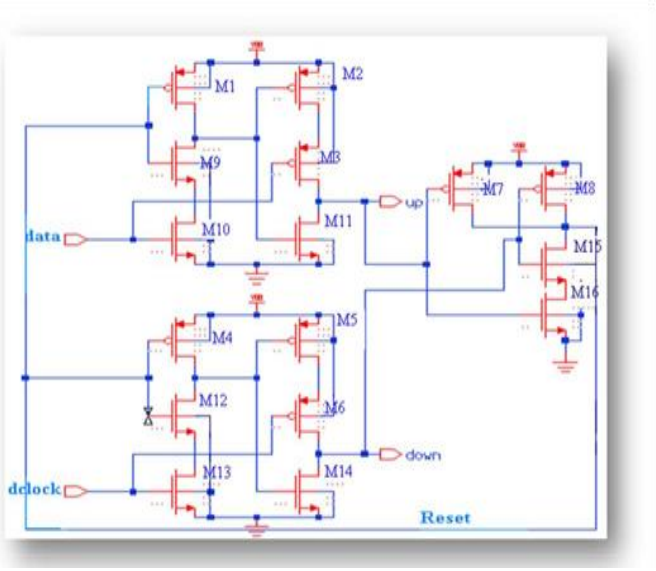

Figure 6. PFD using NAND GATE Schematic

3.4 Modified Phase Frequency Detector

The reset path is modified in the design of Modified PFD. The input signals are straight connected to reset signal of another D flip flop as shown in the figure 7. NOR gate at reset path is used to eliminate and therefore dead zone is removed. With the modified circuit of D flip flop, the reset time is reduced and therefore the jitter is reduced.

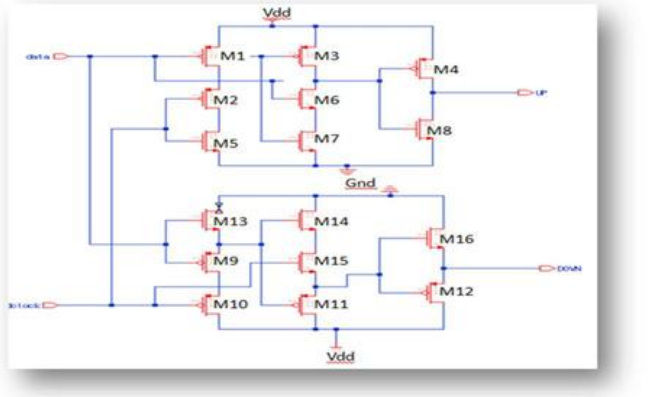

Figure 7. Modified PFD schematic

IV. SIMULATION RESULT

4.1 Simulation Results of Phase Frequency Detector Using AND Gate

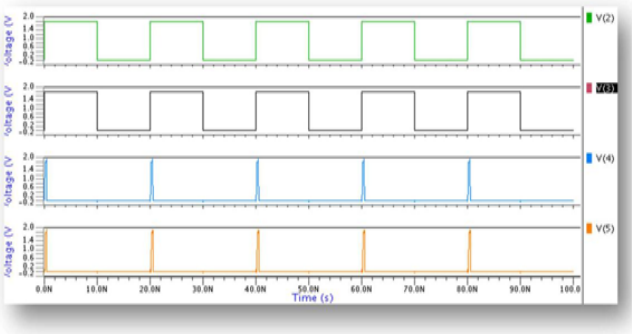

Figure 8. Basic PFD using AND GATE (Lock Condition) 0.18 µm

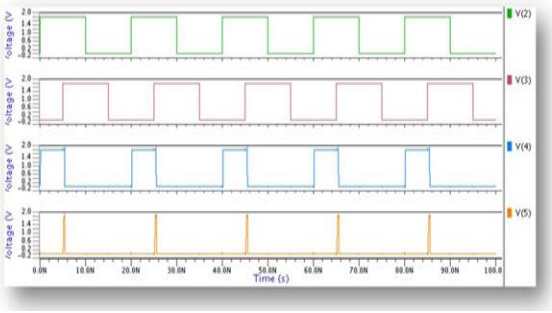

Figure 9. PFD using AND GATE (CLK Leading Condition) 0.18 µm

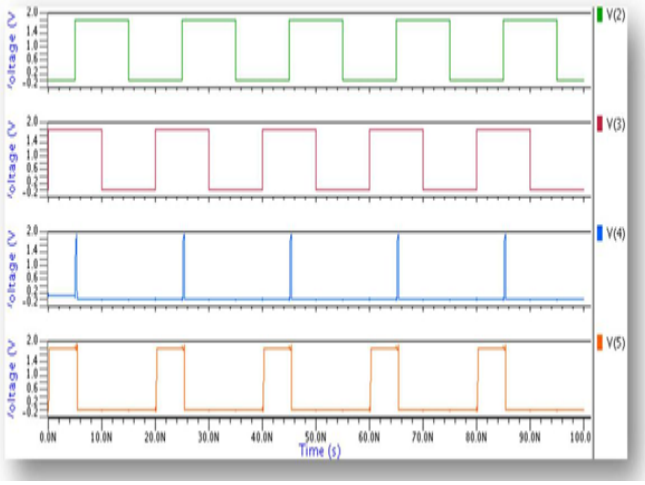

Figure 10. Basic PFD using AND GATE (CLK Lagging Condition) 0.18 µm

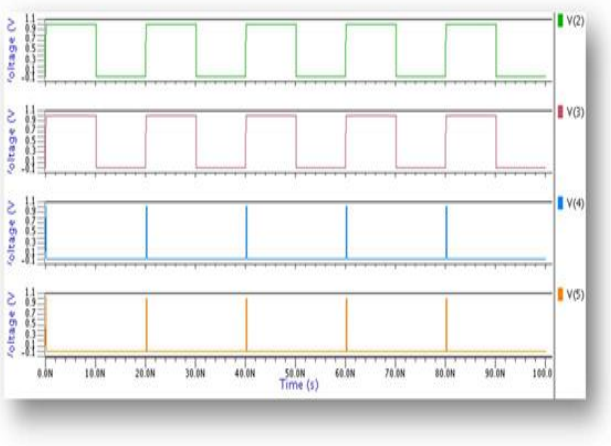

Figure 11. PFD using AND GATE (Lock Condition)90nm

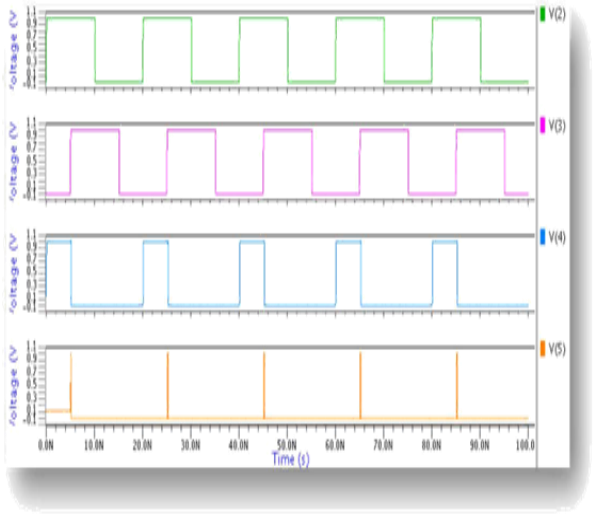

Figure 12. PFD using AND GATE (CLK Leading Condition) 90nm

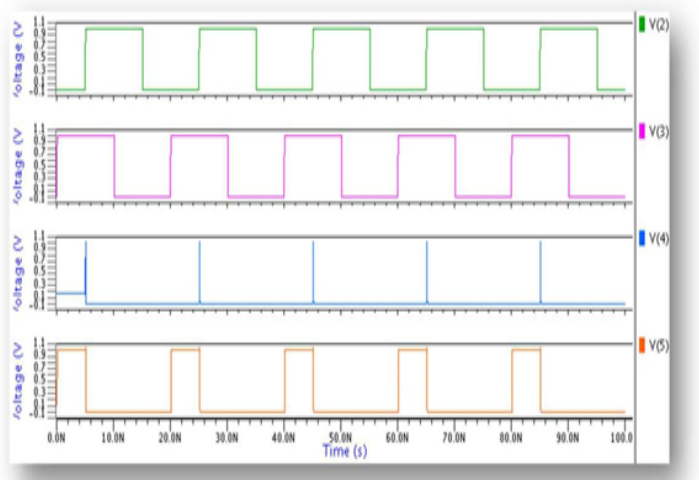

Figure 13. PFD using AND GATE at 20ns (CLK Lagging Condition) 90nm

4.2 Simulation Results of Phase Frequency Detector Using NOR Gate

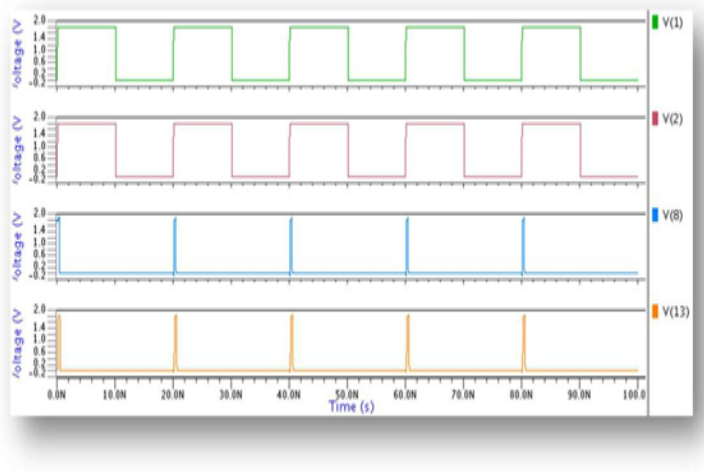

Figure 14. PFD using NOR GATE (Lock Condition) 0.18µm

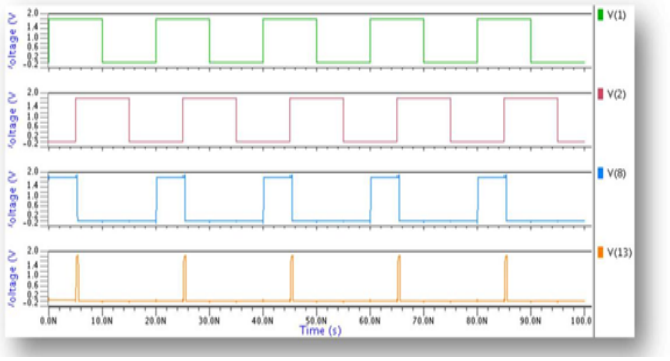

Figure 15. PFD using NOR GATE (CLK Leading Condition) 0.18µm

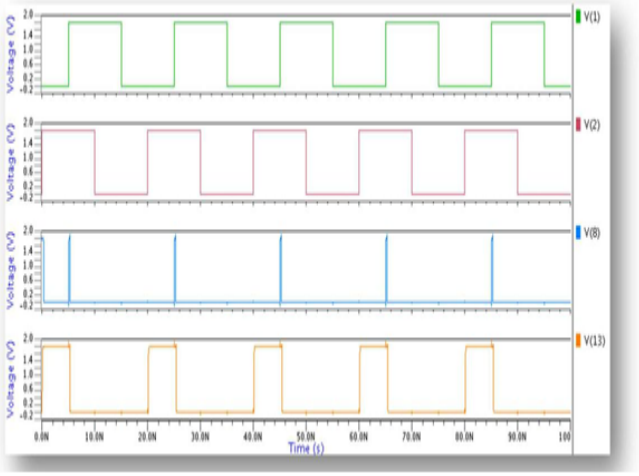

Figure 16. PFD using NOR GATE (CLK Lagging Condition) 0.18µm

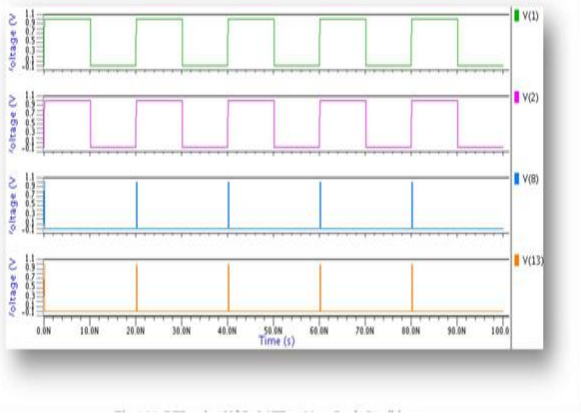

Figure 17. PFD using NOR GATE at 20ns (Lock Condition) 90nm

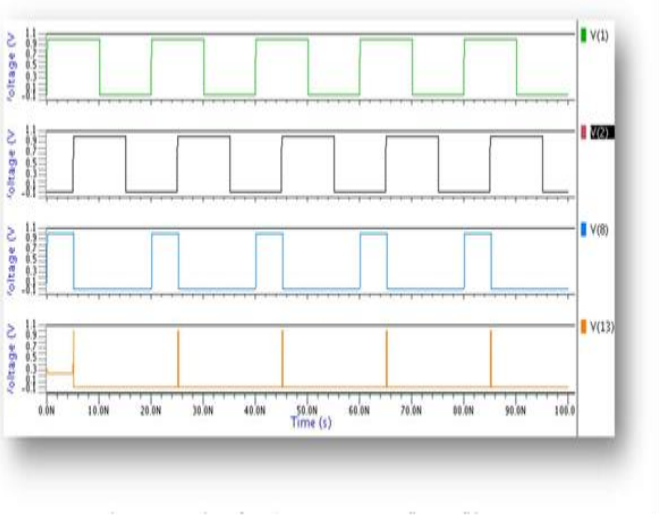

Figure 18. PFD using NOR GATE at 20ns (CLK Lagging Condition) 90nm

4.3 Simulation Results of Phase Frequency Detector Using NAND Gate

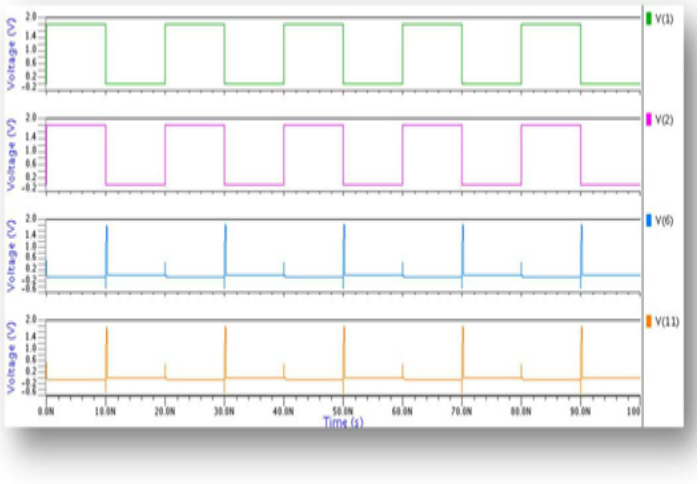

Figure 19. PFD using NAND GATE at 20ns (Lock Condition) 0.18µm

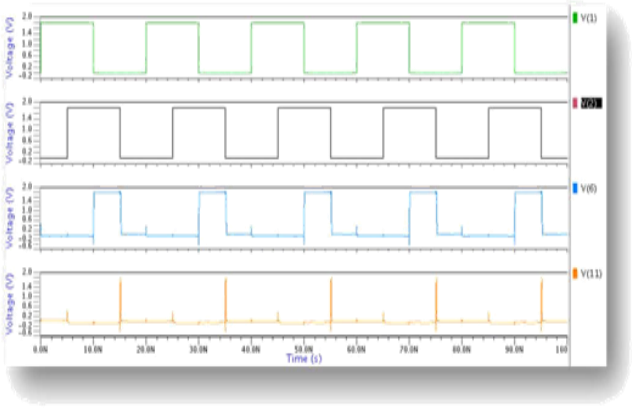

Figure 20. PFD using NAND GATE at 20ns (CLK Leading Condition) 0.18µm

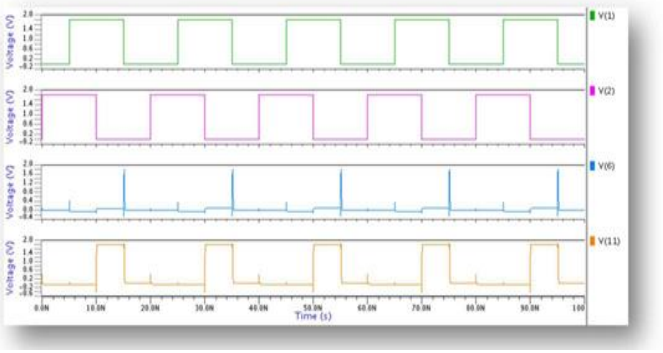

Figure 21. PFD using NAND GATE at 20ns (CLK Lagging Condition) 0.18µm

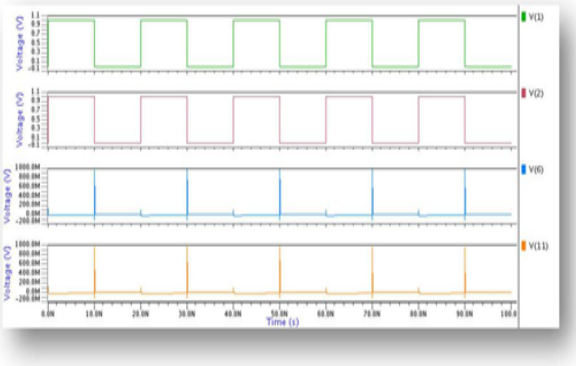

Figure 22. PFD using NAND GATE at 20ns (Lock Condition) 90nm

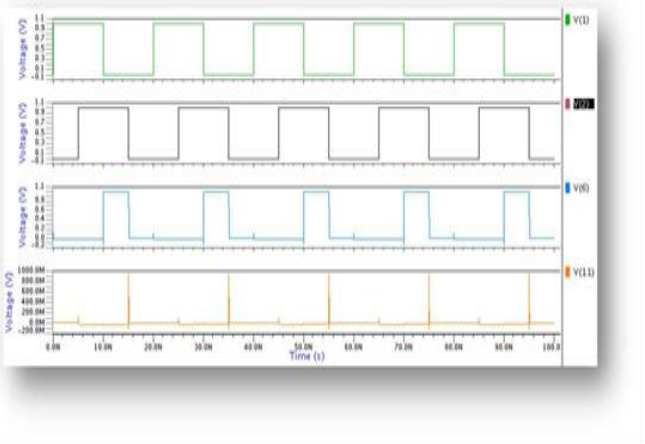

Figure 23. PFD using NAND GATE at 20ns (CLK Leading Condition) 90nm

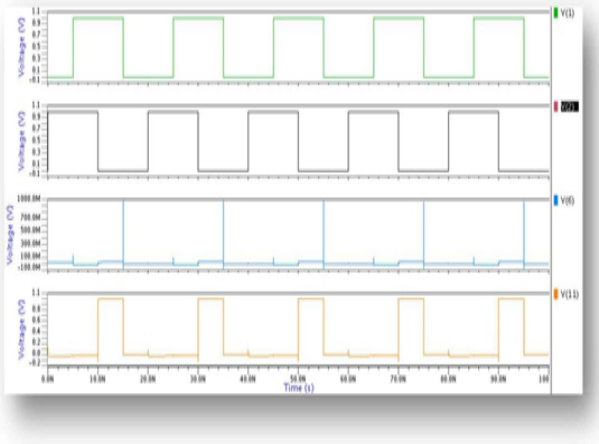

Figure 24. PFD using NAND GATE at 20ns (CLK Lagging Condition) 90nm

4.4 Simulation Results Modified Phase Frequency Detector

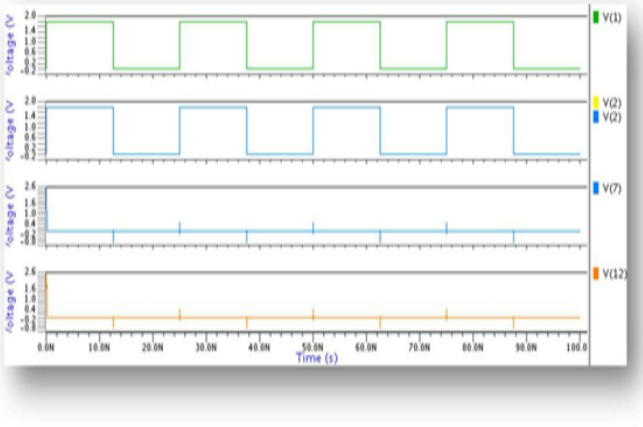

Figure 25. Modified PFD at 50MHz (lock condition) 0.18µm

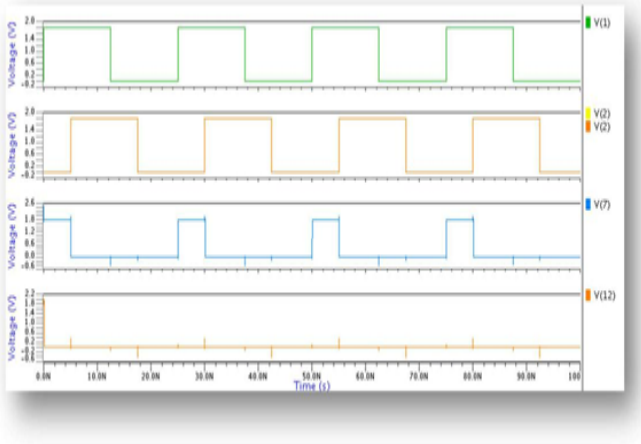

Figure 26. Modified PFD at 50MHz (DATA Leading Condition) 0.18µm

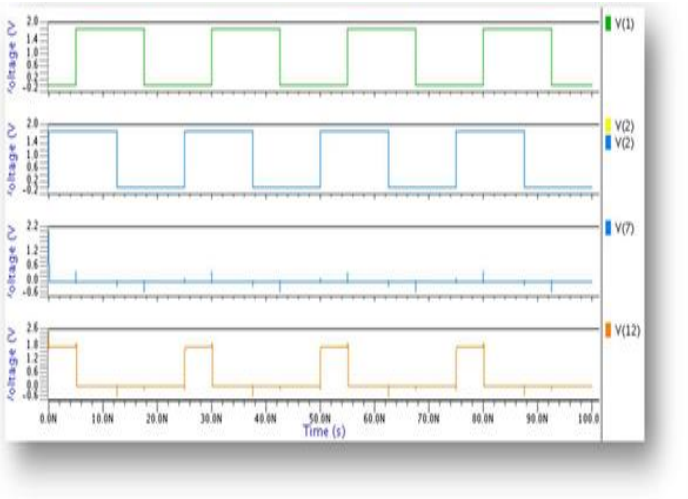

Figure 27. Modified PFD at 50MHz (DATA Lagging Condition) 0.18µm

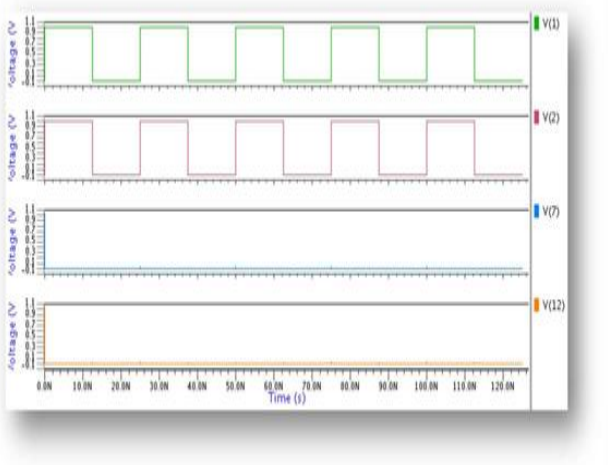

Figure 28. Modified PFD at 50MHz (lock condition) 90nm

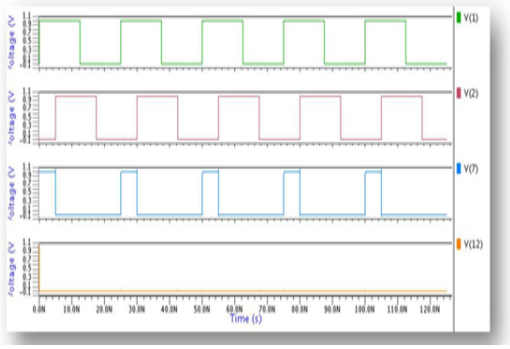

Figure 29. Modified PFD at 50MHz (DATA Leading Condition) 90nm

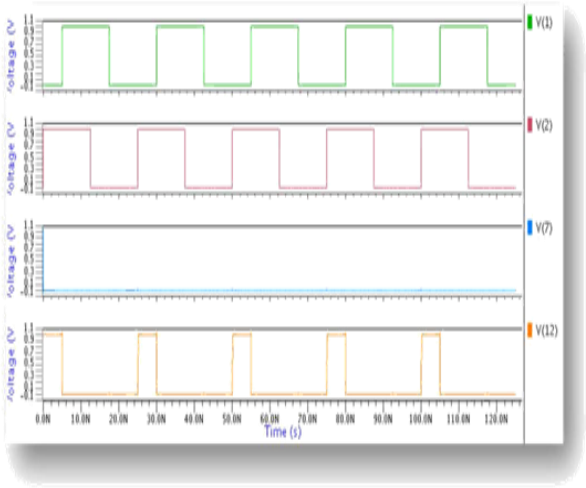

Figure 30. Modified PFD at 50MHz (DATA Lagging Condition) 90nm

Table 1. Result of AND Gate PFD

Parameter	Design Results	
Technology	0.18µm	90nm
Input frequency	1 GHz	1 GHz
Transistor count	22	22
Power consumption	7.7899 µW	5.1769 µW
Dead zone	45ps	13ps
Glitch Period	321ps	82ps

Table 2. Result of NOR Gate PFD

Parameter	Design Results	
Technology	0.18µm	90nm
Input frequency	1 GHz	1 GHz
Transistor count	20	20

Power consumption	6.1316 µW	4.3725 µW
Dead zone	39ps	12ps
Glitch Period	82ps	76ps

Table 3. Result of NAND Gate PFD

Parameter	Design Results	
Technology	0.18µm	90nm
Input frequency	1 GHz	1 GHz
Transistor count	16	16
Power consumption	4.2587 µW	2.6249 µW
Dead zone	18ps	11ps
Glitch Period	245ps	55ps

Table 4. Result of Modified PFD

Parameter	Design Results	
Technology	0.18µm	90nm
Input frequency	1 GHz	1 GHz
Transistor count	16	16
Power consumption	58.714 nW	34. 576 nW
Dead zone	31ps	18ps

V.CONCLUSION

The Phase Frequency Detector is characterized in terms of the Dead-Zone, Glitch period and power consumption. The simulation results allow the circuit designer to fully explore the tradeoffs in Phase Frequency Detector design, such as Dead-Zone, Glitch period and power consumption. The various designs of PFD presented in this paper can be utilized for development of advanced and sophisticated PLL and DLL.

VI. REFERENCES

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