Correspondence of Multilevel Inverters for Smart Grid Communication Systems

Shreya.D.Petkar[1], Srushti.S.Mathad[2], Prof Trupti P.Pawale[3], Prof. Ravindra Motekar[4], Prof. R.L.Chakrasali[5]
[1,2,3,4]*Department of Electrical and Electronics Engineering, KLS VDIT, Haliyal,*
[5]*Department of Electrical and Electronics Engineering, SDM, CET, Dharwad*
Karnataka, India.

Abstract - In recent years, voltage source multilevel inverters are being applied extensively in industry as they have many advantages compared to conventional two level inverters. It's an electronic device used in the implementation of high power. The major advantage such as higher output voltage at low switching frequency, low voltage stress(dv/dt), lower total harmonic distortion(THD),less electro-magnetic interference (EMI),smaller output filter and higher fundamental. The output of hybrid system of solar(PV cells) and wind power is given to inverter with original switching frequency, the inverter discussed in this paper has the capacity of generating 7 levels of voltage the output, is replicated by MATLB/SIMULINK software. The strength and potential of this inverter is agreed from the result of Simulation model to breed the multilevel of voltage. Smart grid is used to improvise to existing conventional transmission and distribution system so as to make it more reliable in terms of performance, power quality customer satisfaction, security etc. Therefore smart grid when combined with hybrid system with advanced levels of electric data from one node to other node considering the authentication and security as the primary and essential need to make the system intelligently.

I. INTRODUCTION

With the ever increasing energy demand and depletion of fossil reserves the modern world is shifting towards the period of energy crisis. The carbon footprint is increasing day by day from these conventional sources so it has compelled to look after the alternative energy sources which are both cost effective and eco-friendly.

Solar energy and wind energy comes under this category, but their intermittent nature makes it difficult to supply stable and continues power. Because the solar source exhibits the direct current when exposed to solar radiations, and wind exhibits alternating current so combining these two is difficult with the different nature. So once the energy of the PV cells is converted to from DC to AC so the next process of combining the solar and the wind energy will become an easy task. However this hybrid system which also includes the storage system such as battery helps to overcome problem of back protection. Morden techniques are developed to increase the efficiency of the storage system and converts ensuring maximum power generation with minimum requirement of equipment.

This new multilevel inverters, for the hybrid renewable energy system increases the voltage gain and improves the voltage profile by reducing the harmonic content resulting in the improved power quality compared to existing system. Such a new multilevel inverter are used fro integration of hybrid energy and must have feasible attributes to support for the sustainable and high power quality. The inverters convert DC to AC and help to maintain the fixed voltage and frequency for wind turbine generator for various loads. The inverter which exhibit the characters like highly productive, low stand by losses, low harmonic distortion, easy maintenance, and reliability are good off-grid inverters. As the demand from the customer is increased for the quality and clean power supply, that fulfilled by levels of the inverters switching in the design if the inverter is improved. The inverter is designed as a MLI by its levels of switching. MLI have found use in renewable energy sources interface and in micro grids and etc. Based on these background, the paper gives us the information of modern topology for 3 phase 7 levels of MLI. The MATLAB/SIMULINK tool is used to conclude the results for the hybrid system.

Communication - The main goal of the SG system to provide the authentication and security and to do this means to digitalize the system, so to achieve this it becomes very important to provide the communication or link between the various nodes at the sender as well as receiving end. The speeds the work of identifying the errors, inspects the system, secure the system against cyber attacks and so on.

II. CIRCUIT OF CONVENTIONAL TOPOLOGY

There are two types of cascaded inverters, i.e. symmetrical and asymmetrical. If the inverter is installed with equally balance values of input voltage source and at this level, if n number of sources exits in every phase then the load can be reached at 2n+1 levels such inverters are symmetric cascaded inverters. Most of the cascade symmetrical inverters have the potential of generating multiple voltage sources and more voltage levels. The conventional inverters have the series construction of H-bridges. Each bridge in the series is with the voltage source and anti parallel diode with the four switches of unidirectional. These have the capacity of generating 3 voltage levels; +VDC,0 and –VDC at the output.

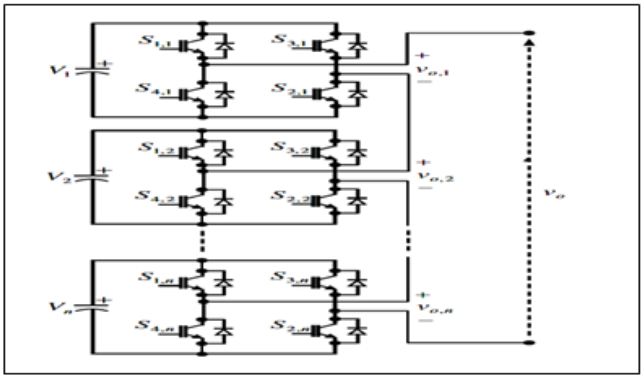


Figure 1: cascaded MLI topology.

As explained before its with the n number of voltage sources occur in the inverter construction.
Hence equation 1 becomes the input sources values in the unary incremental scheme
Vk=Va
Va = a V1 a = 1,2,3,.....n (1)
Equation 2 represents the binary incremental scheme of input voltage source values
Va = a2 V1 a =1,2,3,.....n-1 (2)
Equation 3 represents trinary incremental scheme of input voltage source values
Va = 3 a V1 a =1,2,3,.....n-1 (3)

III. THE PROPOSED TOPOLOGY

Fig 2 will give the picture of schematic block diagram of MLI. From the figure the inverter comprises of n number of input ports as a voltage source and the switches with 2n+2 in number. All the switching of the circuit consist of anti parallel diodes with the unidirectional IGBTs. H-bridge can produce voltage levels of positive and negative because the polarity at the input will be changing alternatively. In fig 2 the complete system consists of two parts; power section and control section. The power section comprises of power rectifier, filter capacitor, and 3 phase diode clamped MLI. To have a non pulsating output at the capacitor filter we have to feed the 3 phase bridge rectifier with the sinusoidal input. The condenser filter in the circuit will completely take off the ripple in the DC voltage. Here with the help of capacitor filter the pure DC voltage is supplied to the 3 phase MLI. To generate the AC output from the DC input voltage the MLI consist of 36 MOSFET/IGBT controlled switches in the circuit.

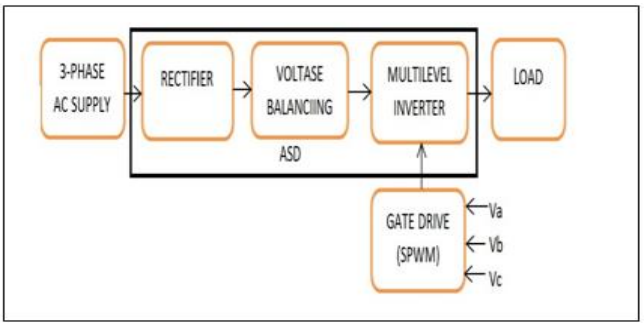


Figure 2: Block diagram of cascaded multilevel inerter

Table 1: voltage level with respect to no of switches

No.of input sources	No.of output voltage levels	Switches for proposed topology	Switches for conventional topology
4	7	5	12

The controlled circuit of the projected system is kept under the observation by the Gate triggered circuit, optocoulper and microcontroller. To oblige the MLI through the MOSFET switches the microcontroller will produce signal of 5 volt. To get the better results like production of different output voltage, which also reduces the final cost of the inverters, carpet area and switching losses the proposed inverters uses fewer switches compared to the traditional cascade which is according to the table displayed above. The table1 explains the generation of output voltage and also number of switches required for single phase conventional cascade inverter in both the symmetrical and asymmetrical ways.

IV. SIMULATION MODEL

To produce the 7 level output voltage with 5 IGBTs and 4 DC power source of 12V are used. This is shown in the simulation model of fig 3. Fig 7 shows simulated output voltage. The help of FFT window in MATLAB/SIMULINK the harmonic spectrum is analyzed.

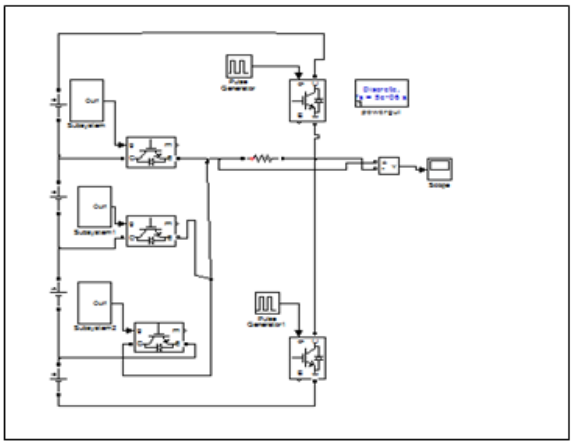


Figure 3: model of MLI with 5 witches.

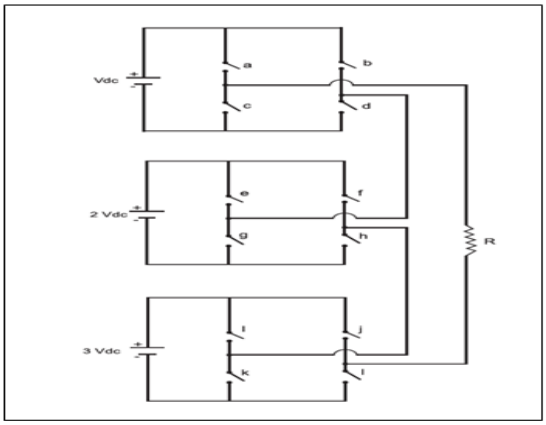


Figure 4: model of MLI with 12 switches.

Table 2: Switching scheme of MLI (12 switches).

	A	B	C	D	E	F	G	H	I	J	K	L
0	0	0	0	0	0	0	0	0	0	0	0	0
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
2Vdc	1	0	0	1	1	0	0	1	0	0	1	1
3Vdc	1	0	0	1	1	0	0	1	1	0	0	1
2Vdc	1	0	0	1	1	0	0	1	0	0	1	1
Vdc	1	0	0	1	0	0	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0
- Vdc	0	1	1	0	1	1	0	0	1	1	0	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0

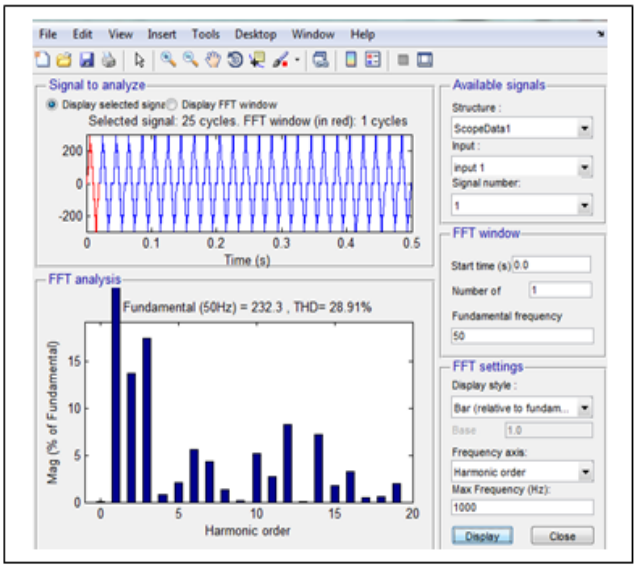


Figure 5: THD of MLI (12 switches).

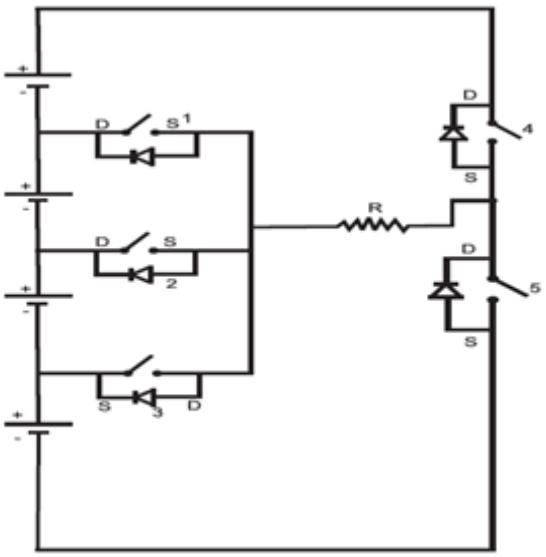
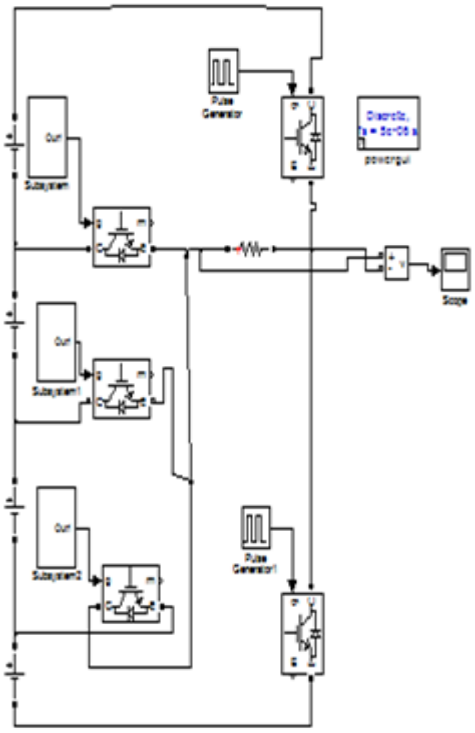


Figure 6: Schematic diagram of MLI(5switches).



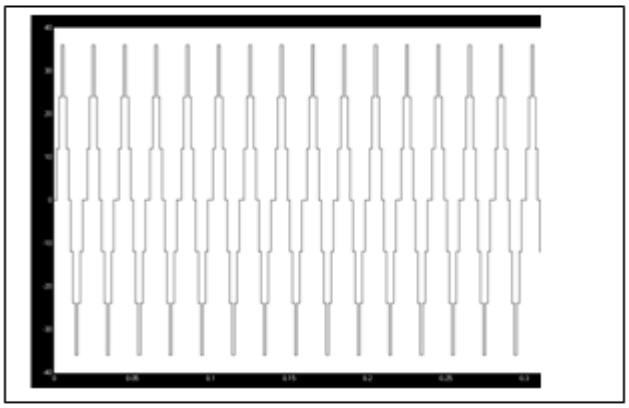


Figure 7: Output voltage waveform of MLI.

Table3: Switching scheme of MLI(5 switches)

	a	b	c	d	E
0	0	0	0	0	0
Vdc	1	0	0	1	0
2Vdc	0	1	0	1	0
3Vdc	0	0	1	1	0
2Vdc	0	1	0	1	0
Vdc	1	0	0	1	0
0	0	0	0	0	0
- Vdc	0	0	1	0	1
-2Vdc	0	1	0	0	1
-3Vdc	1	0	0	0	1
-2Vdc	0	1	0	0	1
-Vdc	0	0	1	0	1
0	0	0	0	0	0

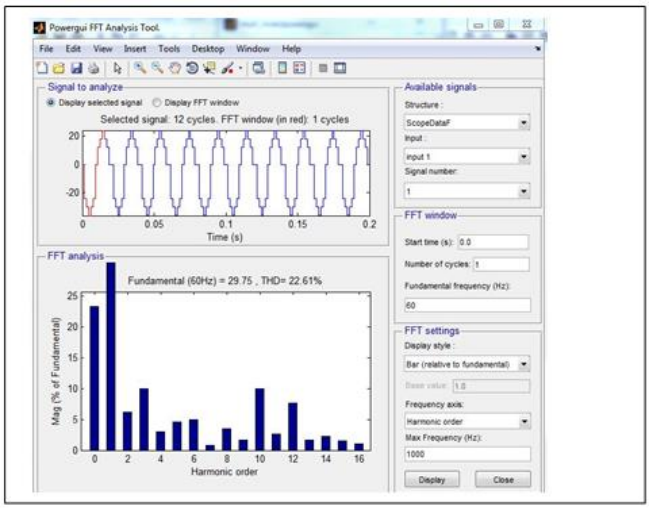


Figure 8: THD of MLI (5 switches).

V. RESULTS AND DISCUSSION

The fig 7 depicted, it resembles much more to a sine wave. The proposed inverter has a 7 levels of voltage in its half cycle due to an uneven step widths. The harmonic distortion is bête compared to earlier topologies. To find the percentage of THD of output voltage waveform the FFT study of output voltage must be carried out. According to planned topology i.e. 7 level inverter with 5 switches the THD is 22.61% and also its without the use of LC filter which is shown in the fig 8. By using the 12 switches its 28.91%. So in comparison with other topologies the 7 level MLI with 5 switch has the many advantages. Compared to cascade topology the necessity of switches here is less. As we have topology of flying capacitor there is not a problem of voltage unbalance. As mentioned before the 3 levels of voltages are generated i.e. +VDC, 0, and –VDC. So as to make it digitalized its provided with the communication or linked between the various nodes at the sender and receiving ends. The main goal of the system is to provide authentication and security.

VI. CONCLUSION

The projected inverter in this paper is 1-phase 7 level inverter is exposed to generate an increased stepped output with few switches of semiconductor. Size of the geometric area is reduced due to less complicity by the use of the fewer switches and by controlling over all circuit. According to the result reduced THD and switched losses are obtained. As discussed in the results the THD with the 5 switches is 22.61% and with the 12 switches its 28.91% is recorded. As we have observed in the simulation the THD decreases with the decrease in the number of switches. So this planned topology is giving us the THD within the standards so next attempt of the project is to obtain the THD in the range of 15-25% with the reduction in the number of switches. To authenticate the design and the result of MATLAB is also provided. Therefore the combination of this advanced inverter with the hybrid system helps in the communication of electric data from one node to other node with the security.

VII. ACKNOWLEDGEMENT

The sense of contentment and elation that accompanies successful completion of this paper be incomplete without mentioning the names of the peoples who helped me in accomplishing this work.

We humbly thank Prof. Manjunatha HOD, Department of Electrical and Electronics, VDIT, Haliyal for their encouragement.

We would like to express my sincere gratitude toour guides Prof. Ravindra Motekar and Prof. Trupti Pawale for their continuous support and encouragement and invaluable guidance throughout the project synopsis.

We extend my sincere thanks to all teaching and non teaching staff for their valuable support and guidance.

VIII. REFERENCES

[1]. M.H.Rashid, Power Electronics: Circuits, Devices and Applications, Prentice Hall, New York, NY, USA, 3rd edition, 2004.

[2]. T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. P. Kothari, “Cascaded seven level inverter with reduced number of switches using level shifting PWM technique,” in International Conference on Power, Energy and Control (ICPEC ’13), pp. 676–680, February 2013.

[3]. R. A. Ahmed, S. Mekhilef, and H. W. Ping, “New multilevel inverter topology with minimum number of switches,” in Proceedings of the 14th International Middle East Power Systems Conference (MEPCON ’10), pp. 1862–1867, Cairo University,Cairo, Egypt, December 2010.

[4]. J. J. Nedumgatt, D. Vijayakumar, A. Kirubakaran, and S. Umashankar, “A multilevel inverter with reduced number of switches,” in Proceedings of the IEEE Students’ Conference on Electrical, Electronics and Computer Science (SCEECS ’12), pp.1–4, March 2012.

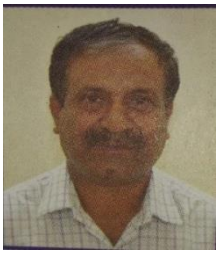
Authors profile

Shreya .D. Petkar
Student of kls’s vdit haliyal
Perceiving BE in Electrical and Electreonics

Srushti.S. Mathad
Student of kls’s vdit haliyal
Perceiving BE in Electrical and Electreonics

Prof. Trupti P. Pawale
B.E: In Electrical Engineering from K. K. Wagh College of Engineering and Technology,
Nasik under Pune University (2002)
M.Tech: In Digital Electronics from BVBCET, Hubli (2011)
Ph.D: Pursuing in the area of Stand Alone (Hybrid) Smart Grids

Prof. Ravindra Motekar
B.E: In E & E Engg. from Gogte Institute of Technology, Belagavi (2011)
M.Tech: In Industrial Electronics from VDRIT, Haliyal (2015)



Prof.R.L.Charasali
Dean academic and R and D of SDM CET, Dharwad