Folded 32 Bit Carry Skip Adder Using Carry Feed Forward Adder

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Abstract- In this paper, folded carry skip pass adder was implemented and demonstrated. This effects in low power consumption when as compared with hybrid carry skip adder. In this carry skip unit became replaced via a prediction block named convey feed forward which gives us intermediately predictions and facilitates eliminating prediction block and nucleus level and minimizes the complexity of architecture. This reduces the delay issue of the circuit. The resultant simulations had been implemented the usage of CADENCE-verilog, The analysis of results represents low energy consumption through essential course..

IndexTerms **-** Carry Skip adder, low energy consumption, hybrid carry skip adder, prediction block, carry feed forward.

I. INTRODUCTION

Cryptography An adder is a digital circuit that plays addition of numbers. In many computers and different varieties of processors adders are used inside the arithmetic common sense gadgets or ALU. They also are utilized in other components of the processor, in which they are used to calculate addresses, table indices, increment and decrement operators, and comparable operations.

Although adders may be constructed for lots variety representations, along with binary-coded decimal or extra-3, the most common adders function on binary numbers. In cases in which 's complement or ones' supplement is getting used to symbolize negative numbers, it is trivial to alter an adder into an adder–subtractor. Other signed quantity representations require extra common sense around the basic adder.

In this segment, a quick description of the adder architecture and the exact time delay (T) and region (A) complexity based on unit gate version is presented. In the unit gate version each gate has a gate-rely of 1 and a gate-delay of one except XOR and XNOR gates having gate counts and gate delays of , while the gates with more than 2 inputs, the gate-counts and gate-delays may be computed in terms of the ones given for the gates with inputs; also, inverters and buffers are neglected.

The popular deliver generate-propagate common sense is used to reduce the critical put off of the adder at the same time as blocks of RCAs are used for lesser strength consumption. In our layout, the generate propagate logic balances the delay and the wide variety of inputs to the bypass logic limits the vital course put off.

The 32-bit convey-bypass adder layout offered in this paper uses a aggregate of RCAs together with convey-bypass logic (SKIP), carry-generate common sense (CG), and institution generate propagate logic (PG). The whole adder is split into some of variable-width blocks. Both the carry era and bypass logic use AOI and OAI circuits. The width of every block is confined via the target delay T. Each block is similarly divided into sub-blocks. A sub-block can also contain extra stages of sub-blocks in a recursive manner. The lowest-degree sub-block is fashioned by a number of variable width RCAs.

Power dissipation is important trouble in the electronics device so the purpose of this assignment is to analyze and compare the performance of Carry skip adder at exceptional enter voltages. Various filter out designs are found in adder utility so it's miles required to efficaciously compute the multiply and acquire operations. Various strategies were proposed to layout multiplexer which can be efficient in terms of overall performance, low energy consumption and region.

II. LITERATURE REVIEW

Since there's a finite upward thrust/fall time for both pMOS and nMOS, during transition, as an example, from off to on, each the transistors may be on for a small time period in which contemporary will find a direction immediately from VDD to floor, as a result creating a quick-circuit modern. Short-circuit strength dissipation will increase with upward push and fall time of the transistors.

An extra form of electricity intake have become tremendous in the Nineties as wires on chip became narrower and the long wires have become greater resistive. CMOS gates at the end of those resistive wires see slow input transitions. During the middle of these transitions, both the NMOS and PMOS logic networks are partially conductive, and contemporary flows without delay from VDD to VSS. The power for that reason used is known as crowbar energy. Careful layout which avoids weakly pushed long skinny wires ameliorates this impact, but crowbar power can be a vast a part of dynamic CMOS energy.

To accelerate designs, producers have switched to constructions which have decrease voltage thresholds but because of this a present day NMOS transistor with a Vth of two hundred mV has a sizeable subthreshold leakage modern. Designs (e.G. Desktop processors) which consist of considerable numbers of circuits which aren't actively switching still eat power because of this leakage cutting-edge. Leakage energy is a enormous part of the entire energy consumed by means of such designs. Multi-threshold CMOS (MTCMOS), now to be had from foundries, is one technique to managing leakage strength. With MTCMOS, high Vth transistors are used whilst switching velocity is very crucial, even as low Vth transistors are used in speed touchy paths. Further generation advances that use even thinner gate dielectrics have a further leakage component because of present day tunnelling thru the extremely thin gate dielectric. Using high-okay dielectrics rather than silicon dioxide that is the conventional gate dielectric permits similar device overall performance, however with a thicker gate insulator, for this

reason keeping off this current. Leakage strength reduction the use of new fabric and system designs is important to sustaining scaling of CMOS.

ADDERS are a key constructing block in arithmetic and logic gadgets (ALUs) [1] and as a result increasing their speed and decreasing their energy/energy consumption strongly have an effect on the rate and power consumption of processors. There are many works at the challenge of optimizing the rate and electricity of these units, which have been mentioned in [2]–[9]. Obviously, it's miles highly suited to gain better speeds at low-power/energy consumptions, which is a assignment for the designers of general cause processors.

One of the effective techniques to decrease the strength intake of digital circuits is to lessen the supply voltage due to quadratic dependence of the switching power on the voltage. Moreover, the subthreshold modern, which is the main leakage issue in OFF devices, has an exponential dependence on the deliver voltage stage through the drain-induced barrier lowering impact [10]. Depending on the quantity of the supply voltage discount, the operation of ON gadgets may live in the superthreshold, near-threshold, or subthreshold areas. Working inside the superthreshold area presents us with decrease put off and better switching and leakage powers compared with the near/subthreshold regions. In the subthreshold place, the good judgment gate put off and leakage electricity show off exponential dependences on the supply and threshold voltages. Moreover, these voltages are (probably) problem to technique and environmental variations within the nanoscale technologies. The versions boom uncertainties inside the aforesaid overall performance parameters. In addition, the small subthreshold cutting-edge reasons a big delay for the circuits running in the subthreshold region [10].

Recently, the close to-threshold location has been considered as a region that offers a more appropriate tradeoff point among put off and power dissipation compared with that of the subthreshold one, as it effects in lower postpone compared with the subthreshold vicinity and notably lowers switching and leakage powers as compared with the superthreshold location. In addition, near-threshold operation, which makes use of deliver voltage levels close to the edge voltage of transistors [11], suffers notably much less from the system and environmental versions as compared with the sub-threshold region.

There are many adder households with distinct delays, power consumptions, and area usages. Examples encompass ripple bring adder (RCA), bring increment adder (CIA), carry skip adder (CSKA), bring choose adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures together with their characteristics may be observed in [1] and [13]. The RCA has the only shape with the smallest vicinity and power consumption however with the worst vital course delay. In the CSLA, the speed, power intake, and vicinity usages are drastically larger than those of the RCA.

The PPAs, which might be also referred to as deliver appearance-ahead adders, take advantage of direct parallel prefix structures to generate the deliver as rapid as viable [14]. There are different styles of the parallel prefix algorithms that lead to distinct PPA structures with one-of-a-kind performances.

As an instance, the Kogge–Stone adder (KSA) [15] is one of the quickest structures however consequences in huge energy intake and location utilization. It need to be mentioned that the shape complexities of PPAs are more than those of different adder schemes [13], [16]. The CSKA, which is an effective adder in terms of energy intake and area utilization, become brought in [17]. The vital direction postpone of the CSKA is a great deal smaller than the one in the RCA, while its region and power intake are much like those of the RCA.

In addition, the strength-put off product (PDP) of the CSKA is smaller than the ones of the CSLA and PPA systems [19]. In addition, due to the small variety of transistors, the CSKA advantages from relatively brief wiring lengths as well as a normal and simple format [18]. The relatively lower speed of this adder shape, but, limits its use for high-pace programs.

In this thesis, given the attractive functions of the CSKA shape, we've got focused on reducing its delay via editing its implementation based totally on the static CMOS logic. The awareness on the static CMOS originates from the preference to have a reliably operating circuit under a wide range of supply voltages in fairly scaled technology [10]. The proposed change increases the speed notably whilst maintaining the low area and energy consumption capabilities of the CSKA. In addition, an adjustment of the structure, based on the variable latency method, which in flip lowers the energy consumption with out significantly impacting the CSKA velocity, is also offered. To the nice of our know-how, no paintings focusing on layout of CSKAs operating from the first-rate threshold place right down to near-threshold area and additionally, the layout of (hybrid) variable latency CSKA structures were pronounced inside the literature.

III. METHODOLOGY

The sum is found in two stages. The RCA block finds intermediate results that are the first stage and the final result is the result from the incrementation block. The incrementation block is a chain of half adders in which one input is carry of previous stage and other input is intermediate result. Since the carry input is given to incrementation block, there is no carry input for RCA block and hence all the 1st Full adders of RCA block in all stages except the 1st stage can be replaced by half adder. In the first stage sum is calculated by RCA and the carry is propagated to AOI block. The propagated carry is given to both AOI skip logic and also to the incrementation block. Since the RCA blocks of every stage does not requires carry of previous stages all RCA block find the intermediate results simultaneously.

The operation of AOI and OAI stages can be explained by two cases, first case is that if carry is propagated from previous state and second is when carry is not propagated. Consider the case in which carry is propagated from previous stage and all input bits are in carry propagation condition, then all intermediate bits will be 1, hence the output of AND gate will be 1. This one will be propagated to AOI logic. The first gate

of AOI compound gate is AND gate. This AND gate will generate 1 only if there is a carry from previous stage is 1. The second gate of AOI compound gate is NOR. So the input to this NOR will be one so it will generate output 0, which is the inverted carry from previous stage.

This is again inverted by a NOT gate and given to incrementation block. So the time of propagation of carry in this case will be the sum of time taken by and gate TAND and time taken by skip logics which can be TOAI or TAOI logic.

If all input bits are in propagation condition and carry from previous stage is zero the output of AND gate in AOI will be zero and hence it have to wait to receive the third input which is from RCA. Same condition exists if the input bits are not in propagation condition. Similar case occurs for OAI block also. The time required for carry propagation if all the intermediate results are not one will be the sum of time taken for carry propagation through the RCA chain TRCA and the time taken for carry to propagate through the skip logic.

Advantage of this model is that for finding carry output of next stage the carry from incrementation block is not required. So the delay for generation of final result does not depends on the delay for carry propagation from one block to other. Also all the intermediate results can be calculated simultaneously by RCA without waiting for the carry from previous block. The carry is calculated based on intermediate results and carry from previous block. The disadvantage of this model is that if all inputs are not in propagation condition then all the intermediate results will not be one, in such cases the skip logic have to wait for the carry from RCA block.

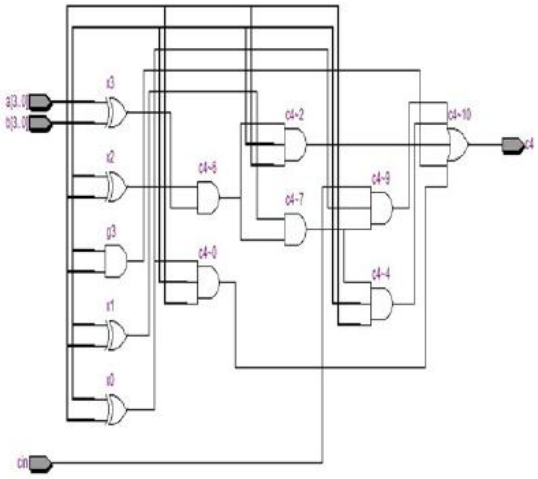

Fig.1: CARRY FEED FORWARD BLOCK

In conventional carry skip adder the carry is skipped only when all input bits are in propagation mode. Only in this case the carry prediction unit will generate an output of one, which is given to multiplexer as select line. Based on this input the multiplexer is selecting any one of the input that is the carry of previous state or the carry of the RCA. If the input bits are not in propagation mode the adder will have to wait until the carry of RCA block is generated. The probability of all bits in propagation mode is very less. The idea of proposed model is that to generate the carry from of the input bits, if input bits are not in propagation condition. The input bits are first fed to a XOR gate. In this step we can reuse the XOR gate which is used by the carry prediction unit. The carry is generated from this XOR outputs by using simple ANDOR logic which is a modified version used in Look ahead carry adder. The block which is used to generate carry is carry feed forward block (Fig.3) and the complete architecture is shown in Fig.4. The carry generated by this carry feed forward block is fed to the input of multiplexer. The multiplexer will select the carry generated from carry feed forward block if the input bits are not in propagation mode. So the delay when input bits are not in propagation condition (eq.6) is the sum of time for propagation through XOR gate and time for propagation through AND-OR logic and time for propagation through the skip logic.

T=TXOR+TAND+TOR+TMUX---- Eq.(6)

Delay in conventional adder was the delay of RCA chain that is reduced to delay of AND and OR logic. The proposed model can generate the carry without much delay when the input bits are not in propagation condition. A conventional carry skip adder skip carry only if the bits are in propagation condition, and in other cases the delay will be proportional to number of XOR gate the carry propagates. Since the carry is generated by the carry feed forward mechanism we does not require carry from the RCA chain. So the last full adder in this RCA chain is replaced by two XOR gates. The two AND gates in the last full adder of each RCA block can be removed, which helps to reduce the area. For generating the carry the carry feed forward block requires 4-AND gates and 1-OR gate. Out of this 4-AND gates two will be compensated by removal of two AND gate from last full adder of RCA chain. So only two AND gates and one OR gate will be more in the proposed architecture. The proposed model is more optimized version of CSKA for high speed applications.

In C.I.CSKA carry skip adder the carry is skipped only when all the intermediate inputs are one. This happens only when all input bits are in propagation mode. If this case is not happed the second gate in OAI-AOI compound gate will wait for the carry generated by the RCA block. If the carry starts propagating from the first adder then the carry have to propagate through all eight XOR gates and the delay in this case will the very high.

The proposed CFF-C.I.CSKA uses the same CFF mechanism which is used by CFF-CSKA. That is to generate the carry from of the input bits. The input bits are first fed to a XOR gate. The output of this XOR gate is fed to AND-OR logic to generate the carry of each RCA block. The block which is used to generate carry is carry feed forward block (Fig.3) and the complete proposed architecture is shown in Fig.1. The carry generated by this carry feed forward block is fed to the second gate of AOI-OAI skip logic.

In cases where the input bits are not in propagation mode the CFF block will generate the carry output using ANDOR logic, from the XOR ed input bits. The CFF block requires two three input AND gate and one OR gate. Since the carry provided to each RCA block is zero, the number of AND gates in carry feedforward block can be limited to three. Since the last full

adder is modified with out AND gates, the newly added block requires only one AND and one OR gate. By adding 4-XOR gates, one AND and one OR gate per block it is possible to make the C.I.CSKA to skip carry in all conditions.

Since the carry input to each RCA block is zero, the first full adder in each RCA block can be replaced by half adders. Also the carry generated by RCA block is not required because the carry feedforward block generates the carry. Hence the last full adder of RCA chain is modified in such a way that the two AND gates required for the generation of output carry is removed. The carry generated by CFF block helps the second gate in the AOI-OAI logic to decide the carry of next block. The advantage is that if the bits are not in propagation mode the adder will have to wait until the carry of RCA block is generated. This architecture has so many advantages. In CI-CSKA finding carry output of each stage the carry from incrementation block is not required. In CFF CI-CSKA the carry for next block does not requires the carry from incrementation block as well as from RCA block. The carry from RCA block is generated by CFF block which can reduce the delay (E.7).

TMAX=TXOR+TAND+TOR+TAOI(or)TOAI-------(7)

Thus the carry is calculated based on intermediate results and carry from previous block if all intermediate bits are in propagation condition. If not the carry to next state is find from CFF mechanism. The disadvantage of this model is that for carry calculation we requires 4- XOR gates, three AND gates and one OR gate per block. Since the first full adder in each RCA block is replaced by half adder and the last full adder of RCA chain is modified in such a way that the two AND gates required for the generation of output carry is removed the increase in area due to feed forward block can be compensated to a greater extend. This proposed CFF-CI-CSKA is an area efficient model which compensates for two XOR gates and two AND gates. CFF-CI-CSKA can be used for high speed applications.

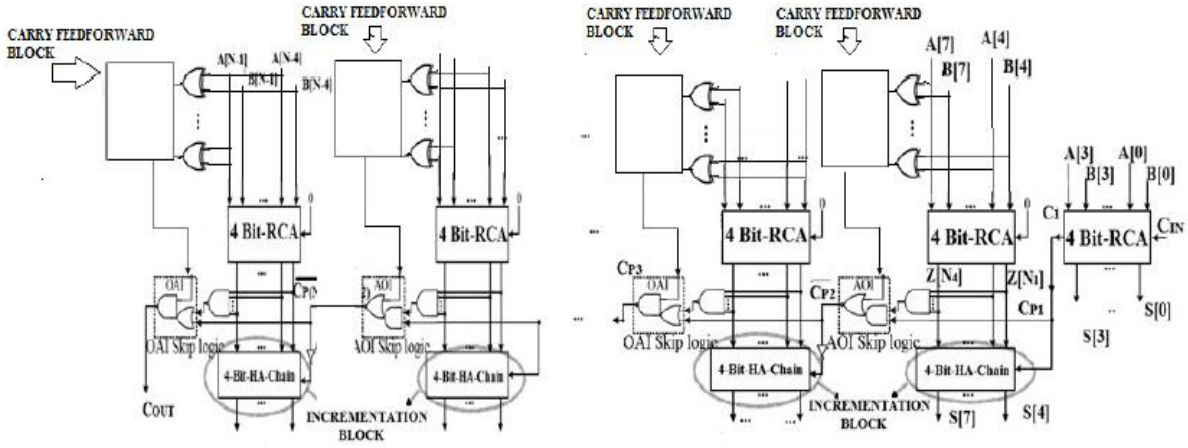

Fig.2: Proposing CI-FOLDED-CSKA ARCHITECTURE

Each 4-bit CSA block is formed by cascading four FAs. As the mirror circuit only produces *Co*. So, if we want to connect two FAs, we need to invert it back to *Co*. However, this can slow down the whole circuit because it will add more inverters to the carry propagation path. Fortunately, if we invert all *A, B* and *Ci* signals, from the equations (1, 2, 3), value of *P* does not change while values of both *S* and *Co* are inverted. From this observation, the 4-bit CSA block can be formed as depicted, no inverter is needed at the carry outputs of each FA. The carry is skipped if $P\_ = P3P2P1P0 = 1$ (as shown in Fig. 1). To avoid a high fan-in circuit that can make the $Ion/Io\ f\ f$ ratio low at subthreshold voltages, the logic $P\_$ is formed from only 2-input NAND and NOR gates as shown in Fig. 4(a) (instead of an 4-input AND gates). The 2-input NAND and NOR gates are shown in Fig. 4(b) and (c) with transistor sizing in order that they have worst-case pullup and pulldown times equivalent to a minimum size balanced inverter (which was shown in Fig. 2(b)).

The carry out of a 4-bit CSA block is gotten from a 2-input MUX. This MUX uses a transmission gate with buffer (by an inverter) at output as shown in Fig. 6. Benefit of the output buffer here is two-fold. First, it makes *Cout* stronger at output of each 4-bit CSA block. Second, it avoids the case when *C*0 can be skipped and travels through all eight 4-bit blocks without any intermediate buffer. This will seriously degrade the final carry output signal due to weak driving current (so it will not meet the robustness requirement of $VOL\ \_\ 0.1VDD$ and $VOH\ \_\ 0.9VDD$ even at high supply voltages), and also slows down the overall speed of the adder.

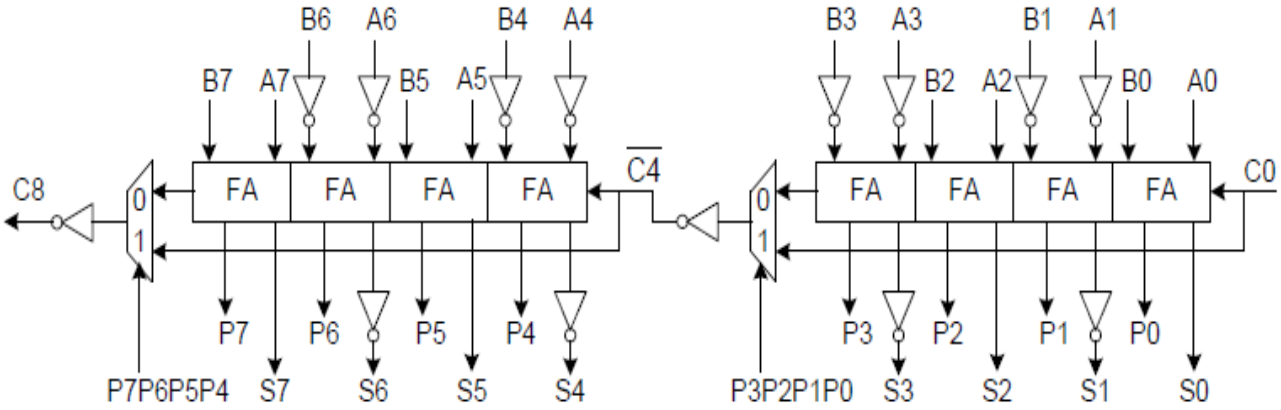

Fig.3: Connection of two 4-bit CSA with carry out inverted to form a 8-bit adder.

However, with this output MUX buffer, the carry out of 4-bit block is inverted. Again, instead of using one more inverter for inverting this carry out before connecting it to the next block, we can build the next 4-bit block with inputs inverted as depicted. These two 4-bit CSA blocks form an 8- bit adder block. The final 32-bit adder is formed by cascading these four 8-bit blocks.

IV. RESULTS AND DISCUSSION

a. Results of Descriptive Statics of Study Variables

TABLE 1: EXISITNG SCHEME:

VDD	POWER(mW)	DELAY
0.7	6.47	4.8
0.8	7.3	4.61
0.9	7.43	4.51
1.0	8.05	4.46
1.1	8.13	4.23

TABLE 2: PROPOSING SCHEME

VDD	POWER(mW)	DELAY
0.7	6.32	4.67
0.8	6.53	4.62
0.9	6.84	4.51
1.0	7.5	4.4
1.1	7.8	4.02

b. Results of Simulation

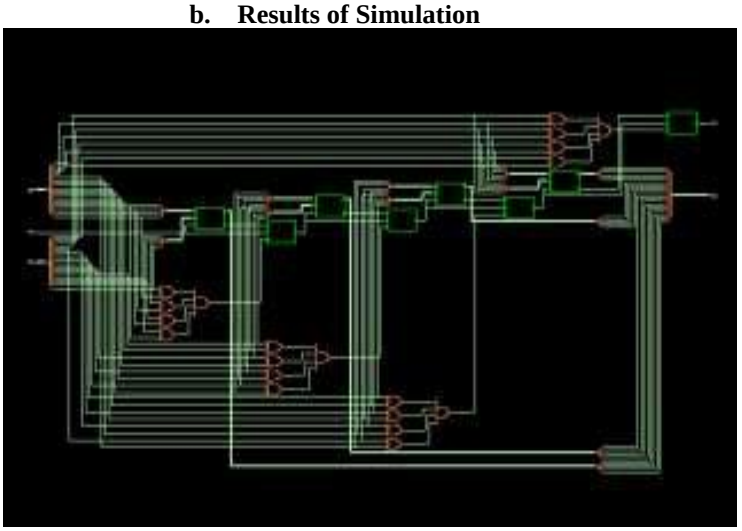

Fig.4: CONVENTIONAL CSKA for 16 bits

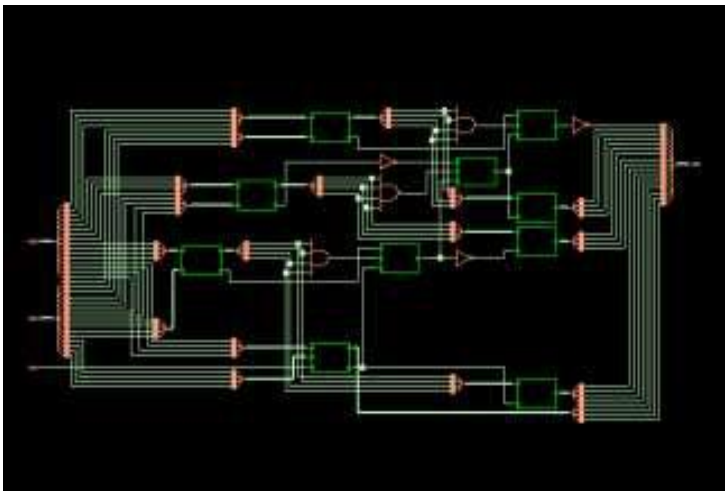

Fig.5: RTL schematic for four bit full adder RTL schematic

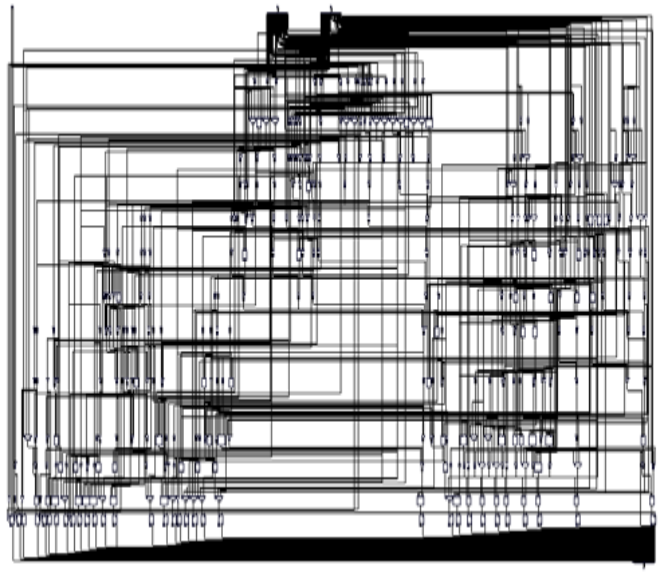

Fig.6: RTL schematic for complete circuit extension

V. CONLUSION

The conventional carry skip adder can be used to skip carry only if the input bits are in carry propagation condition. In CI-CSKA also the carry can be skipped only if the intermediate results are one. But the proposed structure can skip the carry if the input bits are in carry propagation or carry generation condition. The proposed CFF-CSKA architecture requires only 2-AND gates and one OR gate in addition to skip carry. CFF-CSKA is a speed optimized version of conventional CSKA. The second proposed model was CFF-CI-CSKA. This model incorporates many advantages and can be used for very high speed applications. But the extra circuit added with this architecture consumes large area. Analysis shows that the proposed models consumes more area and power but it has an improved timing. So it can be concluded that the proposed models can be used for high speed applications by the cost of area and power.The adder will have minimum EDP point at a voltage higherthan the transistor threshold. Design and evaluation of an 64-bit adder with minimum EDP point in the subthreshold regionis our future work

VI. REFERENCES

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