A Review on Ternary Adder and CNTFET in VLSI

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Abstract- Ternary logic is a promising solution to conventional VLSI binary logic as it offers the advantages of decreased interconnections, greater working speeds and lower chip area. This article introduces a couple of circuits to use carbon nanotube field impact transistors (CNTFETs) to implement a ternary half adder. Many studies are currently underway to design and explore the implementation of CNTFETs in logic gates and to mark their efficiency benefit over existing MOS technology. The implementation for the CNTFET circuit involves binary logic doors, ternary logic gate, ternary and binary memory cells and multi-appraised logics. One of the suggested ternaries to binary decoder circuits simplifies further execution of the circuit and offers great delay and energy benefits in information route circuits such as adder. These circuits were simulated widely using HSPICE to achieve the product strength, delay and energy delay.

Keywords- carbon nanotube field impact transistors, MOS technology, adder, ternary half adder, delay, energy delay

I. INTRODUCTION

Carbon nanotube (CNT), due to its unique structures and excellent physical properties, has attracted significant attention in the field of electronics for the last few decades. Currently, use of CNT in the channel region of a field effect transistor is in experimental phase to obtain a new device called carbon nanotube field effect transistor (CNTFET)[1]. Due to the limitations of CMOS transistors, they are not able to continue the process of feature size reduction and should be replaced by new alternative emerging technologies. CMOS transistors have problems such as short channel effect, reduced gate control, high leakage power and parameter variation [2]. Complementary Metal Oxide Semiconductor (CMOS) process has been the dominant technology, which provides the needed size scaling for implementing low-power, high-performance and high-density VLSI circuits and systems [3].

Therefore, a multithreshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in [3]. However, in this configuration, large OFF-chip resistors (of at least 100 MΩ values) are needed due to the current requirement of the CNTFETs. The design technique proposed in this paper relies on and eliminates the large resistors by employing active load with p-type CNTFETs in the ternary logic gates. In this paper, the multivalued logic design based on multithreshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs [4]. The alternative for the CMOS technology is the CNTFET. The similarity between CMOS and CNTFET in a device structure and principle operation, we can obtain the required CMOS manufacturing and CMOS design in the CNTFET technology [6].

II. LITERATURE REVIEW

The designs of basic ternary gates/operators (inverters, NAND, and NOR) are described in detail, and ternary full adder, and multiplier designs and analysis are presented as examples of the application of these ternary gates design technique. For the arithmetic circuit design, a modified ternary logic circuit design technique is used to speed up and reduce power consumption of the circuits. The modified ternary logic design uses both ternary logic gates and binary logic gates based on the previous ternary logic design structures to take advantage of the two logic design styles' merits. The ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation [1].

CNTFET:

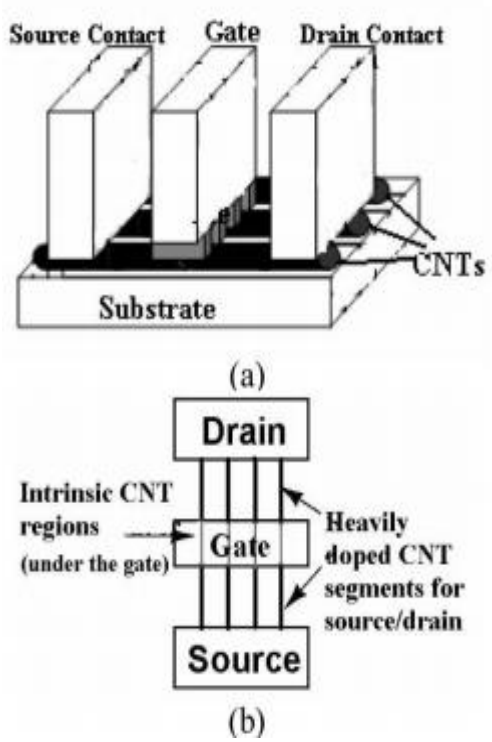

Fig.1: CNTFET (a) Schematic diagram (b) Top view

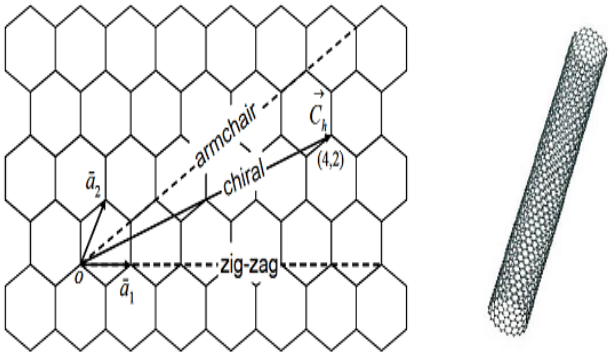

Fig.2: Unrolled graphite sheet and the rolled carbon nanotube lattice structure.

A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. First demonstrated in 1998, there have been major developments in CNTFETs [2] Single walled CNT (SWCNT) is made by rolling graphene sheet into cylindrical shape so that the structure is one-dimensional. SWCNT is used to design electronics devices [8] in CNTFETs. CNT has excellent chemical, mechanical, electrical property. The chemical bond in CNT consists of sp2 which provides it chemical strength. CNT is a good alternative since it provides carrier transportation in one-dimensional thereby suppressing the scattering effect and also it has low power dissipation. SWCNTs electrical property can be either metallic or semiconducting depending on its chirality. Chirality (n, m) is decided by the chiral angle at which graphene sheets are rolled [7]. To alleviate these difficulties, some beyond MOS nanodevices such as Carbon Nanotube Field Effect Transistor (CNTFET), Single Electron Transistor (SET), Graphene Nanoribbon Transistor (GNRT) and Quantum-dot Cellular Automata (QCA), the possible alternatives to replace the conventional bulk CMOS in the near future. However, considering all of these nanodevices, CNTFET could be more of an interest due to its similarities with MOSFET in terms of inherent electronic properties [8]. A suitable alternative for CMOS transistors is CNFET. Because of the similarities between CMOS and CNFET transistors in terms of inherent electronic parameters, CNFET could be a good alternative technology without any major changes in CMOS platforms [4]. In addition, a unique characteristic of CNFET devices is one dimensional band structure which suppresses backscattering and causes near ballistic operation, that makes it suitable for implementing fast and low power CNFET based circuits [8]. Scaling down the dimensions in Si FET is the necessity in modern era but situation like short channel effect where electron are transferred directly between source and drain restricts further scaling as such effect causes parameters variation [9]. Using CNTFET, a nanoelectronic device provides the way for scaling process. Voltage mode MVL circuits are achieved through multi threshold design [7]. In CMOS, multi threshold is obtained by altering voltage across bulk terminal while in CNTFET it can be achieved by just using different diameters [2].

Ternary Full-Adder: -

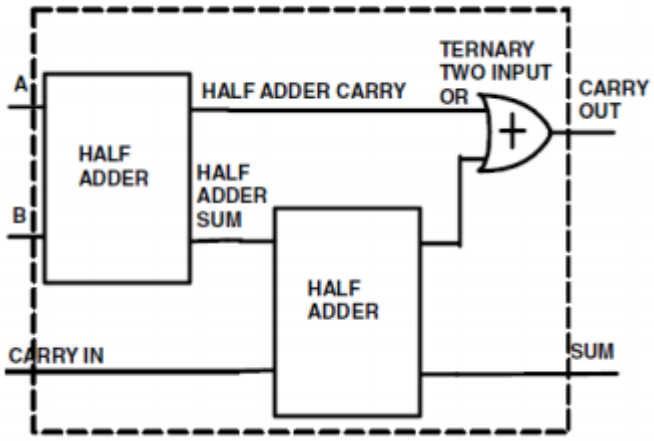

Fig.3: Ternary Full-Adder

A 1-bit ternary full adder adds two ternary numbers and previously calculated carry which here denoted as Cin. This circuit produces a 2-bit output sum represented by the signals Cout and SUM. A ternary full adder can be implemented by cascading two ternary half adder circuits. Fig.4 shows the ternary full adder block diagram using two ternary half adders block. Here the first half adder adds 2 input bits A and B. The following half adder adds the sum output of A and B inputs with past carry (Cin) and generates sum bit and one carry bit in its output. The final carry bit (Cout) is generated by the OR operation between the two carry bits generated from the two stages (first half adder and the second half adder) [9]. Carbon Nano Tube Field Effect Transistors (CNFET) are formed in the shape of a sheet of graphite tubes. Some advantages of CNFETs are such as they have higher ON current compared to MOSFET transistors. By using CNFETs it is possible to scale down feature size, beyond what currently lithographic methods permit. Also, ballistic conduction of CNFETs reduces the power dissipation in the transistor body. One-dimension structure of CNTs reduces the resistivity and consequently the energy dissipation and power consumption [10]. Carbon Nano Tube Field Effect Transistors (CNFET) are formed in the shape of a sheet of graphite tubes. Some advantages of CNFETs are such as they have higher ON current compared to MOSFET transistors. By using CNFETs it is possible to scale down feature size, beyond what currently lithographic methods permit. Also, ballistic conduction of CNFETs reduces the power dissipation in the transistor body. One-dimension structure of CNTs reduces the resistivity and consequently the energy dissipation and power consumption [2]. Full Adder is the basic element for arithmetic operations used in Very Large Scale Integrated (VLSI) circuits, therefore, optimization of 1-bit full adder cell improves the overall performance of electronic devices. Due to unique mechanical and electrical characteristics, carbon nanotube field effect transistors (CNTFET) are found to be the most suitable alternative for metal oxide field effect transistor (MOSFET). CNTFET

transistor utilizes carbon nanotube (CNT) in the channel region. In this paper, high speed, low power and reduced transistor count full adder cell using CNTFET 32nm technology is presented [3].]. Another feature of CNFET is that it has same mobility and consequently same current drive for P-FET and N-FET devices. This makes transistor sizing easier for complex circuits. Among all applications of CNFET transistors, Multiple Valued Logic (MVL) could be more of an interest. MVL logic means using more than two logic values for designing circuits and systems. Using CNFETs is appropriate for MVL designing. Because MVL is based on multiple threshold design technique and determining the threshold voltage of CNFETs is easily possible by changing the diameter of the nanotubes. One of the major challenges of binary logic is the number of pin counts and interconnects specially in dense chips. This problem limits the number of inside and outside connections. By using MVL, we can reduce the circuit area by reducing the overhead in interconnects and pin counts. In MVL designs, wires and interconnections carry more information than binary logic; so, it has higher speed and smaller number of computation stages [6]. Among all radices that exist for MVL logic, e (≈ 2.718) base operations have the most efficient implementation. But due to the hardware restrictions for implementing real systems, we should use natural numbers as the base of computations. So, radix 3 which is the nearest natural number to e; is more attractive ternary logic is the best and leads to less complexity and production cost [8]. The designs of basic ternary gates/operators (inverters, NAND, and NOR) are described in detail, and ternary full adder, and multiplier designs and analysis are presented as examples of the application of these ternary gates design technique. For the arithmetic circuit design, a modified ternary logic circuit design technique is used to speed up and reduce power consumption of the circuits. The modified ternary logic design uses both ternary logic gates and binary logic gates based on the previous ternary logic design structures to take advantage of the two logic design styles' merits [10]. Logic circuits as well as different adders, multipliers and memories are also designed to obtain less delay, lower power consumption and to have reduced interconnection complexity. Currently on-chip interconnections have become a serious challenge as more and more modules are packed into a chip. In a typical binary circuit chip, more of the area is occupied by interconnects, 20% for insulation and only 10% for transistors. These interconnects dissipate lots of energy, increase response time, and cause coupling effects by adding more capacitance, resistance, and inductance to a circuit [9].

III. CONCLUSION

Therefore, we researched High Performance Ternary Adder in this review article using CNTFET.in this method with many benefits such as area, delay, low energy, noise immunity. Using emerging futuristic CNTFET equipment, two enhanced circuits for ternary half adder. Based on HSPICE simulations, the circuit performance is contrasted with the best recorded half-adder circuit using Sandford's CNTFET compact model. Two novel high-performance ternary full adder cells have been proposed based on CNFETs. The proposed circuits have been designed based on multiple-Vth devices by utilizing unique characteristics of Ternary logic is a successful solution to standard VLSI binary logic because it offers the benefits of decreased interconnections, greater working speeds and a lower chip area, and Ternary logic is a successful option to standard binary logic. Due to the decreased overhead circuit such as interconnect and chip region, simplicity and power effectiveness can be achieved in contemporary digital architecture. CNFETs.

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