

# A Novel High Speed, Low Power Dynamic Comparator with High Noise Immunity

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**Abstract** - In this paper, a dynamic comparator design employing complementary metal-oxide-semiconductor logic is reported. The design was implemented using Tanner EDA tools in 0.18 $\mu$ m technology. Performance parameters such as power, delay and PDP (Power Delay Parameter) are compared with the exiting designs. For 1.2-V supply at 180nm technology, the average power consumption was found to be extremely low (620.3nW). Delay of dynamic and double tail dynamic comparator are (940ps) or (346ps) and PDP is (214.7a) and energy is (49.63f). In comparison with the exiting dynamic comparator designs, the present implementation was found to offer significant improvement in term of power and speed.

**Keywords:** Dynamic comparator, dynamic clocked comparator, power gating, high-speed analog-to-digital converters (ADCs).

## I. INTRODUCTION

Comparator is one of the fundamental building block in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area.

Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual oxide processes, which can handle higher supply voltages. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the dynamic comparator structure, a new double-tail dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors.

### Conventional Double-tail Dynamic Comparator:

The schematic diagram of the conventional dynamic comparator. It is widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption. In this operation of the comparator. During the reset phase when  $CLK = 0$  and  $M_{tail}$  is off, reset

transistors ( $M7-M8$ ) pull both output nodes  $Out_n$  and  $Out_p$  to  $VDD$  to define a start condition and to have a valid logical level during reset. In the comparison phase, when  $CLK = VDD$ , transistors  $M7$  and  $M8$  are off, and  $M_{tail}$  is on. Output voltages ( $Out_p$ ,  $Out_n$ ), which had been pre-charged to  $VDD$ , start to discharge with different discharging rates depending on the corresponding input voltage ( $INN/INP$ ). Assuming the case where  $V_{INP} > V_{INN}$ ,  $Out_p$  discharges faster than  $Out_n$ , hence when  $Out_p$  (discharged by transistor  $M2$  drain current), falls down to  $VDD - |V_{thp}|$  before  $Out_n$  (discharged by transistor  $M1$  drain current), the corresponding pMOS transistor ( $M5$ ) will turn on initiating the latch regeneration caused by back-to-back inverters ( $M3$ ,  $M5$  and  $M4$ ,  $M6$ ). Thus,  $Out_n$  pulls to  $VDD$  and  $Out_p$  discharges to ground. If  $V_{INP} < V_{INN}$ , the circuits works vice versa.

Base double tail comparator uses cross coupled PMOS to speed up the latch operation while addition of two NMOS transistor with input  $f_n$  and  $f_p$  use for power reduction as it gives direct discharge path to our circuit.

### Modified Double tail dynamic comparator:

The double tail comparator architecture is used in low voltage applications because of its better performance in delay reduction.

#### Operation:

The schematic diagram of double tail comparator. The operation of the double tail comparator occurs in two phase which are reset phase and decision making phase. During reset phase  $CLK=0$ ,  $M_{tail1}$  and  $M_{tail2}$  are in off state,  $M3$  and  $M4$  are in on state which pulls both the nodes  $f_n$  and  $f_p$  to  $VDD$ . so according to the input suppose  $V_{inp} > V_{inn}$ , then  $f_n$  drops faster than  $f_p$ . As long as  $f_n$  continues falling, the corresponding PMOS control transistor starts to turn on, pulling  $f_p$  node back to  $VDD$ . So another control transistor ( $M_{c2}$ ) remains off, allowing  $f_n$  to be discharged completely. The control transistor  $M_{c1}$  is on when  $M_{c2}$  is grounded which results in static power consumption so two more switches ( $M_{sw1}$  and  $M_{sw2}$ ) are added.

During the decision making phase the nodes  $f_n$  and  $f_p$  are pre charged to  $VDD$  and it starts its different discharging. As soon as the comparator detects that one of the  $f_n/f_p$  is discharging faster, control transistor will help to increase the voltage difference.

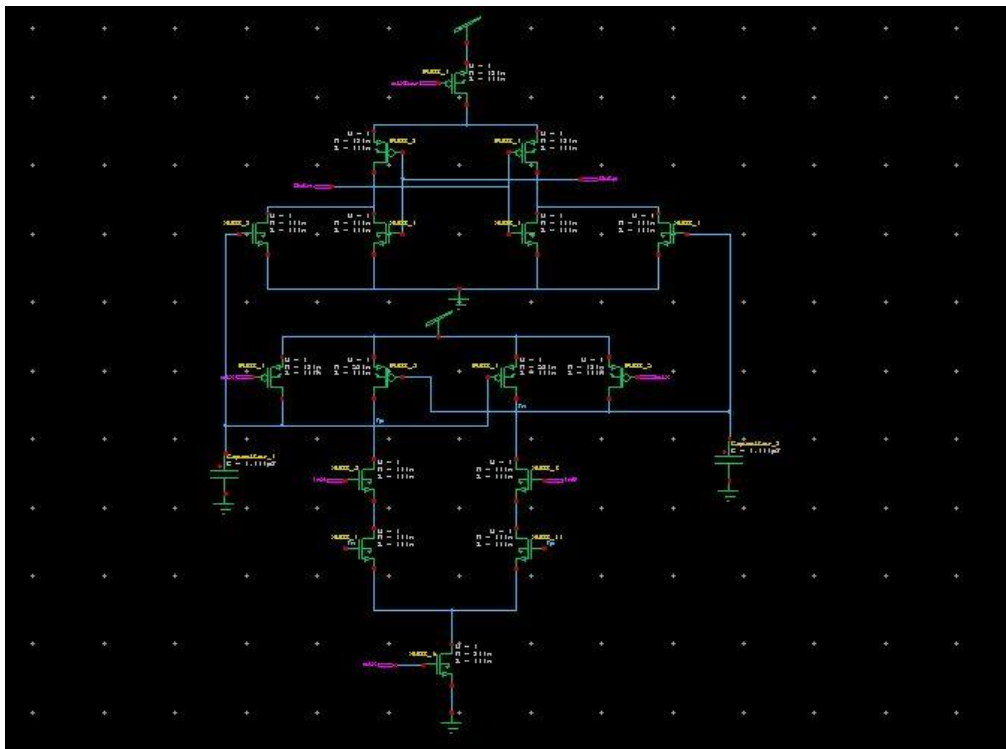


Fig. 1 Schematic diagram of the conventional dynamic comparator

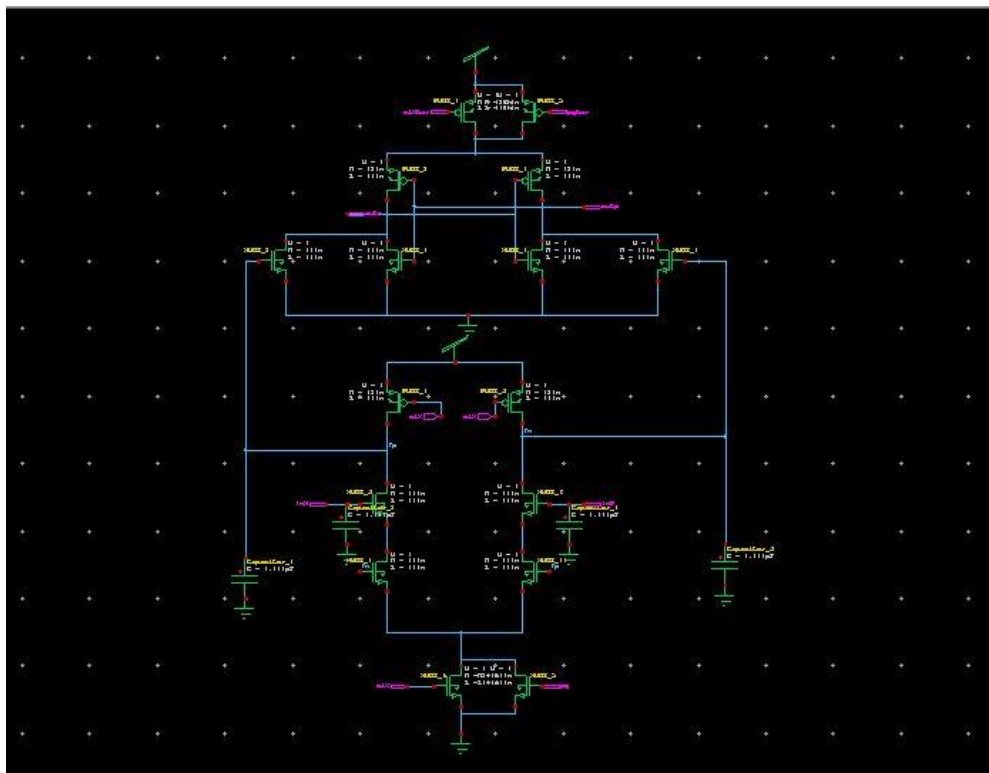


Fig.2 Schematic diagram of Modified dynamic comparator

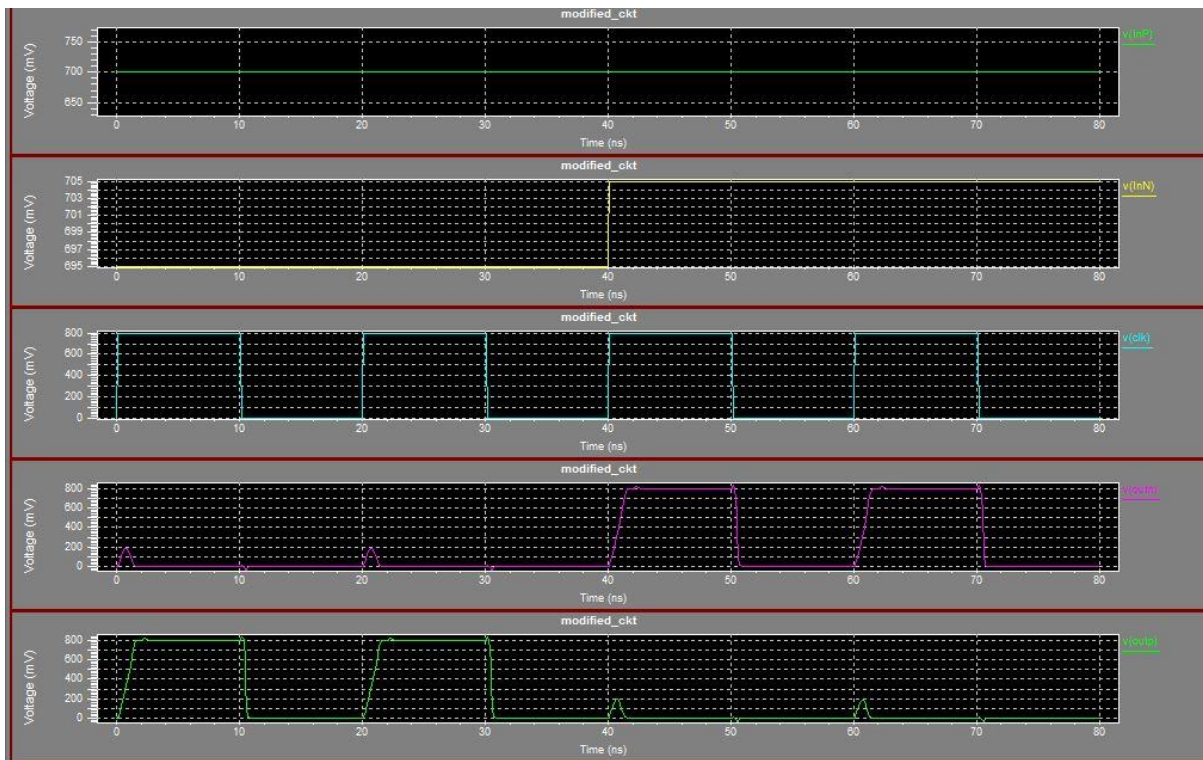


Fig.4 The output waveform of Modified dynamic comparator

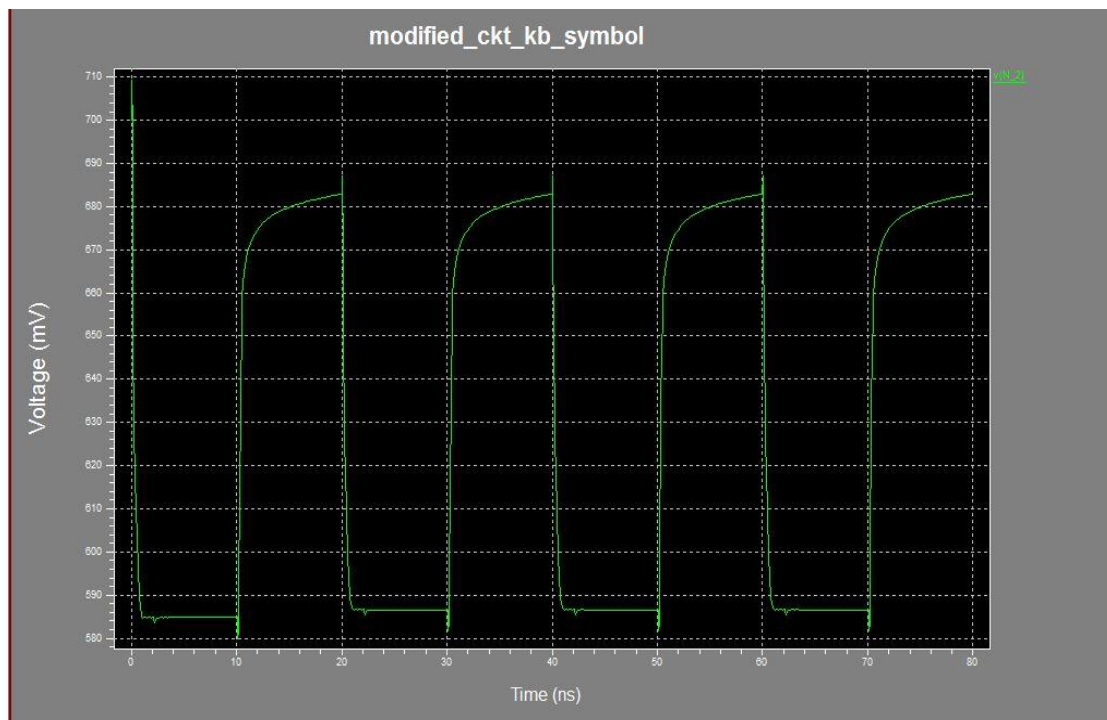


Fig.5 The output waveform of Kick Back of Modified dynamic comparator

## II. RESULTS

To analyse the performance of the structures we have simulated the circuits at 180nm technology and output is been observed which is presented in tabular format below. The power consumption, delay, PDP and energy of dynamic comparator and double tail dynamic comparator are obtained and compared with both the designs.

PARAMETERS	BASED PAPER DOUBLE - TAIL COMPERATOR	MODIFIED DOUBLE-TAIL COMPARATOR	Percentage Improvement
TECHNOLOGY	180nm	180nm	
APPLIED VOLTAGE	0.8v	0.8v	
POWER(nw)	904.58	761.48	15.81 %
DELAY(outp)(ns)	1.1577	0.8811	23.89 %
DELAY( outn) (ns)	1.1280	0.8749	22.43 %
PDP( outp) (fJ)	1.0472	0.6709	35.93 %
PDP( outpn) (fJ)	1.204	0.6662	44.66 %
ENERGY(fJ)	72.36	60.91	15.82 %
KICKBACK NOISE (mV)	14	4	71.42 %

## III. CONCLUSION

Both the design methodologies have been compared and it is evident that there is performance improvement in the proposed circuit. Double tail technique is an effective way to reduce power consumption and delay. All the designs have been simulated at Tanner EDA 14.1 version.

## IV. REFERENCES

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