Design and implementation multiplier using power gating with NBTI aging benefits

P.Sujatha[1] , L. Surendra[2]
[1]*Usha Rama college of engineering and technology,Telaprolu village, Krishna District, AP.*
[2]*Associate Professor, M.Tech, Usha Rama college of engineering and technology,Telaprolu village, Krishna District,AP*

Abstract-In this paper, we have a tendency to show that negative bias temperature instability (NBTI) aging of sleep transistors (STs), beside its prejudicial result for circuit performance and lifelong (LT), presents extensive edges for power-gated circuits. Indeed, it reduces static power as a result of leak current, and will increase ST switch potency, creating power gating a lot of economical and effective over time. The magnitude of those aging edges depends on operational and environmental conditions. We have a tendency to propose AN ST style strategy for reliable power gating, so as to reap the advantages offered by NBTI aging. It depends on the planning of STs with a correct lower Vth compared with the quality STs. this will be achieved by either redesigning the STs with the known Vth price orapplying a correct forward body bias to the onthe market power shift materials.

I. INTRODUCTION

As CMOS technology is scaled down, leakage power increases exponentially and thus has become a critical issue. An effective way to reduce leakage power is power gating [1], [2], [4]–[6]. This technique uses high-Vth transistors, called sleep transistors, to turn off the power supply, reducing leakage power in standby mode. There are two types of power gating designs: header- and footerbased designs, each of which use pMOS and nMOS as a sleep transistor. Because the sleep transistor behaves as a resistor, its width should be sufficiently large to avoid excessive IR-drop. Fig. 1(a) shows a footer-based design [1]. The circuit is divided into several smaller clusters, each with a pMOS header sleep transistor. However, the maximum instantaneous current (MIC) of a cluster may be large, resulting in large sleep transistor width. Long and He [6] proposed a distributed sleep transistor network (DSTN), as shown in Fig. 1(b), and sleep transistor sizing algorithms were proposed in [2]–[4] to reduce area overhead. Compared to the cluster-based design, this design connects all virtual ground (VGND) lines together. Therefore, the current can flow from one cluster to all sleep transistors, and a discharging current can be shared among the sleep transistors, reducing sleep transistor sizes. Note that the virtual ground also has wire resistance that cannot be ignored; therefore, an empirical parameter was used to replace the effect of the virtual ground resistance on a discharging current. However, this parameter cannot accurately model the effect of the virtual ground resistance. It utilizes transistors as power switches [also referred to as sleep transistors (STs)] to disconnect logic blocks from supply voltage during periods of inactivity. In particular, a header switch uses a high-Vth pMOS transistor to control Vdd, while a footer switch uses a high-Vth nMOS transistor to control Vss. Since header STs are more commonly used in commercial power-gated circuits [1], they will be considered in this paper. Along with power issues, electronic systems at nanoscale are increasingly suffering from reliability reduction [2]. In particular, they are prone to aging effects, which negatively impact circuit performance and long-term reliability. Among several aging effects, bias temperature instability (BTI) and hot carrier injection (HCI) are the two most important ones [3]. They cause an increase in transistor threshold voltage (Vth) over time, which leads to a performance degradation, and reduce their lifetime (LT) [3]–[6]. Positive BTI (PBTI) and HCI degrade the behavior of nMOS transistors, while negative BTI (NBTI) affects pMOS transistors [3]. NBTI is predominant over the PBTI and HCI, and is recognized as one of the primary parametric failure mechanisms for modern ICs [3], [5], [7]. Header STs degrade because of NBTI like any other pMOS transistor. Moreover, since they are always ON (under stress) when a power-gated circuit is operating, STs may suffer from an even higher degradation compared with functional transistors [8], [9].

II.PRELIMINARIES

A. BTI Model NBTI (PBTI)

Occurs when a pMOS (nMOS) transistor is under a negative (positive) bias voltage. The Vth drift of a pMOS (nMOS) transistor due to the static NBTI (PBTI) effect can be described by a direct-current (DC) reaction-diffusion (RD) framework. If a transistor is under alternating stress and recovery phases, the DC RD model.

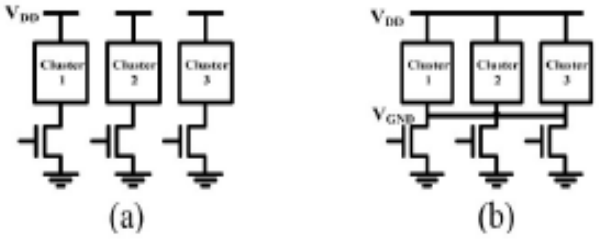

Fig.1Power gating structures. (a) Cluster-based. (b) DSTN designs.

B. Modified BTI-Aware Sleep Transistor Sizing Algorithm

The proposed algorithm, increase and decrease sizing (IDS), contains three steps, as shown in Fig. 3. VDEG is themaximum allowable IR-drop under the BTI effect. In step 1 (lines 1–4), the minimum initial width of the sleep transistors is determined. This is done by finding the minimum current of each cluster (line 2) and using (2) to calculate the initial sleep transistor width (line 3). Then, discharging matrix ϕ, MIC(STi, Tj), R(STi), and Slack(STi, Tj) are updated (line 4). Note that Slack(STi, Tj) is the voltage difference between VDEG and the voltage drop across the sleep transistor STi in the time frame Tj and is used to examine whether the VDEG constraint is met. MIC(STi, Tj)can be obtained using (4) by multiplying matrix ϕ and MIC(Ci, Tj).R(STi) is the obtained resistance for each sleep transistor. In step a pair of (lines 5–9), the breadth of the sleep transistors is hyperbolic till all Slack(STi, Tj) values ar adequate to or larger than zero. inline with the Slack(STi, Tj) values from step one, the smallest amount negative Slack(STi, Tj) price and therefore the corresponding sleep semiconductor device STi ar obtained (line 6). This suggests that the IR-drop within the case of this sleep semiconductor device is comparatively massive. Thus, the breadth of this sleep semiconductor device is initial hyperbolic. The rise magnitude relation is obtained from VDEG divided by the most important IR-drop of STi and is employed to enlarge STi (line 7). Once the adjustment, the new discharging matrix ϕ, MIC(STi, Tj), R(STi), and Slack(STi, Tj) ar updated (line 8). The loop is recurrent till all Slack(STi, Tj) values ar adequate to or larger than zero, which suggests that the VDEG constraint is glad. However, the sleep transistors is also large once the rise step. The decrease step is wont to cut back these over-sized sleep transistors.

III. BACKGROUND ON POWER GATING AND NBTI AGING

Power gating is one in every of the foremost effective static power reduction techniques for nanometre technologies. It depends on byselection powering down bound blocks within the chip that aren't getting used by inserting header STs asynchronous with the pull-up logic or footer STs asynchronous pull-down logic. This way, AN intermediate virtual Vdd or

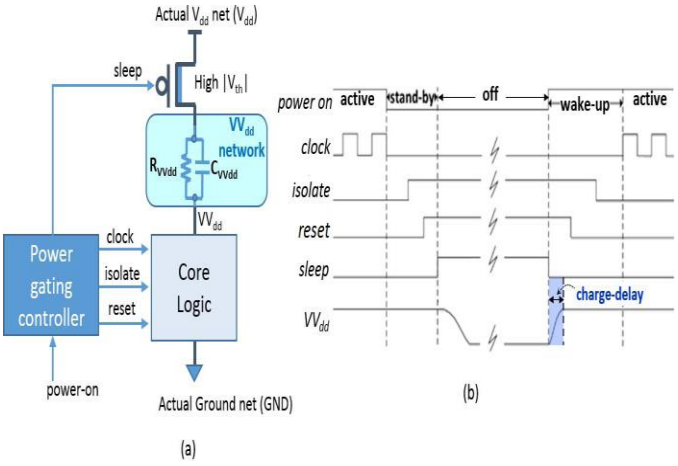

Fig.2 (a) Power-gating approach. (b) Power-gating protocol.

Virtual ground (GND) is formed. Header STs use high-Vth pMOS transistors to attach actual and virtual Vdd, whereasfooter STs use high-Vth nMOS transistors to attach actual and virtual GND. Footer nMOS STs ar generally utilized involtage scaling approaches However, they're expensive to style, since they need a triple-well CMOS method [1]. Header pMOS STs Exhibit a higher leak characteristic than nMOS transistors, and that they ar most

popular in styles, wherever leak constraints ar demanding. Moreover, their style is cheaper compared with nMOS STs, since the n-well is out there for bias sound within the normal CMOS method [1]. Therefore, the utilization of pMOS STs is preferred in commercial power-gated circuits, and will be considered in this paper. The general scheme using header STs is shown in Fig. 1(a), together with the stand-by and wake-up protocols, which are shown in Fig. 1(b) in the typical case where the power-gated core is equipped with clock-gating and isolation features [1].
IMPACT OF NBTI AGING OF SLEEP TRANSISTORS ON POWER-GATED CIRCUITS CHARACTERISTICS
In this section, we analyze the beneficial effects of ST NBTI aging on static power (during OFF mode) and on ST SwE,which is defined as: SwE = ION/IOFF [1]. We also observe static power reduction over time with an experiment conducted with an actual chip. Finally, the detrimental effects of ST NBTI aging on the propagation delay and LT (during active mode) of the power-gated logic and on the charge delay of VVdd network (during wake-up protocol) are also analyzed.

A. Simulation Setup

We consider the power-gating approach in Fig. 1(a) applied to two logic blocks: 1) the b02 benchmark from the itc99 benchmark suite and 2) a circuit composed by ten FO4 cascaded inverters. They are implemented with a 32-nm metal gate, high-k strained-Si CMOS technology [18], with a supply voltage Vdd = 1 V. Header pMOS STs are implemented by adopting a high-Vth model, while logic gates are designed using the low-Vth model. Logic gates are sized in order to be symmetric for the worst case delay. The VVdd network is modeled with a lumped RC circuit, whose parameters have been derived from [26]: RVVdd = 1_ and CVVdd = 5 fF for the b02 benchmark and CVVdd = 7 fF for the NOT chain. Note that the NOT chain is larger than the b02 benchmark and this area difference is reflected by the different values of the parasitic capacitance associated with the VVdd power network in the two case studies.In actual designs, power network is distributed [27] and switching logic is realized by means of many STs deployed throughout the system [28]. For the purpose of our analysis, since the VVdd network is modeled as a lumped RC circuit, we design the STs as a single, equivalent high-Vth pMOS transistor. If we considered multiple STs, they would be all in parallel with the same gate, drain, and source voltage values, and would be exposed to the same BTI degradation. Consequently, they would behave as a single, larger transistor. for every thought-about circuit, we have a tendency to verify the ratio of the STs so as to introduce AN IR drop adequate to zero.1 Vdd at t0. this is often a constraint typically adopted by the qualitypower-gating approaches neglecting th result of NBTI [1], [8], [12]–[14].

B. Power Switch NBTI Aging useful Effects

In this section, we have a tendency to assess the useful effects of ST NBTI aging on each the static power consumption and therefore the ST SwE, and that we show that power-gating techniques become a lot of efficient and effective over time.

1) Static Power: once a customary power-gating approach victimization high-Vth ST is applied, static power drops to sixty four.5 pW (b02 benchmark) and thirty five.1 pW(NOT chain), with a discount exceeding ninety fifth compared with a style while not power gating. These 2 values ar the number of static power that styleers expect to consume if a customary power-gating design flow (not accounting for NBTI) is taken into account. Therefore, they represent the particular style constraints for static power consumption. we have a tendency to ask these values as static power style constraint at t0, and that we denote them as SPDC0(b02) and SPDC0(NOT). leak current has 2 main contributors [1]: 1) subthreshold current and 2) gate current. The subthreshold current contribution dominates, since the gate current is well controlled by the utilization of high-k dielectrics. Therefore, onceAN ST is OFF, its leak.

IV. EXPERIMENT SETUP AND RESULTS

The algorithms are enforced in C/C+, and therefore the BTI model from is employed to get the Vth of the sleep transistors. The Benchmarks are from ISCAS eighty five and eighty nine, the simulation framework. RTL web lists are synthesized to gate level web lists, and therefore the SDF file is generated victimization style compiler. Infobahn lists ar then simulated to get the VCD file with ten 000 random patterns, and placement and routing ar done to get the situation of every gate and therefore the virtual ground resistance victimization SoC Encounter. supported the gate location, the gates in a very given row ar classified as a cluster. The MIC of every cluster is calculable victimization time and therefore the VCD file, and therefore the computer file containing time frames and current information is generated. Then, the time frames are partitioned based on the information contained in the output file and are designated as the inputs for the experiments.

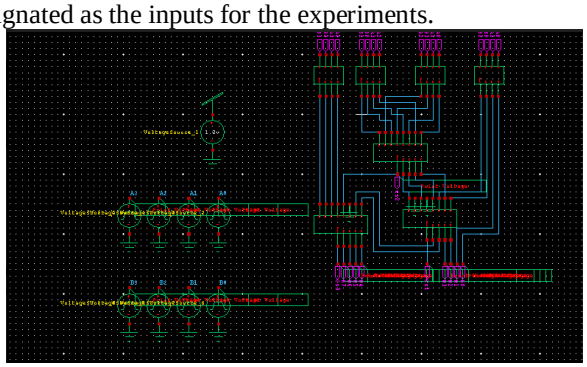

Fig.3proposedmul.PNG

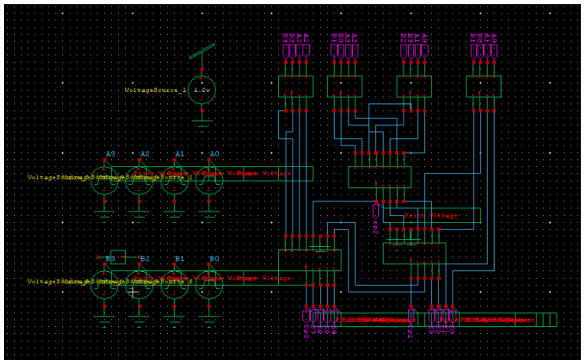

Fig.4 existingmul.PNG

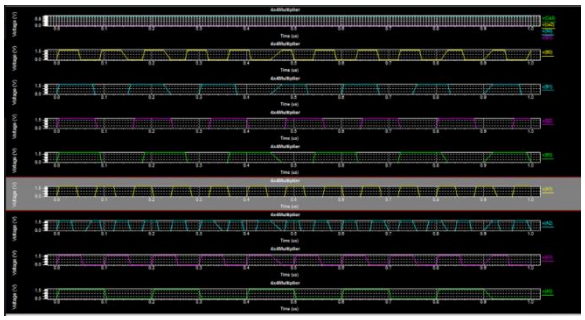

Fig.5 proposed wave form

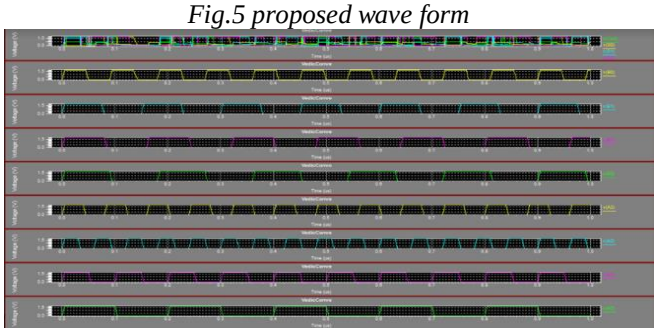

Fig.6 existingwaveform

V. CONCLUSION

In this paper, we showed that ST aging presents noticeable beneficial effects on static power and ST SwE, whose magnitudes depend on operating conditions. The beneficial effect on static power has also been proven by means of experimental measurements. Based on this feature, we proposed a new ST design strategy for reliable power gating, which offers better cost-reliability tradeoffs compared with alternative approaches based on either ST oversize or adaptive body bias. This paper proposed two sleep transistor sizing algorithms to reduce the total sleep transistor width under the BTI effect. A trade-off between runtime and sizing results can be made by choosing the proper algorithm. The total sleep transistor width obtained using the proposed algorithms when only the BTI effect on sleep transistors is considered was reduced.

VI. REFERENCES

[1]. M. Anis, S. Areibi, and M. Elmasry, "Design and optimization of multithreshold CMOS (MTCMOS) circuits," IEEE Trans. Comput.- Aided Design Integr. Circuits Syst., vol. 22, no. 10, pp. 1324–1342, Oct. 2003.

[2]. D. S. Chiou, D. C. Juan, Y. T. Chen, and S. C. Chang, "Fine-grained sleep transistor sizing algorithm for leakage power minimization," in Proc. 44th ACM/IEEE Design Autom. Conf. (DAC),San Diego, CA, USA, 2007, pp. 81–86.

[3]. D. S. Chiou, Y. T. Chen, D. C. Juan, and S. C. Chang, "Sleep transistor sizing in power gating designs," in Proc. 7th Int. Conf. ASICON, Guilin, China, 2007, pp. 1326–1331.

[4]. D. S. Chiou, Y. T. Chen, D. C. Juan, and S. C. Chang, "Sleep transistor sizing for leakage power minimization considering temporal correlation," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 8,pp. 1285–1289, Aug. 2010.

[5]. D. Flynn, R. Aitken, A. Gibbons, and K. Shi, Low Power Methodology Manual: For System-on-Chip Design. New York, NY, USA: Springer-Verlag, 2007.

[6]. (2013). The International Technology Roadmap for Semiconductors.[Online].Available:http://www.itrs.net/LINKS/ 2013ITRS/ Home2013.htm

[7]. H. Yi, T. Yoneda, M. Inoue, Y. Sato, S. Kajihara, and H. Fujiwara,"A failure prediction strategy for transistor aging," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 11, pp. 1951–1959, Nov. 2012.

[8]. S. Borkar, "Electronics on the far side nano-scale CMOS," in Proc. forty third IEEE/ACM style Autom. Conf. (DAC), Jul. 2006, pp. 807–808.

[9]. M. Agarwal et al., "Optimized circuit failure prediction for aging: utility and promise," in Proc. IEEE Int. Test Conf. (ITC), Oct. 2008, pp. 1–10.

[10]. M. Omaña, D. Rossi, N. Bosio, and C. Metra, "Low price NBTI degradation detection and masking approaches," IEEE Trans. Comput., vol. 62, no. 3, pp. 496–509, Mar. 2013.

[11]. W. Wang, Z. Wei, S. Yang, and Y. Cao, "An economical technique to spot essential gates below circuit aging,"in Proc. IEEE/ACM Int. Conf. Comput.-Aided style (ICCAD), Nov. 2007, pp. 735–740.

[12]. A. Calimera, E. Macii, and M. Poncino, "Design techniques for NBTI-tolerant power-gating architectures," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 4, pp. 249–253, Apr. 2012.