Low Power Optimization of GNRFET based 2 To 4 and 4 to 16 Mixed Logic Decoders

Jyoti Rani[1], Vishal Anand[2]

[1]*M.Tech Scholar, Department of Electronics and Communication, Punjab Technical University, Punjab, India*

[2]*Professor, Department of Electronics and Communication, Punjab Technical University, Punjab, India*

Abstract- In this paper, a mixed-logic design method with the use of GNRFET technology for line decoders 2 to 4 and 4 to 16 mode is proposed, combining the basic transmission gate logic, the pass transistor dual-value logic and base CMOS logic. To configurations are studied and analyzed which are 14T and 15T, 14T is for low power and low transistor count benefit and 15T is for high performance in terms of power and delay. GNRFET comes out to be excellent substitute of bulk MOSFET. Also, according to researchers the short channel effects are basically reduced in GNRFET, the results of the decoders are compared with the MOSFET counterpart. The technology nodes taken is 32nm as short channel effects increase the power consumption and unnecessary switching in the circuit. It is seen that the power, PDP and Voltage Source Power Dissipation are improved in the circuit by about 97%, 98% and 99% respectively with same but lower delays.

Keywords- *Decoder, GNRFET, Nano Ribbon, Power*.

I. INTRODUCTION

Static CMOS circuits are utilized for most by far of logic gates in incorporated circuits. [1] They comprise of correlative nMOS pull down and pMOS pull up systems and present great execution just as protection from commotion and gadget variety. In this way, CMOS logic is described by power against voltage scaling and transistor estimating and accordingly dependable task at low voltages and little transistor sizes. [2] Information signals are associated with transistor gates just, offering decreased plan unpredictability and assistance of cell-based logic blend and structure. Pass-transistor logic was primarily created during the 1990s, when different structure styles were presented, planning to give a feasible option to CMOS logic and improve speed, power and zone. [3][4] Its primary plan distinction is that inputs are connected to both the gates and the source/drain dispersion terminals of transistors. Pass transistor circuits are actualized with either individual nMOS/pMOS pass transistors or parallel sets of nMOS and pMOS called transmission gates. This work builds up a mixed-logic plan approach for line decoders, joining gates of various logic to a similar circuit, with an end goal to get improved execution contrasted with single-style structure. [5] Line decoders are major circuits, generally utilized in the fringe hardware of memory exhibits (for example SRAM), multiplexing structures, usage of Boolean logic capacities and different applications. Regardless of their significance, a generally little measure of writing is devoted to their streamlining, with some ongoing work including and a method to propose a better technique is presented. [6][11]

II. GNRFET AND DECODERS

GNRFETs are a vital advance in the development of semiconductors since mass CMOS experiences issues in scaling past 32 nm. Utilization of the back gate prompts very intriguing plan openings. [7] Rich decent variety of configuration styles, made conceivable by free control of GNRFET gates, can be utilized successfully to decrease absolute dynamic power utilization IG/LP mode circuits give an empowering tradeoff among power and zone. In these theories, 2:4 decoders is talked about with 14 transistor and 15 transistor LP, LPI, HP and HPI in present situation, power decrease is a noteworthy issue in the technology world. The low power configuration is serious issue in superior computerized framework, [1][8] for example, chip, advanced flag processors (DSPs) and different applications. The chip thickness and higher working pace prompts the arrangement of astoundingly complex chips with high clock frequencies. In this way, arranging of low power VLSI circuits is a mechanical need in these in light of the prominence for minimized buyer machines gadget. [12] [10] In a microchip/microcontroller-based system, the most customarily used square is the bearing set decoder. In this way; it will be not wrong in case we state the bearing set decoder uses more power. Along these lines overhauling the vitality of this square will be valuable to diminish the general power use of the system. Along these lines, proposed plan for this theory is the utilization of GNRFET system to diminish power utilization of guidance decoder. [14][15] In this proposition, we have proposed the structure of 2:4 decoder with the utilization of GNRFET logic to lessen the power of the decoder and subsequently will help in power decrease of generally framework.

III. SIMULATION RESULTS

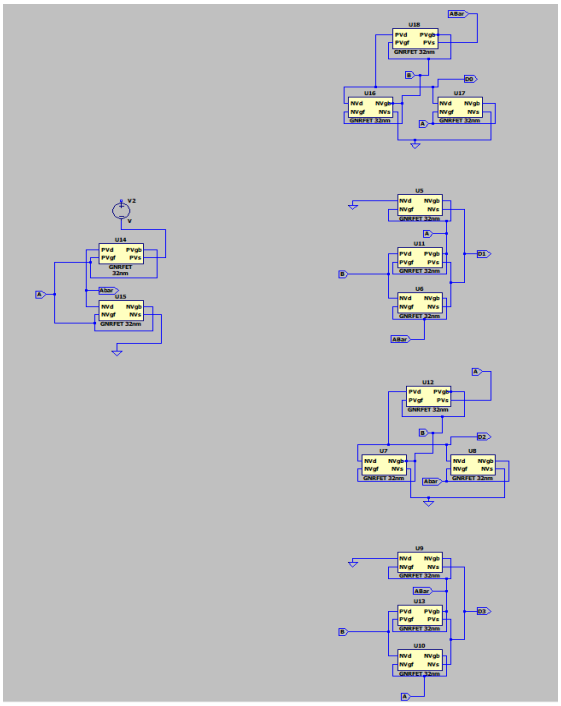

Fig.1: Two-input 2 to 4 decoder using GNRFET

Figure 1 shows a two input 2 to 4 decoder using GNRFET Technology in 32nm in MOS like GNRFET Mode. In short gate mode the back gate is connected to the front gate. The main important parameters in logic circuit design are Tox which is dieclectric thickness, sp spacing between GNRs, p is edge roughness and nrib which is number of ribbons.

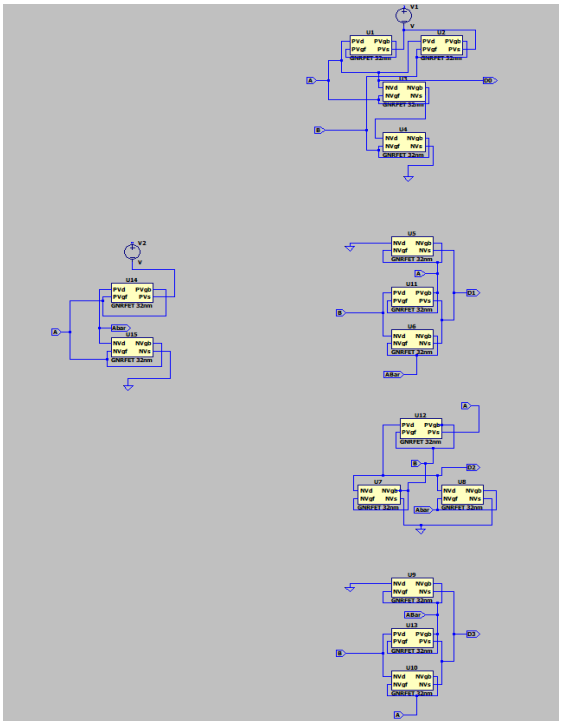

Fig.2: Two-input 2 to 4 decoder Technique using GNRFET

Figure 2 shows a two input 2 to 4 decoder using GNRFET Technology in 32nm in MOS like GNRFET Mode. This figure is for the 15 T in which the DO part is basically in CMOS logic and others in DVL/TGL mixed valued logics.

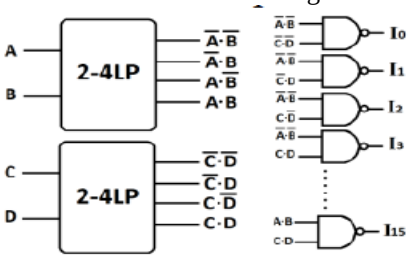

Fig.3: Proposed 4 to 16 decoder based on GNRFET

Figure 3 shows Proposed 4 to 16 decoder based on GNRFET Technology. The short gate decoders in 14t and 15t mode are then used for making inverted 4 to 16 decoder based on GNRFETs, as seen in the figure 3 and 4 the NAND gates are used in cmos logic for GNRFETs. To obtain the 16 outputs I0 to I16.

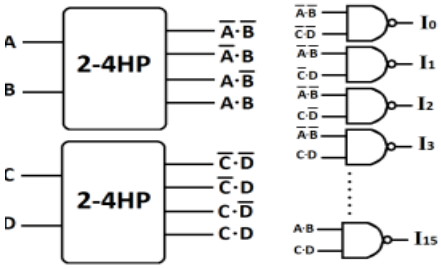

Fig.4: Proposed 4 to 16 decoder based on GNRFET

Figure 4 shows Proposed 4 to 16 decoder based on GNRFET Technology in High Performance mode, the working is same as of the MOSFET counterpart as discussed earlier.

IV. SIMULATION RESULTS

Figure 5, 6 shows the Average Power Comparison and Delay Comparison between different techniques as mentioned below in the figure. It shows the improvement in GNRFET based circuits.

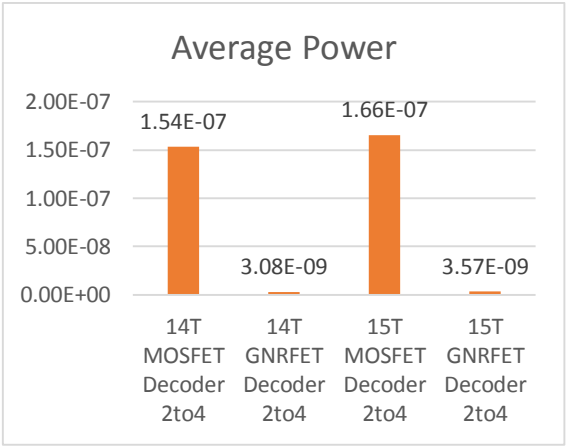

Fig.5: Average power in between 14T MOSFET Decoder 2 to 4 to 15 T GNRFET Decoder 2 to 4

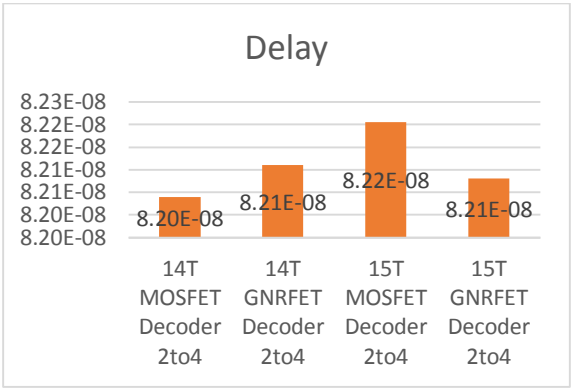

Fig.6: Delay in between 14T MOSFET Decoder 2 to 4 to 15 T GNRFET Decoder 2 to 4

In Figure 7 and Figure 8 shows the comparison of PDP and Voltage Source Power Dissipation of the circuits in 14T and 15T modes shows lower values in GNRFET based circuits showing significant improvement in the circuits.

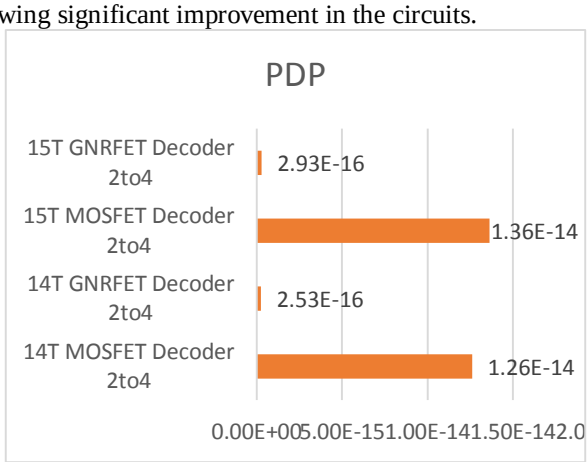

Fig.7: PDP in between 14T MOSFET Decoder 2 to 4 to 15 T GNRFET Decoder 2 to 4

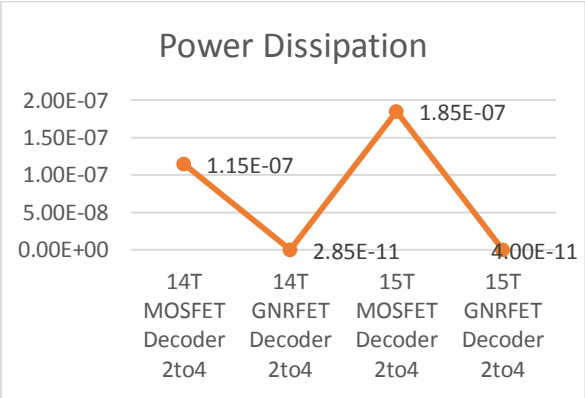

Fig.8: POWER DISSIPATION in between 14T MOSFET Decoder 2 to 4 to 15 T GNRFET Decoder 2 to 4

Now, similarly in Figure 9 and Figure 10 shows the improvement in 4 to 16 GNRFET circuits based on Average Power Consumption and Delay.

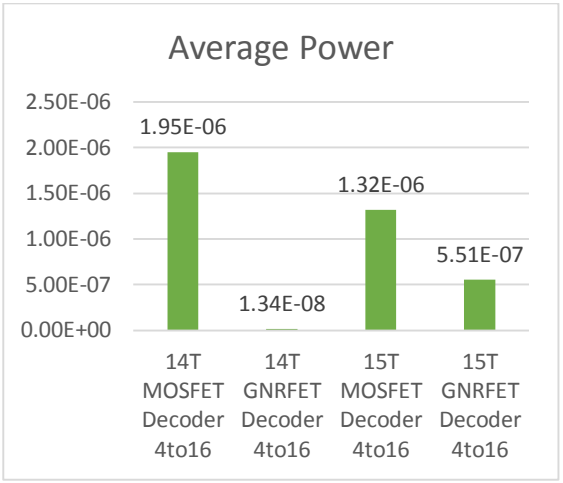

Fig.9: Average power in between 14T MOSFET Decoder 4 to 16 to 15 T GNRFET Decoder 4 to 16

In table 1, all results are shown in tabulated form.

Table 1: simulation result

	14T MOSFET Decoder 2to4	**14T GNRFET Decoder 2to4**	**15T MOSFET Decoder 2to4**	**15T GNRFET Decoder 2to4**
Average Power	1.54E-07	3.08E-09	1.66E-07	3.57E-09
Delay	8.20E-08	8.21E-08	8.22E-08	8.21E-08
PDP	1.26E-14	2.53E-16	1.36E-14	2.93E-16
Power Dissipation	1.15E-07	2.85E-11	1.85E-07	00E-11
	14T MOSFET Decoder 4to16	**14T GNRFET Decoder 4to16**	**15T MOSFET Decoder 4to16**	**15T GNRFET Decoder 4to16**
Average Power	1.95E-06	1.34E-08	1.32E-06	5.51E-07
Delay	8.11E-08	8.18E-08	7.84E-08	8.18E-08
PDP	1.58E-13	1.10E-15	1.03E-13	51E-14
Power Dissipation	8.61E-07	12E-10	5.48E-07	35E-10

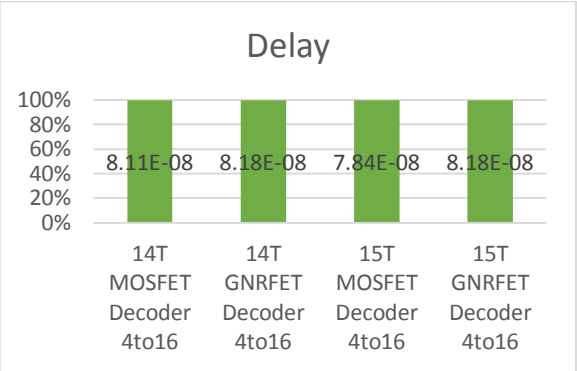

Fig.10: Delay in between 14T MOSFET Decoder 4 to 16 to 15 T GNRFET Decoder 4 to 16

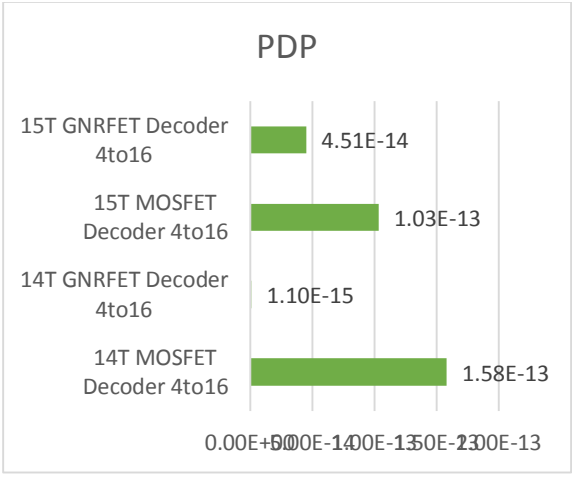

Fig.11: PDP in between 14T MOSFET Decoder 4 to 16 to 15 T GNRFET Decoder 4 to 16

In above Figure 11 and below Figure 12 PDP and Voltage source power dissipation are shown compared to the Mos counter circuits.

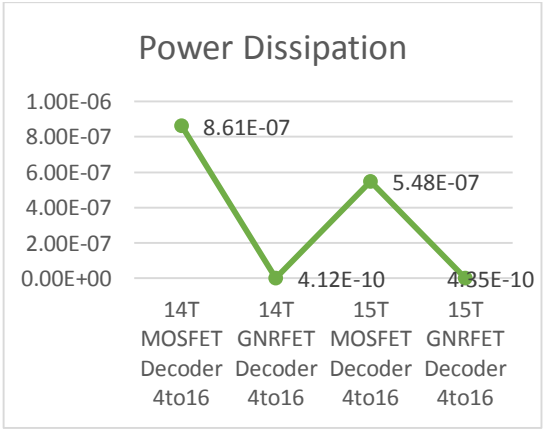

Fig.12: POWER DISSIPATION 14T MOSFET Decoder 4 to 16 to 15 T GNRFET Decoder 4 to 16

V. CONCLUSION

The use of GNRFET over MOSFET in the proposed technique reduces Average Power consumption; it indicated that GNRFET is a promising substitute for MOSFET beyond 32nm technology. The reduced short channel effects in GNRFET and better control over the gate of the GNRFET improves the Average Power in designed techniques.

VI. REFERENCES

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