Optimization of A Ternary Half Adder using Shorted Gate FINEFT Technology in 32nm

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Abstract- In This paper, a Low Power and Low Delay Based Ternary Half Adder Using FINFET Technology. In this paper, we are designing ternary adder using CNTFET and FinFET Technology and different adder circuit sum circuits and ternary decoder circuit are used. Here we are using N Channel P channel FinFET in shorted gate mode in 32nm technology. The FinFET is used in all ternary adder circuit and then a comparative analysis is performed to find the PDP, leakage power, average power and delay of the proposed system and these values are compared with ternary adder CNTFET. Nowadays as small portable devices consuming is largely increased, we can use the low power approaches are considerably taking into account. This improves the speed and power performance of the ternary adder.

Keywords- Ternary Adder, Fin Type FET, NFIN, HFIN

I. INTRODUCTION

As per Moore's law the quantity of transistors on a chip will be multiplied about like clockwork. [1][2]For this reason we need to shrivel the extent of the transistor into nano-scale locale. Because of the restrictions of silicon-based Field Effect Transistors (FETs), finding an appropriate option is significant. [3] As transistors are downsized to nanometer, various nano-scale material, for example, carbon nanotubes as a swap for silicon base gadgets. [4]To find a swap for the CMOS innovation numerous gadgets and strategies are considered by analysts, for example, Quantum-dab Cellular Automata (QCA), turn wave engineering, Single electron gadgets, Quantum processing, and so forth.[5][6] Carbon Nanotube Field Effect Transistor (CNTFET) is one of the rising components of nanoelectronics that has the preferable presentation over all the best in class rising innovation. Also, FinFET is another promising technology. [7] Here in this paper we compare a ternary half adder CNTFET based with a proposed work ternary half adder using FinFET and its performance is improved by varying the NFIN, HFIN and TFIN parameters. The ternary adder block diagram is shown in figure 1.

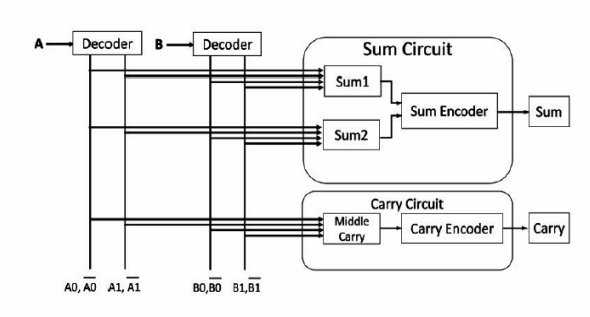

Fig.1: Ternary Half Adder

The circuits for ternary decoder, sum circuit and carry circuit are shown in figure 2 to 4 below.

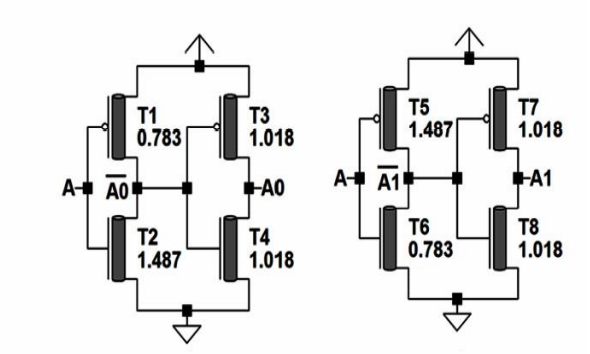

Fig.2: Ternary decoder circuit

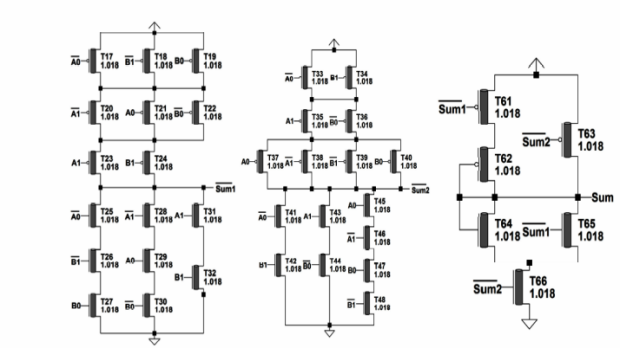

Fig.3: Ternary sum circuit

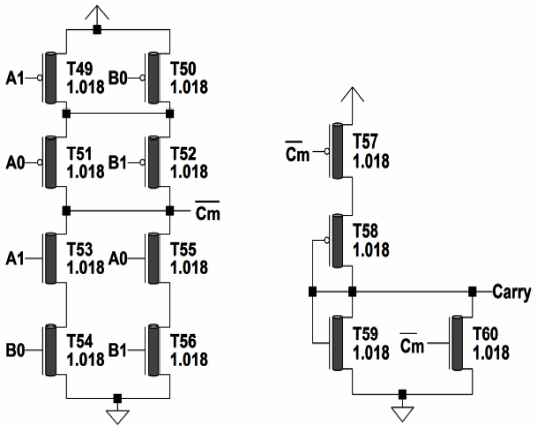

Fig.4: Ternary carry circuit

Implementations:

The circuits from figure 2 to 4 are implemented on 32nm CNTFET and FinFET, for the proposed FinFET based circuit the NFIN, HFIN and TFIN is varied in such a way that it gives better power and delay and hence EDP and PDP is also improved. In our proposed work HFIN is 9nm and TFIN is 7nm and NFIN is 1 for better optimization. The results are simulated in Synopsys HSPICE.

FinFET gadgets can be utilized to build the exhibition by diminishing the spillage current and power dispersal, since front and back gates both can be controlled autonomously or both at the same time.

The viable width of a FinFET gadget is quantized because of the vertical gate structure. The fin stature decides the base width with the two gates integrated, Wmin is given by,

Wmin = 2.Hfin + tsi

Where, Hfin is fin stature and tsi is the thickness of silicon body. Ordinarily, the fin thickness is kept littler than the fin stature to decrease the short channel impacts. The FinFET tallness Hfin, together with the fin pitch (controlled by photolithography) defines the FinFET gadget width Wfin inside the given silicon width of the planar gadget, to show signs of improvement gadget quality The key advantages of FinFET innovation over MOSFET incorporates low off flows, higher on flows, lower normal power utilization and diminishes short channel impacts (SCEs).

Research gatherings and organizations, for example, Intel, IBM, have appeared in creating comparative gadgets, just as instruments to relocate veil designs from mass MOSFET to FinFET.

II. RESULTS

Figure 5 to 10 all results are explanation are presented.

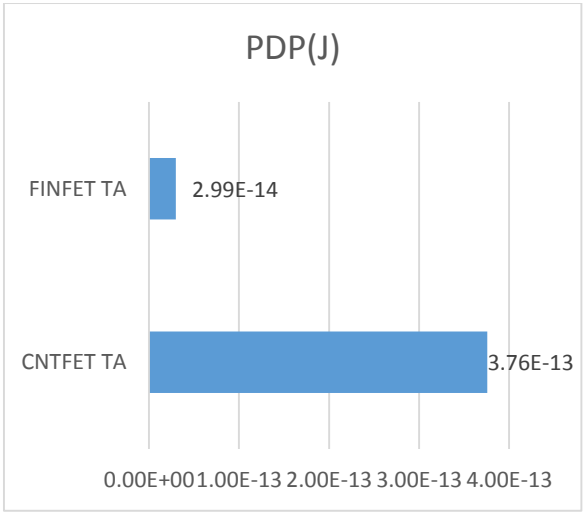

Fig.5: PDP of proposed system

The figure 5 shows the PDP of proposed system. here comparing the ternary adder CNTFET and ternary adder FinFET, here the PDP is the low in ternary adder FinFET compare to ternary adder CNTFET.

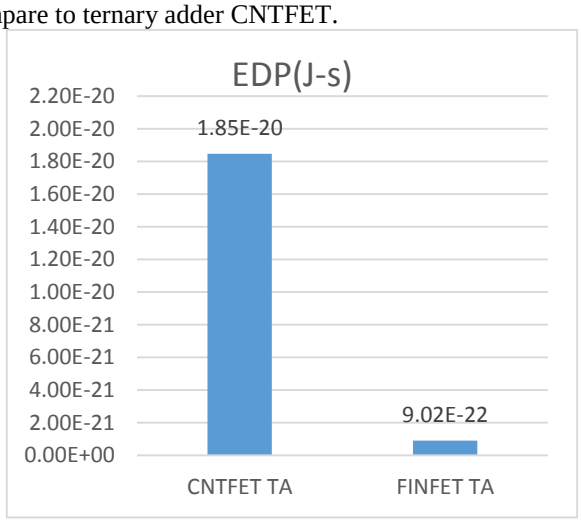

Fig.6: EDP of proposed system

The figure 6 shows the EDP of proposed system, here the leakage delay is low in ternary adder FinFET compare to ternary adder CNTFET.

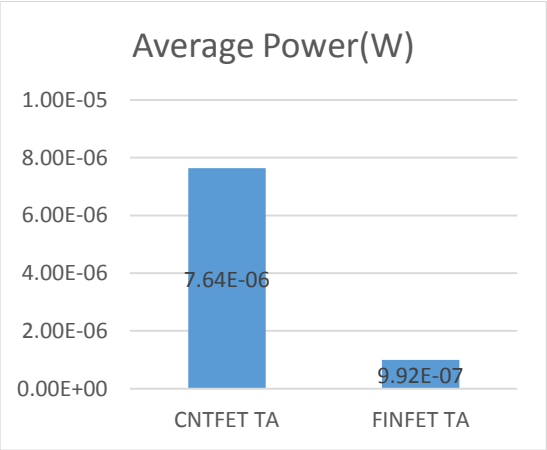

Fig.7: average power of proposed system

The average power of proposed system, the average delay is low in ternary adder FinFET compare to ternary adder CNTFET and it is shown in above figure 7.

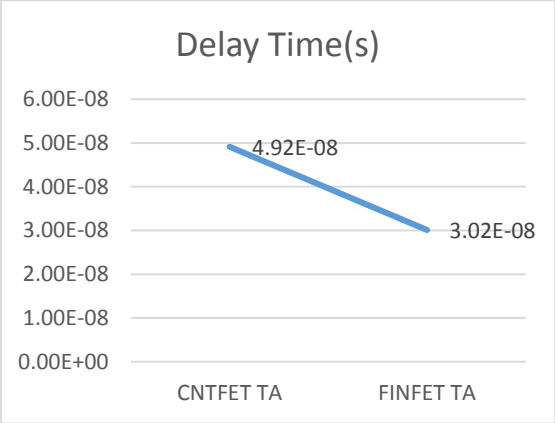

Fig.8: Delay of proposed system

The above figure 8 shows the delay of proposed system graph diagram, it shows the delay value of ternary adder CNTFET and ternary adder FinFET. The delay value is same in ternary adder CNTFET and ternary adder FinFET.

Table 1: Simulation Result

	Ternary Adder Technology Used	
Output Parameter Observed	CNTFET TA	FINFET TA
Average Power(W)	7.64E-06	9.92E-07
Delay Time(s)	4.92E-08	3.02E-08
PDP(J)	3.76E-13	2.99E-14
EDP(J-s)	1.85E-20	9.02E-22

The above table 1 shows the different parameter comparison in ternary adder CNTFET and ternary adder FinFET. Here we can see the average power, delay, PDP and EDP values of Ternary Adder CNTFET and Ternary Adder FinFET.

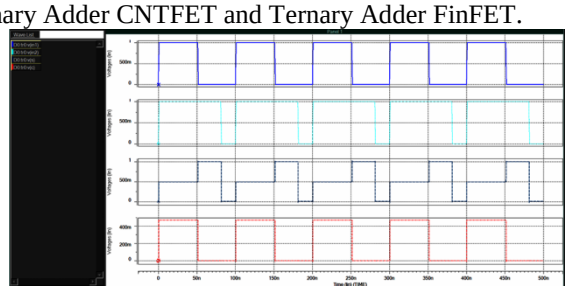

Fig.9: Waveform of CNTFET based Ternary Adder

The above figure 9 shows the waveform of CNTFET ternary Adder

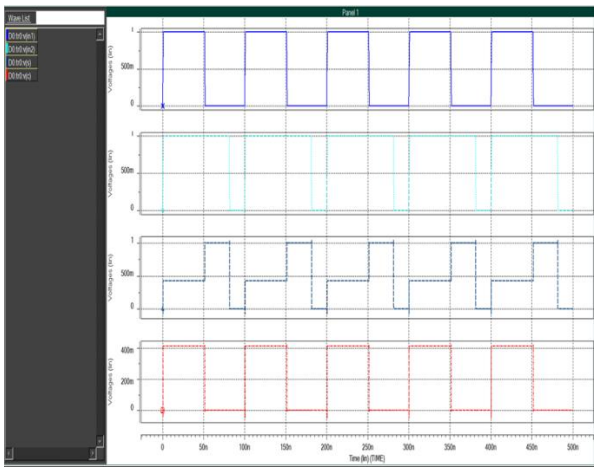

Fig.10: Waveform of FinFET based Ternary Adder

The figure 10 shows the waveform of FinFET ternary Adder.

III. CONCLUSION

Hence here we are studied and designed on HSPICE simulations a Low Power and Low Delay Based Ternary Half Adder Using FINFET Technology. Here we are using different ternary adder circuit using N channel and P channel FinFET. In this study we are compared ternary adder CNTFET and ternary adder FinFET. We are finding the values of PDP, EDP, average power and delay and comparing PDP, EDP, average power and delay of ternary adder CNTFET and ternary adder FinFET. Here we can see the low values are getting ternary adder FinFET compared to ternary adder CNTFET. static power consumption reaches its minimum amount. Extensive different analyses have been carried out to examine efficiency in all aspects. Simulation results are demonstrated that we have achieved the efficient circuit design parameters such as power consumption and power-delay product.

IV. REFERENCES

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