Design of Voltage Regulator for High Speed Applications

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Abstract- This paper gives a solution to enhance the transient behavior of a voltage regulator. A voltage regulator works as a power efficient way of stepping down an external supply voltage to the desired internal core supply voltage. The most important and critical block of a voltage regulator is the final output stage (i.e. driver stage). For a good transient response performance, the driver stage must have reasonably good bandwidth, which is obtained by adding dynamic leaker at the driver stage. It is designed in Cadence Virtuoso Schematic Editor and simulated by using Cadence Virtuoso Spectre Circuit Simulator tool targeted to be fabricated on TSMC 0.18µ process. The voltage regulator generates 1.9v from 3.3v external supply and the load current varies from few hundred mA to close to zero mA. The proposed circuit is particularly useful for low power high speed applications.

Keywords- Bandgap reference, Error Amplifier, Cadence, Transient, simulation.

I. INTRODUCTION

The present research relates generally to high performance voltage regulator designs, and more particularly pertains to high performance voltage regulator designs which have settling times which are fast enough to meet today's microprocessor/ microcontroller requirements [1] when they are entering an active mode from a passive mode. A chip with a voltage regulator can be operated with a single external power supply. More than one level of internal power supply voltage can be generated for different applications in different operating modes. Using a lower power supply voltage reduces power consumption by the circuit. Moreover, a voltage regulator regulates the supply voltage such that it becomes relatively insensitive to external power variations.

Voltage regulator is more suitable for microprocessor/ microcontroller applications because its internal voltage supply is regulated by a differential amplifier. When entering an active mode, a microprocessor/microcontroller will instantly draw a large amount of current. It typically takes more than 3 clock cycles for the voltage regulator to settle the internal voltage. A voltage regulator is provided for controlling a voltage generator which produces a boost voltage across a charge reservoir for supply to one input of a plurality of word line drivers in a memory array.

The voltage regulator includes a bandgap reference generator, a first differential circuit[2],[3] for producing a transition voltage from the reference voltage and the power supply voltage, a first transistor for comparing the power supply voltage with the boost voltage, a second transistor for comparing the transition voltage with the reference voltage and a latching comparator for equating the signal outputs from the first and second transistors so as to define a control signal for the voltage generator. Along with further specific details of the voltage regulator, a preferred bandgap reference generator is described.

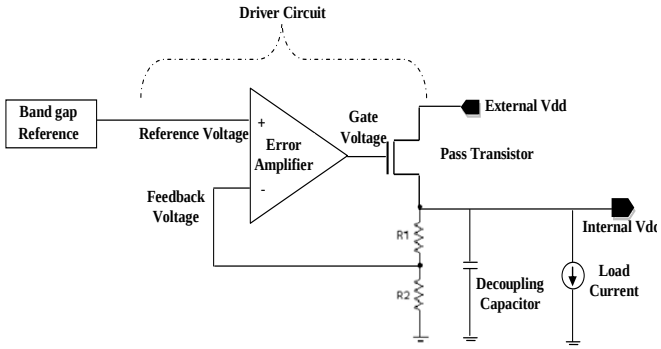

Fig.1: Block diagram of Voltage Regulator

Voltage regulator block diagram is shown in figure1. The main blocks of a voltage regulator are bandgap reference circuit followed by the driver circuit. The bandgap reference generates a temperature compensated stable reference voltage. The driver circuit consists of an error amplifier (i.e. a gain stage in the feedback loop) and cmos pass transistor. The amount of de-coupling capacitor available in regulator is less due to area constraint.

In general for high speed applications the circuit runs at high frequencies and the circuit transit from one mode to another mode in a fraction of nanoseconds time. So, the load current of the regulator also varies from few hundred mA to almost zero mA in a fraction of nanoseconds time. At negative temperatures zero mA load current is possible, where the circuit leakage current is almost negligible. In that condition, whenever the circuit switches from select mode to deselect mode, the pass transistor turns off, for a small duration of time, due to voltage fall in the gate voltage node. If the circuit switches again to the select mode, during the time when nmos pass transistor is off, internal Vdd falls much below than its specified lower limit. To eliminate this problem, dynamic leaker circuit is added at the internal Vdd node to obtain fast transient response.

II. DESIGN OF REFERENCE GENERATOR

Many integrated circuits require a stable reference voltage for their operation. Bandgap-voltage references are commonly used

voltage references in such integrated circuits. Bandgap voltage references can operate with a lower supply voltage and also dissipate less power. Unfortunately, the output voltage of a bandgap voltage reference is more dependent upon temperature and this factor becomes important if the integrated circuit is to be subjected to a wide range of temperatures.

A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits[3], usually with an output voltage around 1.25 volts, close to the theoretical bandgap of silicon at 0 K.

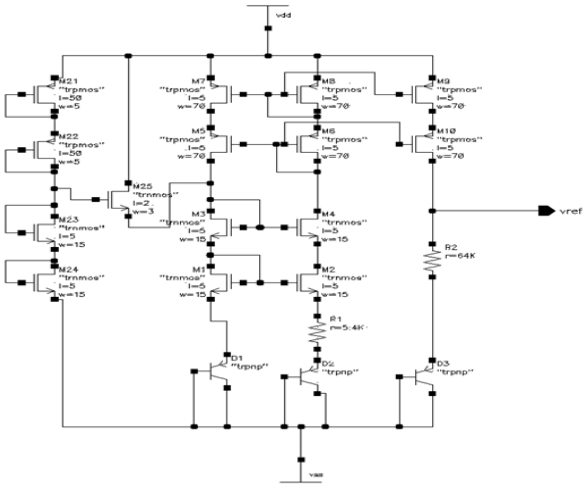

Fig.2: Bandgap Voltage Reference Circuit

Bandgap Voltage Reference Circuit the cascode connection of M1 through M8 forces the same current through D1 and D2. Where D2 has an emitter area K times larger than D1.in this configuration, the voltage across D1 must be equal to the voltage across D2 and R, or

$$V_{d1}=IR+V_{d2} \text{ ……. [1]}$$

We know that

$$I_{d1}=I_s e^{Vd1/nVT} \rightarrow V_{d1}=nV_T.\ln (I/I_s) \text{…….. [2]}$$

And

$$I_{d2}=K.I_s e^{Vd2/nVT} \rightarrow V_{d2}=nV_T.\ln (I/K.I_s) \text{.. [3]}$$

Solving for R in terms of the reference current I results in

$$R = \frac{nVT.\ln K}{I} \quad \text{or} \quad I = \frac{n.K.\ln K}{qR}.T \text{ ...……. [4]}$$

Notice that the current is proportional to the absolute temperature. For K=8 and n=1 the voltage drop across R is only 54 mV. Mismatches the gate-source voltages of M1 and M2 can result in large variations in current when using this scheme. Generally, M1 and M2 are made large for better matching of the IV characteristics. We should also keep in mind that the resistance value R may change up to 20% from wafer to wafer. If a precise current is needed, some sort of on-die tuning is required. More often, however, we care more about the relative current levels and temperature changes on a given die than about the die-to-die relative current levels.

The diode D3 is the same size as D2, while the resistor in series with D3 is L times larger than the resistor in series with D2. The current

$$I = \frac{nVT.\ln K}{R} \text{ ..…… [5]}$$

The reference output voltage with respect to Vss is given by

$$V_{ref} = I.L.R+V_{d3} \text{ ..…….. [6]}$$

The TC of the bandgap reference is zero when

$$\frac{\partial Vref}{\partial T} = 0 \text{ ……. [7]}$$

This is true when

$$L.n.\ln K = 23.5 \text{ ……. [8]}$$

For n=1 and k=8 the factor L is 11.3 for a zero TC. We will round L up to 12 for the design here.

$$Vref = (L.n.\ln K)\ VT + n.V_T.\ln (I/(k.Is)) \text{ … [9]}$$

The reference voltage at 300^0 K for I=10μA, Is=10^{-15}A, n=1, K=8, and L=12 is 1.25V (i.e., Vref=1.25 if Vss=0 and Vdd=5V). The current source designed here was used to bias a resistor of value 65KΩ and a diode with an area of 8 times the minimum size.

III. DESIGN OF ERROR AMPLIFIER

Here error amplifier means CMOS differential amplifier. The differential amplifier is one of the more versatile circuits in analog circuit design. It is also very compatible with integrated-circuit technology and serves as the input stage to most op-amps.

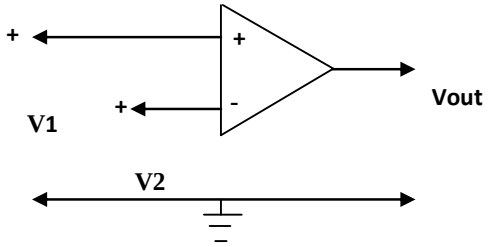

Fig.3: Symbol for error amplifier

Voltages V_1, V_2 and V_{out} are called single-ended voltages. This means that they are defined with respect to ground. The differential-mode input voltage, V_{ID} of error amplifier is defined as the difference between V_1 and V_2.This voltage is defined between two terminals[5], neither of which is ground. The common-mode input voltage, V_{IC} is defined as the average value of V_1 and V_2.These voltages are given as

$$V_{ID} = V_1 - V_2 \quad \text{..... [10]}$$

$$\text{And} \qquad V_{ID} = (V_1 + V_2)/2 \quad \text{..... [11]}$$

Note that V1 and V_2 can be expressed as

$$V_1 = V_{IC} + (V_{ID}/2) \quad \text{..... [12]}$$

$$\text{And} \qquad V_2 = V_{IC} - (V_{ID}/2) \quad \text{..... [13]}$$

The output voltage of the error amplifier can be expressed in terms of its differential-mode and common-mode input voltages as

$$V_{out} = A_{VD}V_{IC} = A_{VC}V_{IC} \quad \text{..... [14]}$$

Where A_{VD} is the differential-mode voltage gain and A_{VC} is the common-mode voltage gain. The objective of the error amplifier is to amplify only the difference between two different potentials regardless of the common-mode value. Thus, an error amplifier can be characterized by its common-mode rejection ratio (CMRR), which is the ratio of the magnitude of the differential gain to the common-mode gain. An ideal error amplifier will have a zero value of AVC and therefore an infinite CMRR. In addition, the input common-mode range (ICMR) specifies over what range of common-mode voltages the error amplifier continues to sense and amplify the difference signal with the same gain. Another characteristic affecting performance of the error amplifier is offset voltage. In CMOS differential amplifiers, the most serious offset is the offset voltage [7]. Ideally, when the input terminals of the differential amplifier are connected together, the output voltage is at a desired quiescent point. In a real differential amplifier, the output offset voltage is the difference between the actual output voltage and the ideal output voltage when the input terminals connected together. If this offset voltage is divided by the differential voltage gain of the error amplifier, then it is called the input offset voltage (VOS).

IV. IMPLEMENTATION OF VOLATGE REGULATOR

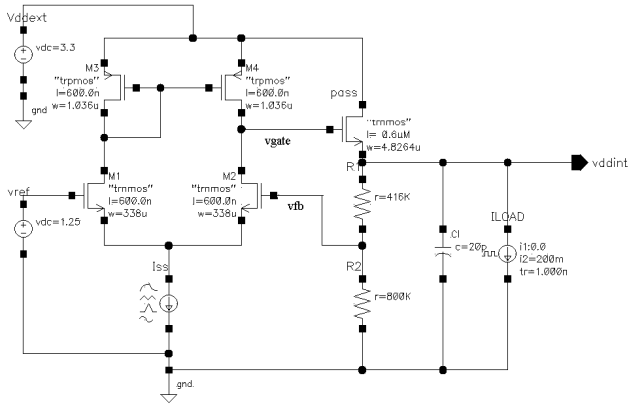

Fig.4: Schematic diagram of voltage regulator

The above figure 4 shows internal circuit of an error amplifier with the nmos pass transistor. When the load current from almost zero mA to few hundred mA rapidly, there is a dip in the internal Vdd level from its steady state value. Undershoot in internal Vdd occurs because of the feedback loop response delay. On the other hand, when the current load switches from few hundred mA to almost zero mA, there is an overshoot in the internal Vdd voltage due to same reason. This momentary overshoot in the internal Vdd, creates an offset at the input of the error amplifier. The overshoot in the internal Vdd node, is unavoidable. But, as the circuit draws negligible amount of leakage current in deselect mode, the internal Vdd node slowly discharges and it takes time to come back in its steady state value. So, the offset at the input of error amplifier remains for a longer period of time. As, in that period, feedback voltage node goes higher compare to reference voltage which is always stable, M2 transistor becomes stronger than M1 transistor. So, M2 transistor draws more current compare to current supplied by M4 transistor. As a result, gate voltage node which is output voltage of error amplifier is discharged heavily, if the input offset is quite high. Once, the gate voltage falls below (internal Vdd+Vth of pass transistor) voltage, the nmos pass transistor turns off. At that moment, the closed loop has been broken. When the input offset of the error amplifier gets reduced, gate voltage node starts to build up again and the nmos pass transistor turns on, in steady state. Suppose, if this transits to select mode, during the time when nmos pass transistor is 'off', the de-coupling capacitor will try to supply the charge initially, to full fill the current demand. But, as the de-coupling capacitor is less in on-chip regulator, it cannot supply charges for a longer period of time, especially when the load current is high in select mode. Since, the closed loop is broken, gate voltage node takes its own time to recover. As long as nmos pass transistor is 'off', internal Vdd node falls. It can fall much

below than the specified lower limit of internal Vdd, even to negative value. Internal Vdd dips once select mode starts when nmos pass transistor is 'off'. This problem normally occurs, if the deselect time is very less. But, if the deselect time is high enough to bring all the nodes into steady state value and then select mode starts, this type of problem will not occur.

V. DESIGN OF DYNAMIC LEAKER

To solve the problem mentioned above, we added a static leakage resistance at the internal Vdd node. So, when the deselect mode starts, the overshoot occurred in the internal Vdd node, will not sustain for a longer period of time, as the static leakage path draws a steady amount of current always. So, the offset at the input of error amplifier will be corrected quickly. As a result, gate voltage node does not fall below the (internal Vdd + Vth of nmos pass transistor), so the nmos pass transistor remains 'on' always. But in this case, a high value of leakage current is required, to keep the nmos pass transistor always 'on' at that transition edge.

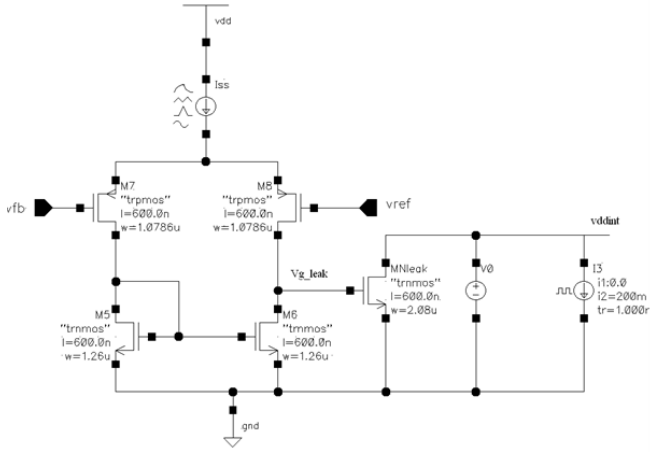

Fig.5: Circuit implementation of dynamic leaker

Another drawback of this method is that - it consumes static current from the load always. Hence, this method is not power efficient and it can violate the current specification of the circuit in deselect mode.

VI. SIMULATION RESULTS

The voltage regulator generates 1.9v from 3.3v external supply and the load current varies from few hundred mA to close to zero mA. Figure 6 shows the results for the out put of error amplifier with dynamic leaker and figure 7 shows the output of the voltage regulator with dynamic leaker in which instead of using static leakage path, if dynamic leaker is used, then it is burning 30µA peak current for a small duration of time, when the chip switches from one mode to other mode. But in steady state, it is drawing almost zero current.

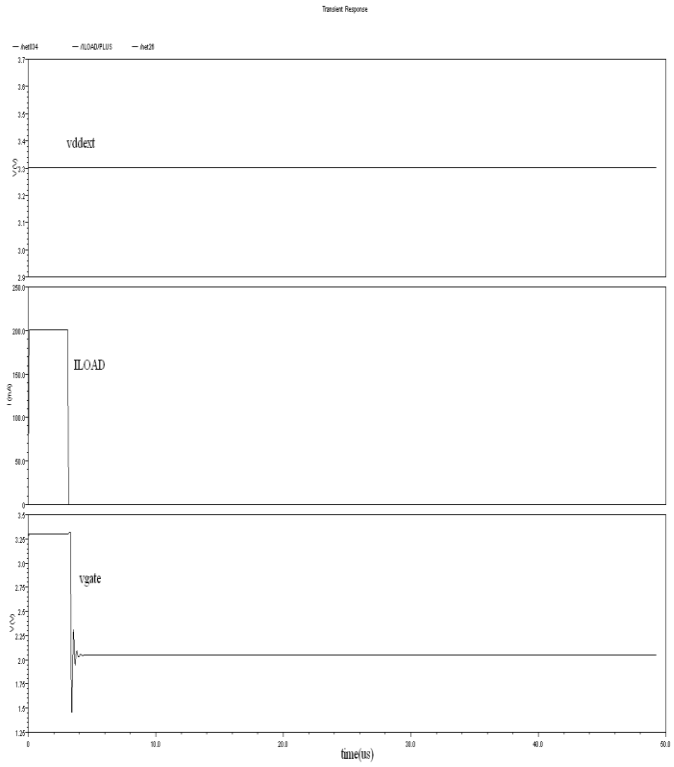

Fig.6: Output of the error amplifier with dynamic leaker at the output node

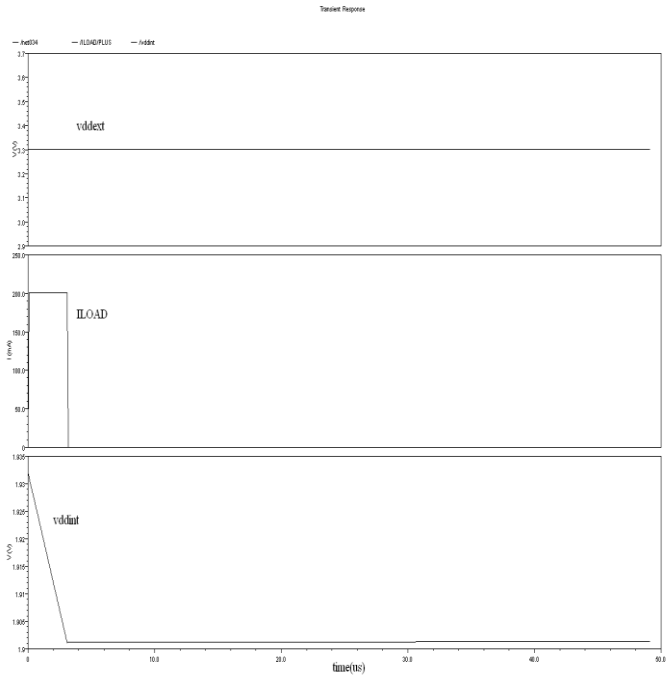

Fig.7: Output of the voltage regulator with dynamic leaker at the output node

Though the dynamic leaker circuit draws a peak of 44mA current for a small duration of time at the select to deselect transition edge, it is quite acceptable in the SRAM application where this type of transition is not quite often. Another advantage of this dynamic leaker is – it consumes only 300uA current internally and the overhead required for this circuit in terms of area is also very less.

VII. CONCLUSION

A novel design has been presented that allows improving the transient behavior of the on-chip voltage regulator in high-speed applications. Simulation results show that, static leaker demands a 0.85mA current to control the internal Vdd dip. On the other hand, the dynamic leaker consumes a peak current of 30µA for a small duration of time to achieve the same equivalent performance. As, in steady state, dynamic leaker draws almost zero current, it improves the active current specification and standby of the full circuit. Another advantage of this dynamic leaker circuit is, it consumes few uA current internally and the overhead required for this circuit in terms of area is also very less.

VIII. REFERENCES

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