International Journal of Modern Science and Technology, 2018;3(3):59-64.
ISSN: 2456-0235.
www.ijmst.co

Research Article

Design and Power analysis of Decoders for Memory Array Structure

K. Gavaskar, V. Malini

Department of Electronics and Communication Engineering,
Kongu Engineering College, Perundurai – 638060. India.

*Corresponding author's e-mail: gavas.20@gmail.com

Abstract

Digital electronics circuits operate with digital signals so there performance is less subject to noise, signal attenuation and manufacturing tolerance. Digital system have prominent role in everyday life due to their ability to represent and manipulate discrete elements of information. Logic circuits for digital system may be combinational or sequential. A decoder is a combinational circuit that converts code into a set of signals. A binary code of n bits is capable of representing upto 2^n distinct elements of coded information. The operation of the decoder may be clarified by the truth table. A decoder that generates the minterms of the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function. A decoder with an enable input is referred to as decoder - demultiplexer. Three different decoders 1X2, 2X4 and 4X16 decoders are analyzed in this paper. Design metrics such as static power and dynamic power are taken into account. All the decoders were designed using SYNOPSYS EDA tool and simulated in 30nm technology. Simulation results shows that the 4X16 decoder has higher power dissipation than the other two decoders.

Keywords: Dynamic power; Static power; Decoder; Array structure; Memory.

Introduction

The process of creating an IC (Integrated Circuit) by combining thousands of transistors into a single chip is termed as VLSI. When complex semiconductor and communication technologies were being developed VLSI began its progress. Most ICs had a limited set of functions they could perform before the introduction of VLSI technology. As side effect of advances in the world of computers, there has been a dramatic proliferation of tools that can be used to design VLSI circuits [1]. The capability of an IC has increased exponentially over the years, in terms of computation power, utilization of available area, yield.

Digital VLSI circuits are predominantly CMOS based. The parameters considered while dealing with VLSI circuits are circuit delays, power and layout [2]. Circuit operating at higher frequencies has two major problems. First is delay in propagation of signals through gates and wires. Second is increased consumption of power. This has two fold effect- devices consume batteries faster, and heat dissipation increases. Coupled with the fact that surface areas have decreased, heat poses a major threat to the stability of the circuit itself [3]. Laying out the circuit components is task common to all branches of electronics which mostly don't depend on operating frequency and mainly depends on complexity of the circuit. There are many possible ways to do this. There can be multiple layers different materials on the same silicon there can be different arrangements of the smaller parts for the same component and so on which affect the stability [4] of the system.

In CMOS circuits, there are three sources of power dissipation. Dynamic power dissipation is due to logic transitions and short circuit current. As the nodes in a digital CMOS circuit transition back and forth between the two logic levels, the parasitic capacitance are charged and discharged. Static power dissipation is main component of power dissipation in deep nanometre technologies (below 45 nm) [5]. When a CMOS circuit is in idle state there is still some leakage power dissipation due to leakage current flowing through nominally OFF transistors. Both NMOS and PMOS transistors used in CMOS logic gates have finite reverse leakage and sub threshold currents. In a silicon

Received: 15.03.2018; Received after Revision: 23.03.2018; Accepted: 23.03.2018; Published: 25.03.2018

chip there are millions of transistors and overall power dissipation due to leakage current [6] is comparable to dynamic power dissipation. Real circuit signals have non-zero rise and fall times which causes both P_{net} and the N_{net} of the CMOS gate to conduct current simultaneously. This leads to flow of a short circuit current for a short period of time. With inputs to the gate are stable at either logic level, only one of the two subnetworks conduct and no short circuit current flows in the circuit. All the above power dissipation depends on activity, timing, output capacitance and supply voltage of the circuit. The total power dissipation is given by eq. (1).

$$P_{tot} = P_{dynamic} + P_{static}$$
$$P_{tot} = (P_{short} + P_{switch}) + P_{static} \quad \ldots(1)$$

The most important factor to consider while designing semiconductor IC for portable device is 'low power design'. The growing market of portable battery powered electronic system demands microelectronic circuit design with ultralow power dissipation.

A decoder is a device which does the reverse of an encoder undoing the encoding so that the original information can be retrieved. Encode [7] is to put something into code to make it unreadable to someone who does not know the code. Decode is to work out the code or unscramble the code. So encoder would be something to code the article, while a decoder unscrambles the code and gives you back the article. Different types of decoder are available which can be chosen based on the need of the application [8]. Decoders are greatly used in applications where the particular output or group of outputs to be activated only on the occurrence of a specific combination of input levels. Very often these input levels are provided by the outputs of a register or counter [9]. When the counter or register continuously pulse the decoder inputs, the outputs will be activated sequentially. And these outputs can be used as sequencing signals or timing signals to switch the devices at particular times.

Applications of the decoder are speed synchronization of multiple motors in industries, war field flying robot with a night vision flying camera, robotic vehicle with the metal detector, RF based home automation system and automatic health monitoring systems [10].

Decoder structures

1X2 decoder

The 1X2 decoder is the basic decoder unit in the combinational circuit. The decoder unit has two inputs and two output [11] ie. inputs are "in" and "en" and the outputs are "out 1" and "out 2". Only when the input "en" is 1 the outputs will be available depending on the input "in". If "en" is 0 the output will not be available. The schematic diagram of 1X2 decoder is shown in fig. 1. Fig. 1 represents 1X2 decoder unit in which "i1" and "i2" acts as inputs and "o1" and "o2" acts as outputs. The input "i2" acts an enable input to the decoder unit. If i2=1, the decoder unit produces output as "and" gate (andts) will be in ON state. The power measured in this case is dynamic power. If i2=0, the decoder unit does not provide correct output as the "and" gate (andts) will be in OFF state. The power measured in this case is static power. Fig. 2 represents the symbol of 1X2 decoder.

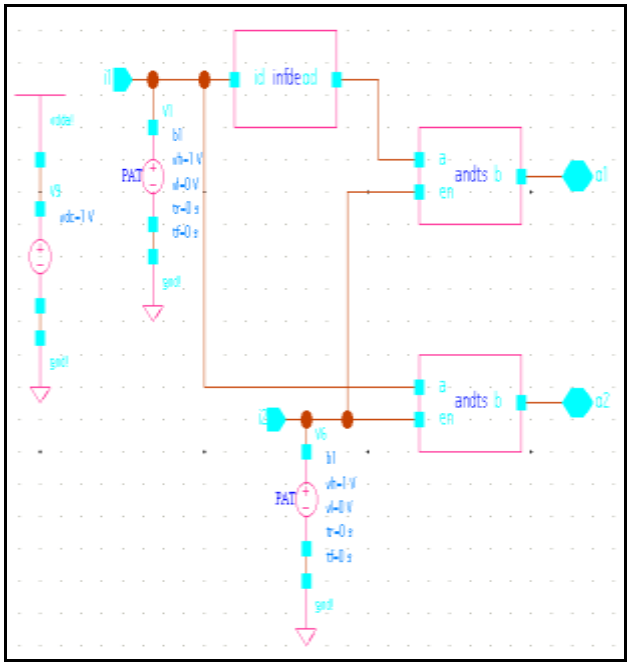

Fig. 1. Schematic diagram 1X2 Decoder

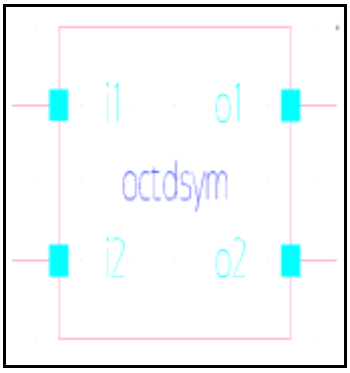

Fig. 2. 1X2 Decoder symbol

2X4 decoder

The 2X4 decoder is the decoder unit mostly used in the combinational circuit for many applications. The decoder unit has three inputs and four outputs [12] ie the inputs are "in", "in1" and "en" and the outputs are "out1", "out2", "out3" and "out4". Only when the input "en" is 1 the outputs will be available depending on the inputs "in" and "in1". If "en" is 0 the output will not be available. The schematic diagram of 2X4 Decoder is shown in fig. 3. Fig. 3 represents 2X4 decoder unit in which "i1", "i2" and "i3" acts as inputs and "o1", "o2", "o3" and "o4" acts as outputs. The input "i3" acts an enable input to the decoder unit. If i3=1, the decoder unit produces output as “and” gate (andts) will be in ON state. The power measured in this case is dynamic power. If i3=0, the decoder unit does not provide correct output as the “and” gate (andts) will be in OFF state. The power measured in this case is static power. Fig. 4 represents the symbol of 2X4 decoder.

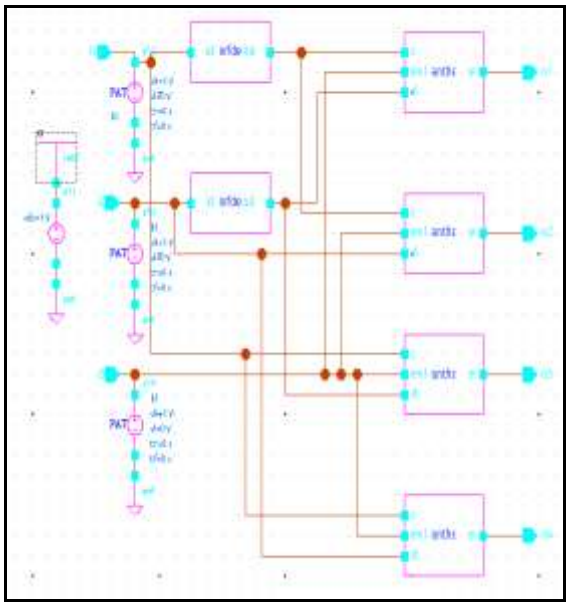

Fig. 3. Schematic diagram of 2X4 decoder

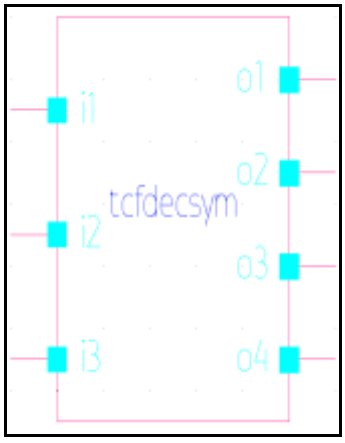

Fig. 4. 2X4 Decoder symbol

4X16 Decoder

The 4X16 decoder is the decoder unit mostly used in many applications which requires more decoded outputs. The decoder unit [13] has five inputs and sixteen output. The inputs are "in", "in1", "in2", "in3" and "en". Only when the input "en" is 1 the outputs will be available depending on the input values. If "en" is 0 the output will not be available. The schematic diagram of 4X16 Decoder is shown in fig. 5. Fig. 5 represents 4X16 decoder unit which has five inputs "a", "b", "c", "d" and "en" and sixteen outputs. The input "en" acts an enable input to the decoder unit. If en=1, the decoder unit produces output as “and” gate (andts) will be in ON state. The power measured in this case is dynamic power. If en=0, the decoder unit does not provide correct output as the “and” gate (andts) will be in OFF state. The power measured in this case is static power. Fig. 6 represents the symbol of 4X16 decoder.

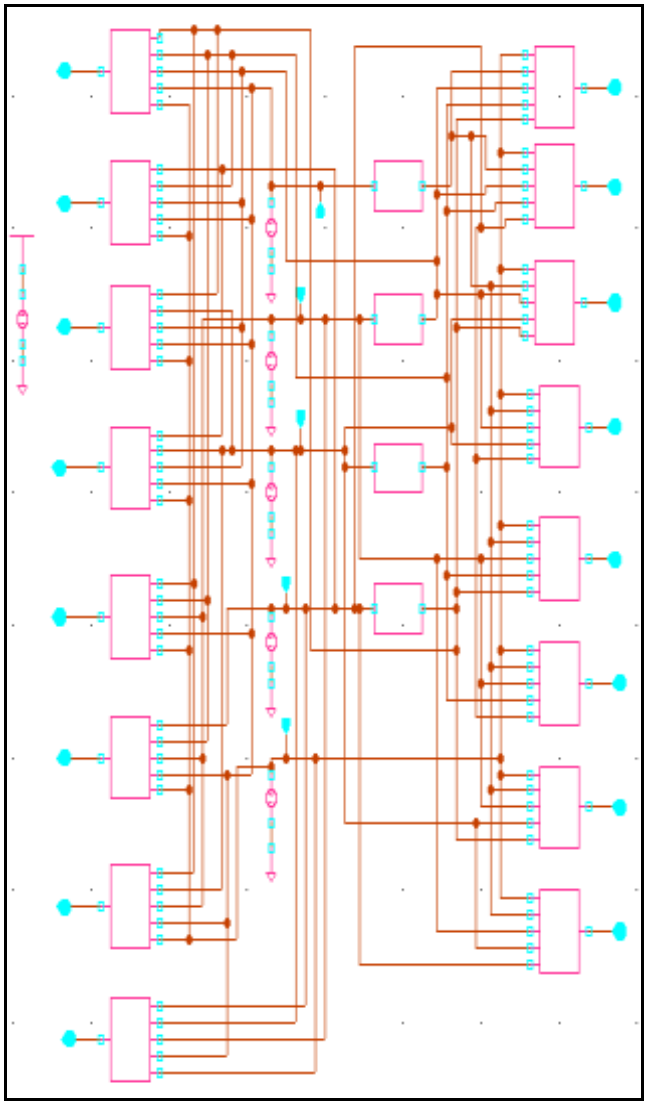

Fig. 5. Schematic diagram of 4X16 decoder

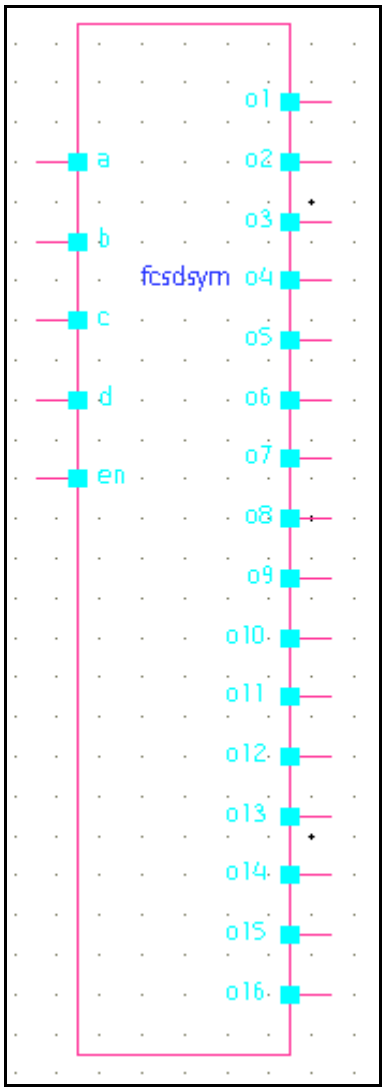

Fig. 6. 4X16 Decoder symbol

Results and discussion

The tool used to design the decoder [14] structures is SYNOPSYS tool. All the cells are simulated in 32nm technology using SAED_iPDK library.

Simulation result of 1X2 decoder

Simulation result of 1X2 decoder is shown in fig. 7. In Fig. 7 v(i1), v(i2) and v(o2) represents the inputs and outputs of decoder unit. The time period is specified in X-axis and voltage is represented in Y-axis. The enable input "i2" is given as 1 and "i1" is given as 1 so output o2 is 1.

Simulation result of 2X4 decoder

Simulation result of 2X4 decoder is shown in fig. 8. In Fig. 8 v(i1), v(i2), v(i3) and v(o4) represents the inputs and outputs of decoder unit. The time period is specified in X-axis and voltage is represented in Y-axis. The enable input "i3" is given as 1 and other inputs "i1", "i2" is given as 1 so output o4 is 1.

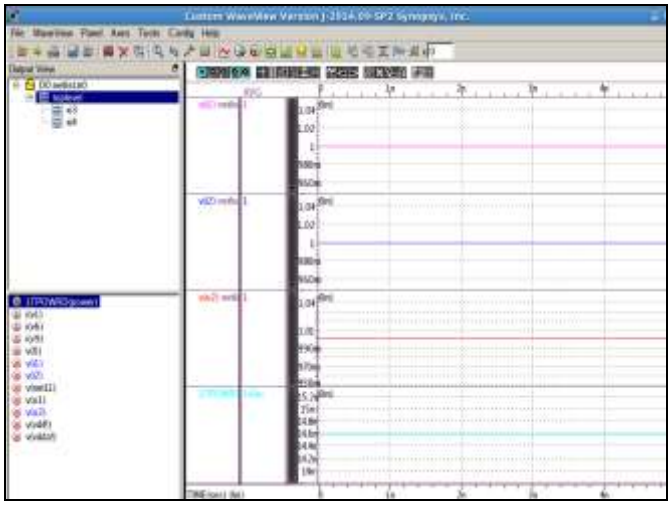

Fig. 7. Simulation result of 1X2 decoder unit

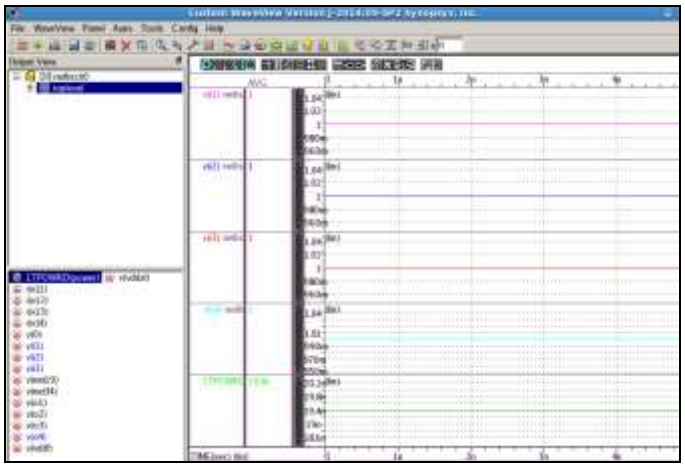

Fig. 8. Simulation result of 2X4 Decoder unit

Simulation result of 4X16 decoder

Simulation result of 4X16 decoder is shown in fig. 9. In Fig. 9 v(a), v(b), v(c), v(d), v(en) and v(o4) represents the inputs and outputs of decoder unit. The time period is specified in X-axis and voltage is represented in Y-axis. The enable input "en" is given as 1 and other inputs "a", "b", "c", "d" is given as 1 so output o16 is 1.

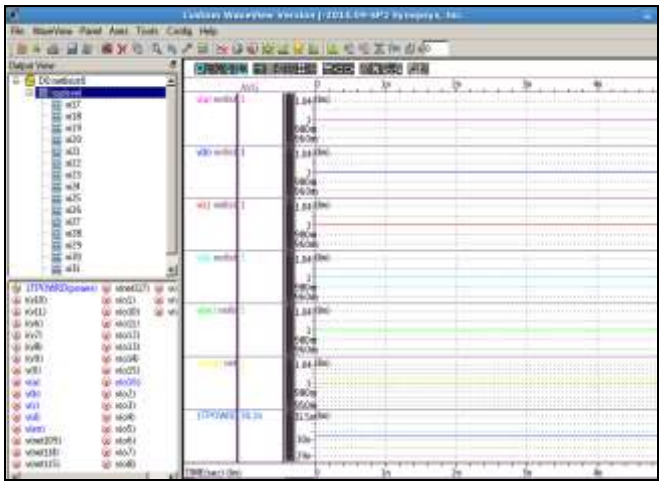

Fig. 9. Simulation result of 4X16 Decoder unit

Power analysis of different decoder units

The power dissipation [15] of different decoder is calculated using SYNOPSYS tool in 30nm technology. Both static and dynamic power is calculated for three different decoders for different voltage values. The average power dissipation of all three different decoders in 30 nm technology is given in table 1 and table 2. It is observed that the 4X16 decoder has high power dissipation compared to other decoder units.

Table 1. Dynamic power analysis of different decoders

Different Decoders	Power dissipation in nanowatts						
	0.6V	0.7V	0.8V	0.9V	1V	1.1V	1.2V
1X2	1.62	2.89	5.04	8.64	14.6	24.2	39.6
2X4	2.4	4.14	7.03	11.7	19.4	31.6	50.8
4X16	4.64	7.51	12	19.1	30.2	47.5	74.1

Table 2. Static power analysis of different decoders

Different Decoders	Power dissipation in nanowatts						
	0.6V	0.7V	0.8V	0.9V	1V	1.1V	1.2V
1X2	1.07	1.92	3.33	5.76	9.83	16.6	27.6
2X4	1.33	2.25	3.79	6.33	10.5	17.4	28.5
4X16	2.52	3.82	5.81	8.92	13.7	21.3	33.2

Graphical representation

Fig. 10 shows the power comparison of 1X2 decoder unit. From the graph, it is observed that the dynamic power dissipation of decoder unit is higher than its static power.

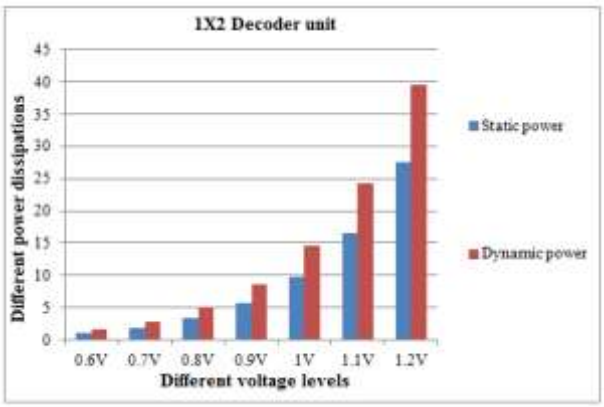

Fig. 10. Power comparison of 1X2 decoder unit

Fig. 11 shows the power comparison of 2X4 decoder unit. From the graph, it is observed that the dynamic power dissipation of decoder unit is higher than its static power.

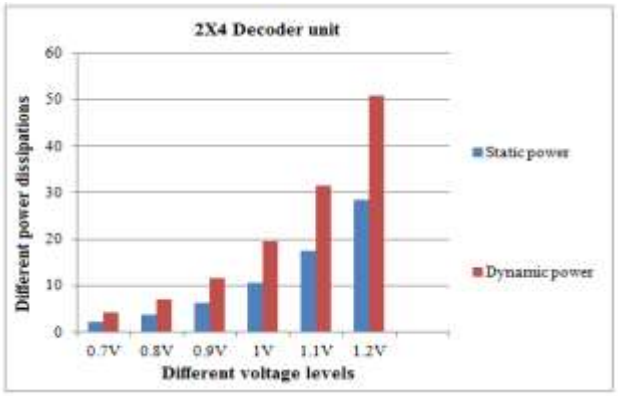

Fig. 11. Power comparison of 2X4 decoder unit

Fig. 12 shows the power comparison of 4X16 decoder unit. From the graph, it is observed that the dynamic power dissipation of decoder unit is higher than its static power.

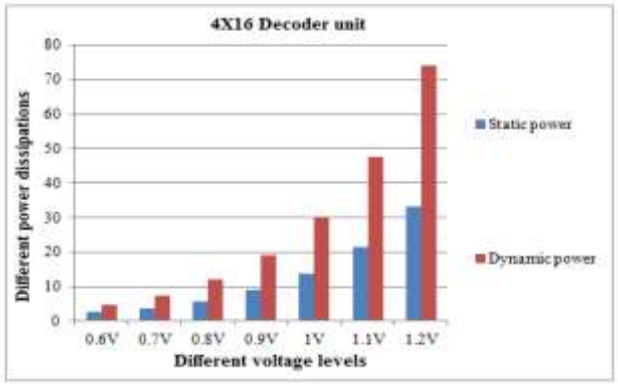

Fig. 12. Power comparison of 4X16 decoder unit

Conclusions

The Power, area, and delay are the major aspects of VLSI industry. In modern day processor power dissipation plays a major role because of the miniaturization of chip design. In this paper both static and dynamic power dissipation of three different decoders are analyzed. The 4X16 decoder has 50%, 34% higher dynamic power dissipation and 25%, 21% higher static power dissipation compared to 1X2 decoder and 2X4 decoder units. The enable input in decoder is a convenient feature for interconnecting two or more standard components for the purpose of combining them into a similar function with more inputs and outputs. Decoders are needed for implementation of array structure. Efficient implementation of array structure needs both row and column decoder to be chosen correctly. Decoders are also used in conjunction with other

code converters, such as BCD to seven segment decoder.

Conflicts of interest

The authors declare no conflict of interest.

References

[1] Soundarya S, Prasanna K. Implementation of low power, delay and area efficient Shifters for Memory Based Computation. . International Journal of Modern Science and Technology. 2017;2(5):217-222.

[2] Sivaranjini S, Kavitha G. Design of area efficient and low power carry select adder. International Journal of Modern Science and Technology. 2017;2(6):243-248.

[3] Gavaskar K, Ragupathy U S. An Efficient Design and Analysis of Low Power SRAM Memory Cell for Ultra Applications. Asian J Res Soc Sci Humn. 2017;7(1):962-975.

[4] Nayak D, Mahapatra.K. Current starving SRAM cell: A strategy to improve the cell stability and power. Circ Syst Signal Pr. 2017;36(10):3047-3070.

[5] Babu A, Ravindra J V R. Design of Ultra Low Power PMOS and NMOS for Nano Scale VLSI circuits. Circ Syst Signal Pr. 2015;34(13):60-69.

[6] Leela Rani V, Latha M. Pass Transistor-Based Pull-Up/Pull-Down Insertion Technique for Leakage Power Optimization in CMOS VLSI Circuits. Circ Syst Signal Pr. 2016;35(8):4139–4152.

[7] Abikayal K, Sriram A. Design of reversible comparator using Reversible Gates with Encoding Technique International Journal of Modern Science and Technology. 2017;2(6):238-242.

[8] Lee GG, Chen CF. High- Throughput Reconfigurable Variable Length Coding Decoder for MPEG-2 and AVC/H.264. J Sign Process Syst. 2016;82:27-40.

[9] Vikram AC, Azid SM. Resource Efficient LDPC Decoders for multimedia communication. Integ VLSI J. 2015;48:213-220.

[10] Shalini S, Shyam A. A Low Power Consuming 1KB (32X32) Memory Array Using Compact 7T SRAM cell. Wireless Pers Comm. 2017;96(1):1099-1109.

[11] Huyen PT, Sabooh A. High throughput partial parallel block layered decoding architecture for non binary LDPC codes. Integration the VLSI Journal. 2017;59:52-63.

[12] Wojciech S. Non binary LDPC Decoders Design for Maximizing Throughput of an FPGA Implementation. Circ Syst Signal Pr. 2016;35:4060-4080.

[13] Pallavi S, Vanya A. Design and analysis of all optical half adder, half subtractor and 4 bit decoder based on SOA-MZI configuration. Opt Quant Electron. 2016;48:159. https://doi.org/10.1007/s11082-016-0429-x

[14] Shiann-Rong K, Ping T. A Low Power Codeword Based Viterbi Decoder with Fine Grained Error Detection and Correction Techniques. Arab J Sci Eng. 2018;43:585-595.

[15] Gavaskar K, Ravivarma G. Power analysis of Sense Amplifier Designs for low voltage Memories. International Journal of Modern Science and Technology. 2017;2(10):345-353.

****

