32 Taps FIR FILTER DESIGN USING BAUGH-WOOLEY MULTIPLIER WITH KSA ADDER

V. PAVANI[1], Dr.B.L MALLESWARI[2], Urvashi Gupta[3]
[1]*M.Tech, VLSI Department, Sridevi Women's Engineering College, JNTUH, Hyderabad, India*
[2]*PRINCIPAL, ECE Department, Sridevi Women's Engineering College, Hyderabad, India.*
[3]*Assistant Professor, ECE Department, Sridevi Women's Engineering College, Hyderabad, India.*
([1]pavani9393@gmail.com)

Abstract-FIR filtering is one of the most widely used operations in several applications, while Reconfigurable finite-impulse response (FIR) filters are one of the most widely implemented components in Internet of Things systems due to their flexibility and low power consumption. The most significant operation in the FIR Filter is Multiplier, when aimed to reduce the power consumption multiplier plays a major role. Previous works deals around Low-Power Operation in Reconfigurable FIR Filters utilizing Baugh-Wooley multiplier and Vedic multiplier to accomplish the low power utilization and less zone. In this paper to reduce even more area and power consumption an FIR filter is designed for 32 taps using Baugh-Wooley multiplier with KSA adder. Implemented design results are more efficient when compared with previous results.

Keywords-*FIR Filter; KSA (Kogge Stone Adder); Baugh-Wooley Multiplier; Vedic Multiplier.*

I. INTRODUCTION

FIR filters assume a critical part in the present advanced flag handling and different applications. In elite frameworks such microchips, DSP and different applications [1]. Expansion and Multiplication of the two double numbers are central and frequently utilized math operations. Statics demonstrates that over 70% directions in chip and the greater part of DSP calculation perform expansion and multiplication. Well these operations rule the execution time. Along previous lines, there's need of fast multiplier. The request of fast processing has been expanding because of extending PC and flag handling applications [3].

FIR FILTER.

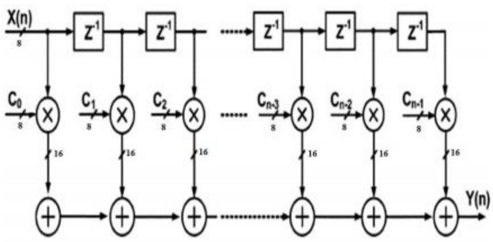

Fig.1: Finite Impulse Response Filter Realization

FIR filters are one of the primary types of filters used in Digital Signal Processing. FIR filters are said to be finite because they do not have any feedback. Therefore, if we send an impulse through the system (a single spike) then the output will invariably become zero as soon as the impulse runs through the filter. A non-recursive filter has no feedback. The Finite Impulse Response Filter Realization is as shown in figure 1. Very often these filters need to support high sampling rate for high-speed digital communication. The number of multiplications and additions required for each filter output, however, increases linearly with the filter order [4]. Since there is no redundant computation available in the FIR filter algorithm, real-time implementation of a large order FIR filter in a resource constrained environment is a challenging task. Many related operations were made for multiplications and additions to improve the computation speed [6]. One of those are Baugh-Wooley multiplier and the Vedic multiplier used in the FIR Filter design that shows high performance.

In this paper we design the FIR Filter using the Baugh_Wooley Multiplier and Vedic Multiplier, and in order to improve even more computation speed, the designed FIR Filter with Baugh-Wooley multiplier has been improved by replacing the adder using Kogge Stone Adder. The rest of the paper shows the implementation of the multipliers and their use in the design of FIR filter for high performance.

II. DESIGN OF FIR FILTER WITH BAUGH-WOOLEY MULTIPLIER AND VEDIC MULTIPLIER.

In the process of the FIR Filter design computation field is more important for the efficient design [4].

$$\mathrm{out(n)} = \sum_{i=0}^{N-1} x(n-i)\, h(i)$$

Above equation shows the computation operation of the FIR Filter. This computation is multiplication operation so in order to improve the efficiency of the Filter design multiplication is mostly considered. Here in this paper we design the FIR Filter with Baugh-Wooly multiplier and Vedic multiplier.

A. Baugh-Wooley multiplier.

The Baugh-Wooley augmentation is one of the most important strategies to manage sign bots. This technique has been so as to plan consistent multipliers, suited for 2's supplement numbers [25].

Let two n-bit numbers, multiplier (A) and multiplicand (B), to be increased. A and B can be communicated as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \quad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \quad (2)$$

Where the ai‘s and bi‘s are the bits in A and B respectively, and an-1 and bn-1 are the sign bits. The product P = A x B, is given by the equation

$$P = A \times B = \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right)$$

$$= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j - 2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1} 2^i - 2^{n-1}\sum_{j=0}^{n-2} a_{n-1} b_j 2^j \quad (3)$$

The final product can be generated by subtracting the last two positive terms from the first two terms. In place of performance subtraction operation, it is possible to obtain the 2‘s complement of the last two terms and add all terms to build the final product. The keep going two terms are n-1 bits in which every that range in parallel weight from position 2n-1 up to 22n-3. after that again, the last item is 2n bits and reaches out in parallel load from 20 up to 22n-1. At first cushion every one of the last two terms in the item P condition with zeros to get a 2n-bit number to have the capacity to include it with the different terms. Then the padded terms increase in binary weight from 20 up to 22n-1. Let X is one of the last two terms that can represent it with zero padding as

$$X = -0 \times 2^{2n-1} + 0 \times 2^{2n-2} + 2^{n-1}\sum_{i=0}^{n-2} x_i 2^i + \sum_{j=0}^{n-2} \times 2^j \quad (4)$$

The final product, P = A x B becomes

$$P = A \times B$$

$$= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j + 2^{n-1}\sum_{i=0}^{n-2} \overline{a_i b_{n-1}} 2^i + 2^{n-1}\sum_{j=0}^{n-2} \overline{a_{n-1} b_j} 2^j - 2^{2n-1} + 2^n \quad (5)$$

Let A and B are 4-bit binary numbers, then the product P = A x B will be 8 bit long and is

$$P = a_3 b_3 2^6 + \sum_{i=0}^{2} a_i 2^i \sum_{j=0}^{2} b_j 2^j + 2^3 \sum_{i=0}^{2} \overline{a_i b_3} 2^i + 2^3 \sum_{j=0}^{2} \overline{a_3 b_j} 2^j - 2^7 + 2^4 \quad (6)$$

The block diagram for 4 bit Baugh Wooley multiplier is shown in Fig 2.

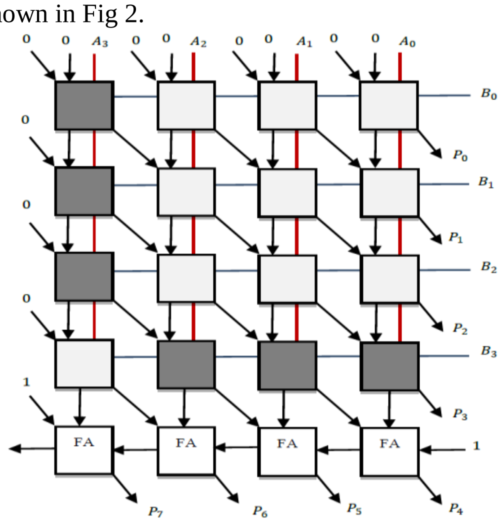

Fig.2: Block diagram of 4 bit Baugh -Wooley multiplier

B. Vedic Multiplier

Vedic science was reproduced from the out of date Indian consecrated writings (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic math is dominatingly in perspective of sixteen principles or word-formulae which are named as sutras. This is a to a great degree intriguing field and shows some practical estimations which can be associated with various parts of working, for instance, enlisting and electronic banner getting ready. Consolidating increment with Vedic Mathematics frameworks would achieve the saving of computational time. Therefore, joining Vedic science for the multiplier setup will enhance the speed of duplication task. The multiplier designing relies upon Urdhva Tiryagbhyam.

Basic multiplication have been by using Vedic multiplier is as shown in the figure.

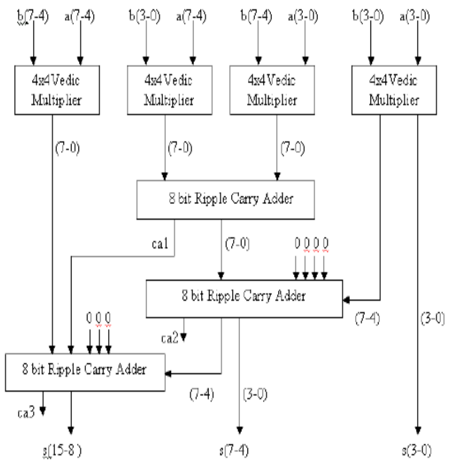

*Fig. 3: 8*8 Vedic Multiplier*

We can implement 8bit, 16bit and 32bit multipliers through the use of 4 bit multiplier [26]. The current 8-bit Vedic multiplier comprises of four 4-bit Vedic multipliers and three 8-bit swell convey adder. Give us a chance to take A and B are of 8-bit input which gives a yield S of sixteen piece and results are gotten in the wake of getting halfway item and doing expansion.

In the design of the FIR Filter with Baugh-Wooley multiplier CSA adder is used for the addition operation that performs computations with an average speed to improve the speed of the computation in the FIR filter and improve the design efficiency Baugh-Wooley multiplier with CSA adder is replaced with Kogge stone adder.

III. DESIGN OF FIR FILTER USING BAUGH-WOOLEY MULTIPLIER WITH KSA ADDER

FIR Filter design using Baugh-Wooley multiplier with Kogge stone. In the process of the FIR filter design to improve the design efficiency Baugh-Wooley multiplier with CSA adder is replaced with Kogge stone adder.

KOGGE-STONE ADDER

Kogge-stone adder is a parallel prefix construction of Carry Look-ahead Adder. Kogge- Stone snake may be appeared as a parallel prefix viper comprising of convey administrator hubs. It is the quickest snake with as indicated by outlining time. It's the regular decision for high appearance adders in industry. The Kogge-Stone Adder was first created by Peter M. Kogge and Harold S. Stone in 1973. The development of 2, 4-bit Kogge-Stone Adder are demonstrated as follows.

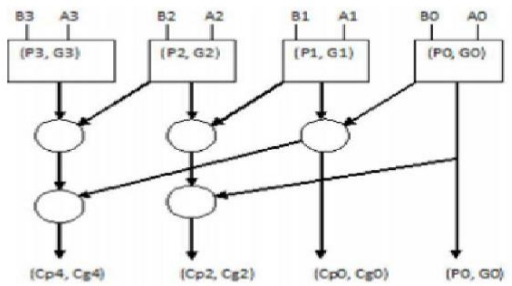

Fig.4:Schematic diagram of 4-bit Kogge-Stone Adder

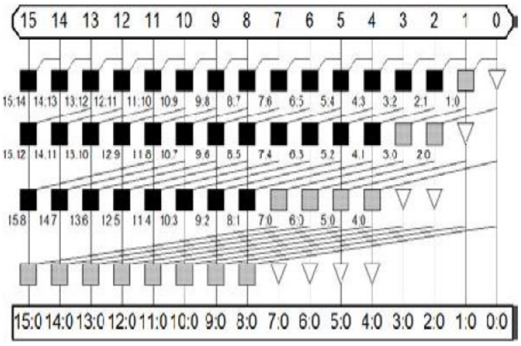

Fig.5: Schematic diagram of 4-bit Kogge-Stone Adder.

IV. SIMULATION RESULTS

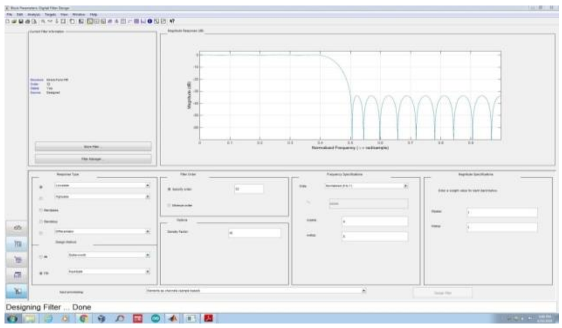

Fig.6: Magnitude response of 32 Taps FIR Filter design

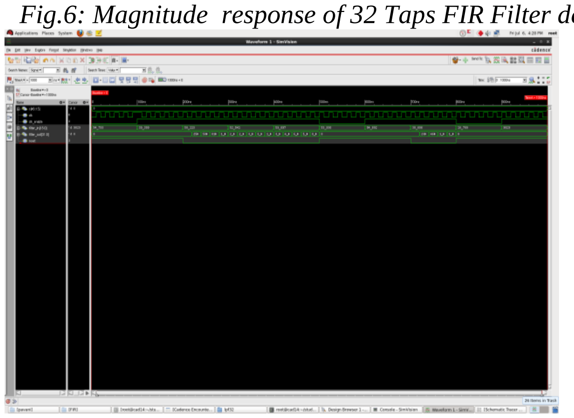

Fig.7: NC Result of 32 Taps FIR Filter design using Baugh-Wooley multiplier with CSA adder.

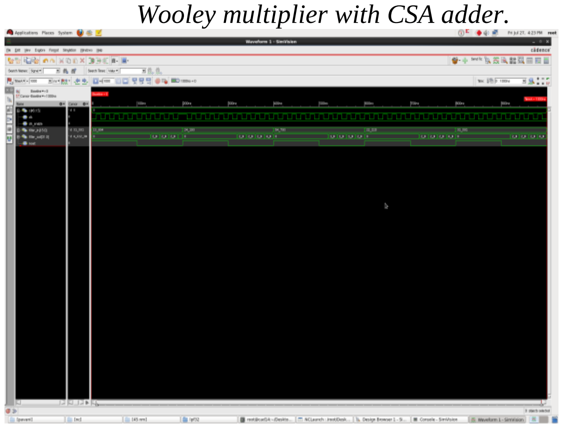

Fig. 8: NC Result of 32 Taps FIR Filter design using Baugh-Wooley multiplier with KSA adder.

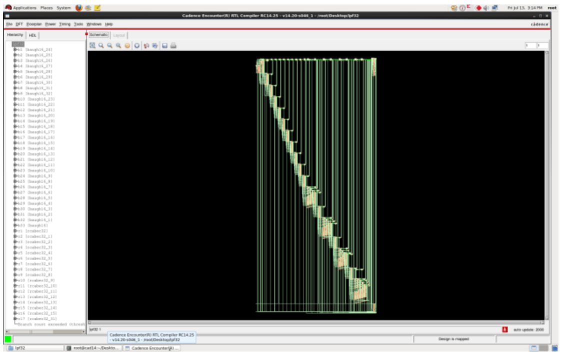

Fig.9: RC Results of32-Taps FIR filter using Baugh-Wooley multiplier with CSA adder

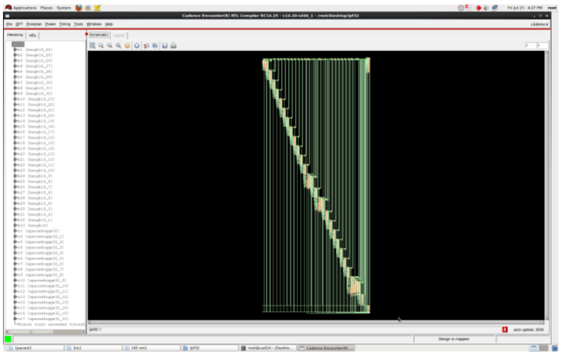

Fig.10: RC Results of32-Taps FIR filter using Baugh-Wooley multiplier with KSA adder.

Comparison Table.

32-taps FIR Filter	Multiplier Type	Power(mW)	Area(µm²)
Low pass	Baugh-Wooley	8.027	35107
High Pass	Baugh-Wooley	8.451	36048
Band pass	Baugh-Wooley	8.106	36915
Band Stop	Baugh-Wooley	8.326	36157

Table .I: 32 Taps FIR filter using Baugh Wooley multiplier with Kogge stone adder.

Filter Type	Multiplier Type	Power(mW)	Area(µm²)
Low pass(8-taps)	Baugh-Wooley	2.608	4034
	Vedic	3.127	6907
Low pass(16-taps)	Baugh-Wooley	4.334	15601
	Vedic	13.390	45753
Low pass(32-taps)	Baugh-Wooley	23.185	61027
	Vedic	37.890	88754
High Pass(8-taps)	Baugh-Wooley	2.175	3510
	Vedic	2.729	6333
High Pass(16-taps)	Baugh-Wooley	4.623	16894
	Vedic	14.140	48325
High Pass(32-taps)	Baugh-Wooley	24.978	60952
	Vedic	56.281	114385
Band pass(8-taps)	Baugh-Wooley	2.497	4028
	Vedic	3.450	8254
Band pass(16-taps)	Baugh-Wooley	4.229	15734
	Vedic	12.106	43941
Band pass(32-taps)	Baugh-Wooley	23.210	61079
	Vedic	37.885	88727
Band Stop(8-taps)	Baugh-Wooley	2.504	3801
	Vedic	2.492	4836
Band Stop(16-taps)	Baugh-Wooley	4.344	15384
	Vedic	12.425	44129
Band Stop(32-taps)	Baugh-Wooley	23.788	60332
	Vedic	48.574	10622

Table. II: Different taps of Fir Filter comparison between Baugh Wooley and Vedic Multiplier

V. CONCLUSION

The designed FIR filter has lower power consumption and less area than compared with other FIR filters. The Baugh-wooley multiplier is used to multiply the signed and unsigned binary numbers after generation of the partial products addition at the last stage of Multiplication and Kogge-Stone Adder (KSA) is used for this addition. Any analytical power and area of our Multiplier design, adder design and other previous designs are presented. This analytical approach can also be used in other designs. By this proposed methods we designed 8, 16 and 32 Taps as a Low Pass FIR Filter, High Pass FIR Filter, Band Pass FIR Filter and Band Stop FIR Filters. This project can also be done as 32, 64 and 128 Taps as a Low Pass FIR Filter, High Pass FIR Filter, Band Pass FIR Filter and Band Stop FIR Filters in advanced technologies like 45nm, 32nm, 28nm etc.

REFERENCES

[1]. M. Alioto, Enabling the Internet of Things: From Integrated Circuits to Integrated Systems. Cham, Switzerland: Springer International, 2017.

[2]. F. Sheikh, M. Miller, B. Richards, D. Markovi´c, and B. Nikoli´c, "A 1–190M Sample/s 8–64 tap energy-efficient reconfigurable FIR filter for multi-mode wireless communication," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2010, pp. 2017–2018.

[3]. R. Hegde and N. R. Shanbhag, "A voltage overscaled low-power digital filter IC," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 388–391,Feb. 2004.

[4]. J. Chen, C. H. Chang, F. Feng, W. Ding, and J. Ding, "Novel design algorithm for low complexity programmable FIR filters based on extended double base

number system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 224–233, Jan. 2015.

[5]. S. Y. Park and P. K. Meher, "Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 7, pp. 511–515, Jul. 2014.

[6]. P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an under designed multiplier architecture," in *Proc. 24th Int. Conf. VLSI Design*, Jan. 2011, pp. 346–351.

[7]. K. Bhardwaj, P. S. Mane, and J. Henkel, "Power- and area-efficient Approximate wallace tree multiplier for error-resilient systems," in *Proc. 15th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2014, pp. 263–269.

[8]. C.-H. Lin and I.-C. Lin, "High accuracy approximate multiplier with error correction," in *Proc. IEEE 31st Int. Conf. Comput. Design (ICCD)*, Oct. 2013, pp. 33–38.

[9]. C. Liu, J. Han, and F. Lombardi, "A low-power, high-performance approximate multiplier with configurable partial error recovery," in *Proc. Design, Autom. Test Eur. Conf. Exhibit. (DATE)*, Mar. 2014, pp. 1–4.

[10]. C. Neau, K. Muhammad, and K. Roy, "Low complexity FIR filters using factorization of perturbed coefficients," in *Proc. Design, Autom. Test Eur.Conf. Exhibit. (DATE)*, 2001, pp. 268–272.

[11]. S. Hong, S. Kim, M. C. Papaefthymiou, and W. E. Stark, "Low power parallel multiplier design for DSP applications through coefficient optimization," in *Proc. 12th Annu. IEEE Int. ASIC/SoC Conf.*, Sep. 1999,pp. 286–290.

[12]. M. Mehendale, S. D. Sherlekar, and G. Venkatesh, "Low-power realization of FIR filters on programmable DSPs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 6, no. 4, pp. 546–553, Dec. 1998.

[13]. B. Parhami, *Computer Arithmetic*, vol. 20. Oxford, U.K.: Oxford Univ. Press, 1999.

[14]. R. Zimmermann, "VHDL library of arithmetic units," in *Proc. 1st Int. Forum Design Lang. (FDL)*, Lausanne, Switzerland, 1998, pp. 267–272.

[15]. Y. Huang, A. Kapoor, R. Rutten, and J. P. de Gyvez, "A 13 bits 4.096GHz 45Nm CMOS digital decimation filter chain with carry-save format numbers," *Microprocess. Microsyst.*, vol. 39,no. 8, pp. 869–878, Nov. 2015. [Online]. Available: http://dx.doi.org/10.1016/j.micpro.2014.11.003

[16]. V. G. Oklobdzija, D. Villeger, and S. S. Liu, "A method for speed optimized partial product reduction and generation of fast parallel multipliers using an algorithmic approach," *IEEE Trans. Comput.*, vol. 45, no. 3, pp. 294–306, Mar. 1996.

[17]. JipsaAntony1 ,Jyotirmoy Pathak2, "Design and Implementation of high speed Baugh-wooley and modified booth multiplier using cadence RTL " IJRET: International Journal of Research in Engineering and Technology eISSN: 2319-1163 | pISSN: 2321-7308.

[18]. "Design of Low Power Booth Multiplier Based Reconfigurable FIR Filter for DSP" Applications S.Chinnapparaj1,R.Arulmozhi2 , M.Infant Priya3 , S.Jayadharany4 , C.Kothai5. International Journal of Engineering Science and Computing, April 2018.

[19]. "Design of Baugh-wooley Multiplier using Verilog HDL" Shruti D. Kale, Prof. Gauri N. Zade IOSR Journal of Engineering (IOSRJEN) www.iosrjen.org ISSN (e): 2250-3021, ISSN (p): 2278-8719 Vol. 05, Issue 10 (October. 2015), ||V2|| PP 25-29.

[20]. H. Eriksson, P. Larsson-Edefors, M. Sheeran, M. Själander, D. Johansson, and M. Schölin, ―Multiplier reduction tree with logarithmic logic depth and regular connectivity,‖ in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2006, pp. 4–8.

[21]. PramodiniMohanty., ―An Efficient Baugh-Wooley Architecture for both Signed & Unsigned Multiplication‖ International Journal of Computer Science & Engineering Technology (IJCSET) Vol. 3 No. 4 April 2012.

[22]. Steve Hung-Lung Tu., Chih-Hung Yen., ―A High-Speed Baugh-Wooley Multiplier Design Using Skew-Tolerant Domino Techniques‖ IEEE 2006.

[23]. M. Hatamian, ―A 70-MHz 8-bit x 8-bit Parallel Pipelined Multiplier in 2.5-µm CMOS,‖ IEEE Journal on Solid-State Circuits, vol. 21, no. 4, pp. 505–513, August 1986.

[24]. M. Själander, H. Eriksson, and P. Larsson-Edefors, ―An efficient twin-precision multiplier,‖ in Proc. 22nd IEEE Int. Conf. Comput. Des, Oct.2004, pp. 30–33.

[25]. M. Själander and P. Larsson-Edefors, ―The Case for HPM-Based Baugh-Wooley Multipliers,‖ Department of Computer Science and Engineering, Chalmers University of Technology, Tech. Rep. 08-8, March 2008.

[26]. Hsing-Chung Liang, Pao-Hsin Huang, and Yan-Fei Tang ―Testing Transition Delay Faults in Modified Booth Multipliers‖ IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 27, No. 9, September 2008.

[27]. W.-C. Yeh and C.-W. Jen, ―High-Speed Booth Encoded Parallel Multiplier Design,‖ IEEE Transactions on Computers, vol. 49, no. 7, pp. 692–701, July 2000.

[28]. Shiann-RongKuang, Jiun-Ping Wang, AndCang-Yuan Guo ―Modified Booth Multipliers With A Regular Partial Product Array‖ IEEE Transactions On Circuits And Systems—Ii: Express Briefs, Vol. 56, No. 5, May 2009.

[29]. Hsing-Chung Liang, Pao-Hsin Huang, and Yan-Fei Tang ―Testing Transition Delay Faults in Modified Booth Multipliers‖ IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 27, No. 9, September 2008.

[30]. M. Sjalander and P. Larsson-Edefors, "High-speed and low-power multipliers using the Baugh-Wooley algorithm and HPM reduction tree," 15th IEEE International Conference on Electronics, Circuits and Systems, 2008.