INTERNATIONAL MICROELECTRONICS AND PACKAGING SOCIETY

San Diego Chapters

Tuesday, August 29, 2017 at 12:00

Technical presentation and lunch

CPI & CBI Risks to FOWLP

Presented by

Mark Nakamoto

(Qualcomm Package Engineering Organization)

Abstract: With the advent of thinner die/packages, new materials and more complex packages Chip Package Interaction(CPI) has become a larger concern for the industry. As the name implies CPI has traditionally been viewed as a component level concern. Wafer Level Packages and variants such as Fan Out Wafer Level Packages (FOWLP) now bring an additional risk which we refer to as Chip Board Interaction. This talk will discuss some of the basics of the CPI and CBI risks to FOWLP which include both mechanical and electrical risks to products. These mechanisms span the Design, Process and Package domains and as such requires collaborative efforts to manage the risks and trade-offs.

Biography: Mark Nakamoto currently is a member of Qualcomm's Package Engineering Organization. He leads the eCPI Team working on the development of Modeling, Characterization and Analysis of the electrical impacts of Chip Package Interaction. Mark has over 30 years of experience in the Semiconductor Industry spanning Silicon Process Development, Process and Device Characterization, Test Structure Design, Reliability, Modeling, Design for Manufacturability, 2.5D and 3D Development and Chip Package Interaction. Prior to Qualcomm Mark held various positions in PDF Solutions, Cadence Design Systems, and Unisys/Burroughs.

Logistics:

Tuesday, August 29th at 12:00 PM. Lunch will be provided.
Location: Kyocera, 8611 Balboa Avenue, San Diego, CA 92123

RSVP required.

$20.00 for IMAPS members. $25.00 for non-members. Free for students with an ID. Please advise if you are non-U.S. citizen when you register. To register and pay online (preferred), please click HERE, or to register via email please contact Iris Labadie ----- iris.labadie@kyocera.com or call 858-614-2592.