XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

1. Background

Designers of RF circuits face diminishing returns when choosing GaN HEMTs for their next generation power products. The superior attributes of GaN over the established realm of LDMOS and Bipolar loses some of its luster when the biasing difficulty is factored in for depletion mode devices. Putting smart circuitry to ensure that GaN HEMTs are safe and unconditionally stable becomes a daunting task to begin with, let alone dealing with the high cost of accommodating several IC components to share space fraught with EMI and RFI. The situation demands a multilayered PCB solution.

But the sensible solution is to let the PCB remain as a 2-layer RF laminate and dropping-in tiny controller and switch modules that take advantage of tight spaces and simple printed line interconnects. A significant reduction of cost and complexity will be apparent in "black box" documentation, parts procurement, assembly, and test.

2. Controller I/O Table

Before we start interconnecting, lets become familiar with the module inputs and outputs. From the table below, reference each label, pin, and description to the schematic and outline drawings in coming pages . Refer to the Product Flyers for more details.

LABEL	PIN 100X 200X	PIN 100L 200L	DESCRIPTION
NTP	1	17	Aux Negative Voltage Tap
VN6	2	1	Optional Neg (-) Supply
POT	3	2	Gate Voltage Input Adjust
PGA	4	3	Pulsed Gate Voltage Out
FGA	5	4	Fixed Gate Voltage Out
GND	6	5	Ground
POT	7		Connected to Pin 3
PTP	8		Aux Positive Voltage Tap
GTL	9	6	Gate Pulse Logic Enable
DTL	10	7	Drain Pulse Logic Enable
VP4	11	8	Optional Logic (+) Supply
OTL	12	9	Active-Low TTL Driver
GND	13	10	Ground
DFB	14	11	MOS Drain Feedback
DRV	15	12	Open Drain MOS Driver
VDS	16	13	High Voltage Supply
REG	17	14	Aux Regulator Output
SHD	18	15	Aux Gate Threshold Adj
PTP	19	16	Aux Positive Voltage Tap

3. Controller I/O Pin Descriptions

WARNING
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

NTP has –4.3V output from a voltage inverter. Tap with >10KΩ trim-pot to establish (-) input to POT pin of the 100 Series only. Otherwise, leave open.

VN6 input is connected to an optional negative supply of > –6V if gate current boost of 100mA is needed for saturated GaN. Internally, there's 30mA. Leave open otherwise.

POT input receives negative voltage for 100 Series or positive voltage for 200 Series. This unity gain buffer provides negative bias to the transistor gate. Temperature-compensation voltage is added here as well.

PGA output produces a square-wave triggered by TTL to pin GTL. It provides gate bias to GaN at a level set from POT pin and down to V_pinchoff established from either the voltage inverter (-4.3V) or from pin VN6.

FGA output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

PTP has +5.0V output from a voltage regulator. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 200 Series only. Otherwise, leave open.

GTL input takes active-low, TTL signal (<4.7V) to control gate switching of the device. It is tied to DTL pin to sequence the gate and drain voltage. This is not used for sub-models. Disconnect from DTL for independent control.

DTL input controls the drain switching end of the transistor. When tied with GTL, the active-low TTL enable switches drain voltage ON and would remain there until gate voltage undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during ramping Vdd up & down.

VP4 input is connected to an optional supply of ≤ +5V. Leave open unless required by sub-models.

OTL output is an active-low TTL drive signal reserved for 300 Series Power CMOS switches. Leave pin open otherwise.

DFB input monitors the presence of drain voltage when the MOS switch is ON. Use if gate switching is desired; otherwise, leave open for sub-models.

DRV output connects to the gate input of MOSFET switch module. Connect to multiple switches with up to 300mA total loads.

VDS input receives from the same supply that powers the GaN.

REG is an auxiliary port of +5.7V from a voltage regulator.

SHD is an auxiliary port for adjusting the gate voltage shutdown threshold. From this node, connect 100KΩ-1MΩ resistor to REG (or PTP) ports for increasing the threshold level, or to GND for decreasing said level.

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3. Switch I/O Pin Descriptions

I/O TABLE: 400 SERIES	
INP	INPUT FROM CONTROLLER DRIVER
GND	GROUND
OUT	OUTPUT TO MOSFET GATES
VG1,VD1,VS1	GATE, DRAIN, SOURCE OF MOS #1
VG2,VD2,VS2	GATE, DRAIN, SOURCE OF MOS #2
VDS	POSITIVE VOLTAGE SUPPLY

I/O TABLE: 300 PNC SERIES	
DRA	DRAIN
GND	GROUND
G A	GATE IN, CMOS
G I	GATE IN
G C	GATE CAP
G V	GATE 15V
SOU	SOURCE

INP input connects directly to the Controller DRV output.
OUT is a low-side driver output which connects to MOSFET gates VG1 and VG2.
VG1, VG2, GA are gate inputs that receive signals from DRV or OTL outputs of the Controller. For a general purpose switch like the 410, the DRV pin can be tied to VG1 & VG2, while bypassing INP & OUT pins.
GI, GC, GV are interdependent gate inputs that connect matching pins of complementary switch pairs. Only when using a single switch that GI and GC are tied together.
VD1, VD2, DRA are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
VS1, VS2, SOU are source inputs that take up to +65V supply. Larger storage capacitance are attached here.

4. Functional Diagrams

The following circuit diagrams are just a sampling of the numerous configurations the Controller and Switch can work for your application. The base model Controller like the 100 & 200 are the most universal, meaning they have the most features that can be utilized or ignored. Sub-categories of these are budget models that have certain features removed for a simpler, more specific application.

The primary function of the Controller is a bias sequencer. Gate voltage is delivered to device before drain voltage and remains there until the drain side has no more potential. The Switch stands ready for shutdown when GaN safety is compromised. The secondary function is to control the Switch with PWM/TTL signals and deliver high-voltage/high-current/high-speed square pulses to power-up or modulate the RF device. Drain switching can also be left in the ON-state indefinitely by grounding the pulse enable pin. The tertiary function is the ability to control gate voltage switching independently or slave to drain switching. In addition to added stability mentioned previously, pulse-shaping can be introduced with gate control.

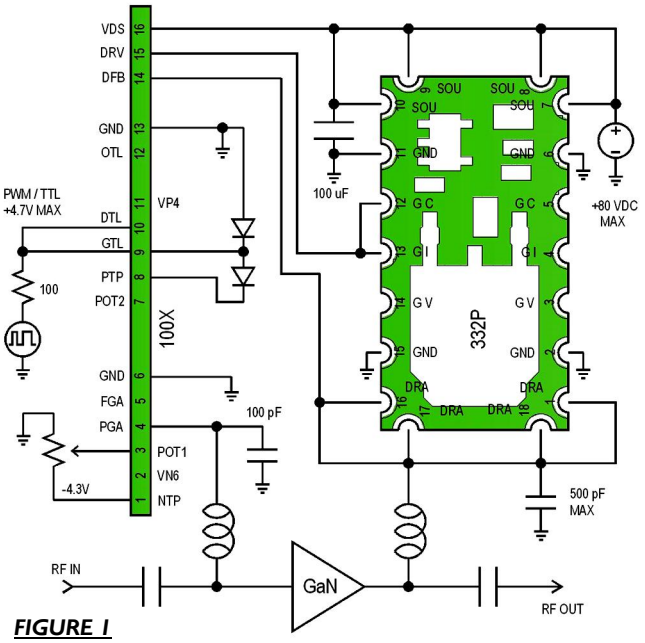

FIGURE 1

The circuit in Figure 1 uses a non-inverting controller, 100X and paired with a pulsed switch 332P. A single power source is used; therefore, gate current from internal inverter is limited to 30mA available to GaN. In cases where negative supply is accessible, the potentiometer should give relief to the negative tap, NTP. There are general purpose switching diodes that protect the TTL inputs from transients, signal level changes, and negative sources.

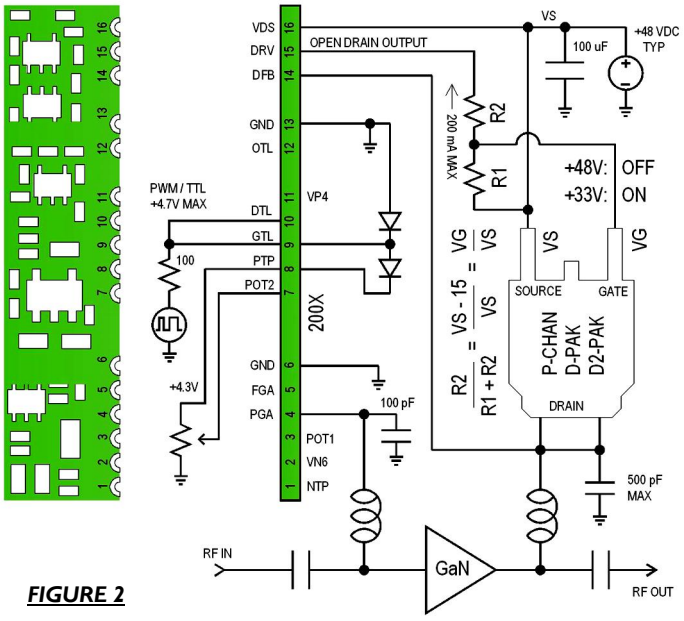

FIGURE 2

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The circuit in Figure 2 has a 200X inverting controller driving a general purpose PMOS transistor. The switch operating in CW is typically used for pulse periods beyond 5msec. The value and rating of the pair of resistors R1 & R2 depend on how much current to draw for increased switching speed. The DRV output of the controller should not exceed 100mA of sink current. A potentiometer taps into the positive auxiliary port to generate an operating gate voltage. This combination also relies on a single power source.

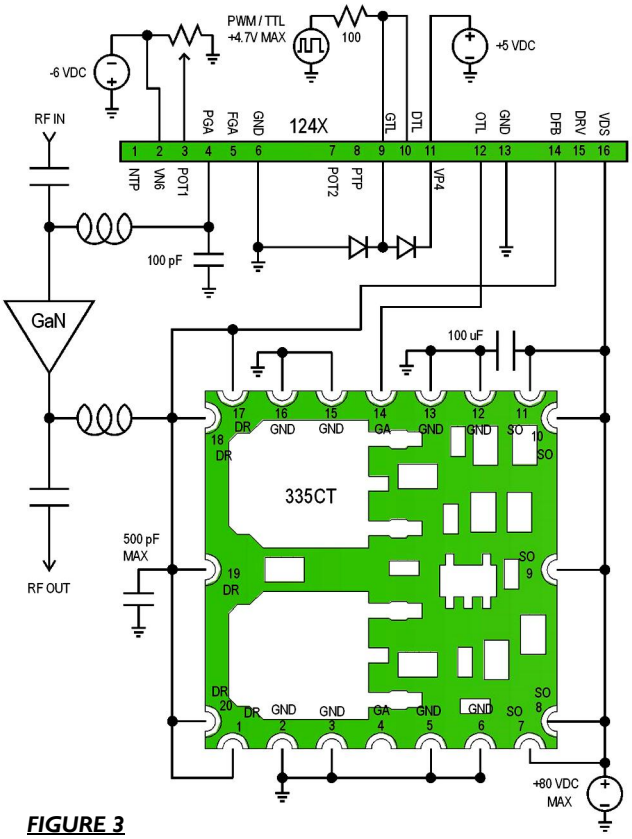

FIGURE 3

A Complementary MOS (push-pull) switch is illustrated in Figure 3 with a power CMOS 335CT controlled by a basic sequencer 124X. The advantage of a P & N-Chan pair is mainly to "pull-down" the drain voltage from say 50V down to 0V as quickly as possible with no significant decay normally seen with single MOSFET switches. Structured rise and fall times (<<200nsec) make for a well controlled spectral characteristic. The negative supply also provides boost current to the gate of a GaN transistor in saturation.

A 220X controller with no gate switching feature drives a 410X dual switch in CW, as shown in Figure 4. The objective is that one switch controls the high-power, final amp stage, while the other switch handle two driver amp stages. While it's possible to tie the gates of three transistors from one controller, their gate impedances may adversely affect their individual bias points and cause current imbalances. It's better practice to buffer each device gate with voltage follower or adjustable gain op-amps.

Even though the controller's fixed or pulsed gate output is able to handle a few device loads, remember that the inverter of the 200X is limited to 30mA unless an external negative source is connected to provide a boost of up to 100mA. Also, having op-amp buffers will further extend the current limit for up to 100mA per buffer, which is a welcome source for applications with saturated GaN transistors.

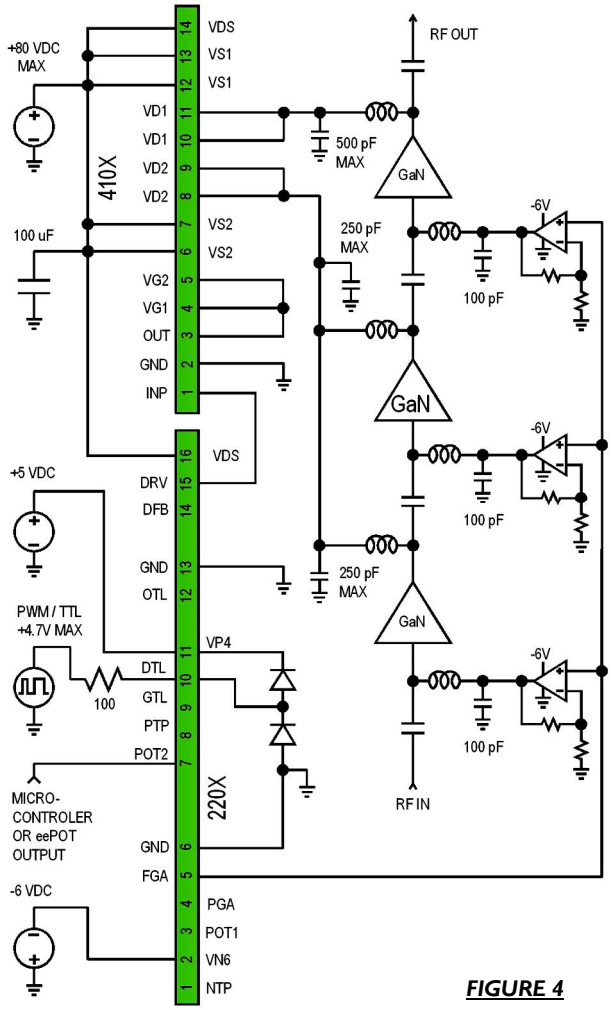

FIGURE 4

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5. More Application Diagrams

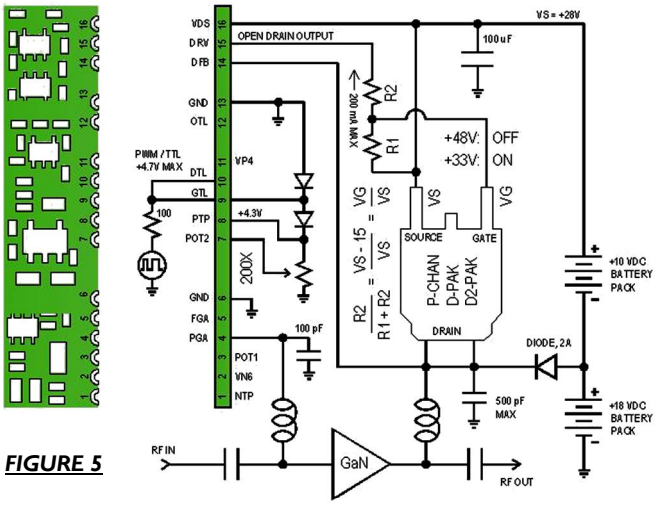

FIGURE 5

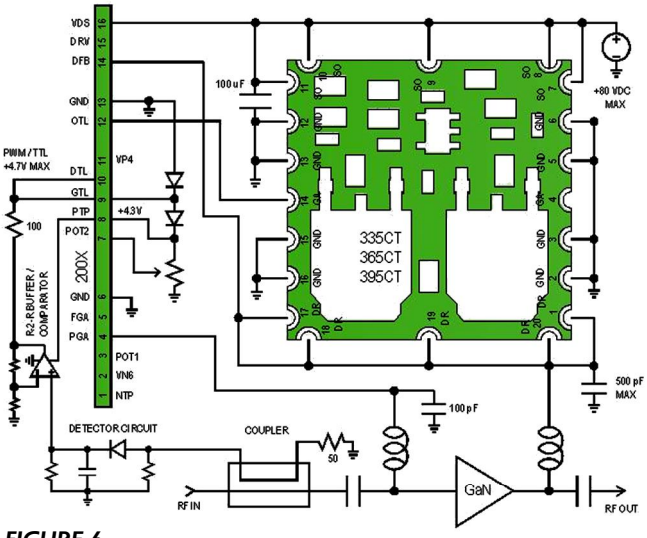

FIGURE 6

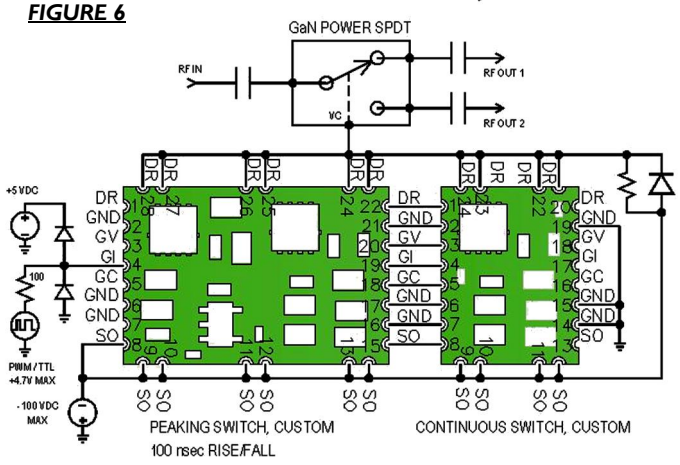

FIGURE 7

The diagrams on the left are customer applications utilizing the Controller and Switch for specific tasks. Figure 5 is a high-efficiency, dynamic drain voltage that provides two power settings for transmitters of emergency radio packs. This concept can also be applied to RF signals with high peak-to-average ratios (PAR). Figure 6 is a kW-level amplifier with short, high-speed pulses. It does not rely on a TTL trigger, but instead, RF is automatically detected and enables the power sequence of the device. Figure 7 is an ultra-high speed driver for a GaN-based SPDT Switch. It uses a peaking-switch with ON & OFF speeds of <100nsec. Then a continuous-switch maintains its state. This customized pair can also be configured for PIN diodes of Silicon or GaN variety.

6. Drop It, Set It , & Forget It

When making a printed circuit board becomes too much of a commitment and fast prototyping is needed to prove a concept, then a drop-in Evaluation Board would make more sense. They provide the quickest and complete solution for proper GaN operation. Figure 8 shows a variety of devices controlled with a tiny 600E Series drop-in, eval board mounted next to it. These also come with castellation for surface-mounting on production units. The CW modules shown below are equivalent to the schematic diagram in Figure 2, page 2. The MOS switches have 12A and 36A peak, with 6A and 16A average capacity respectively.

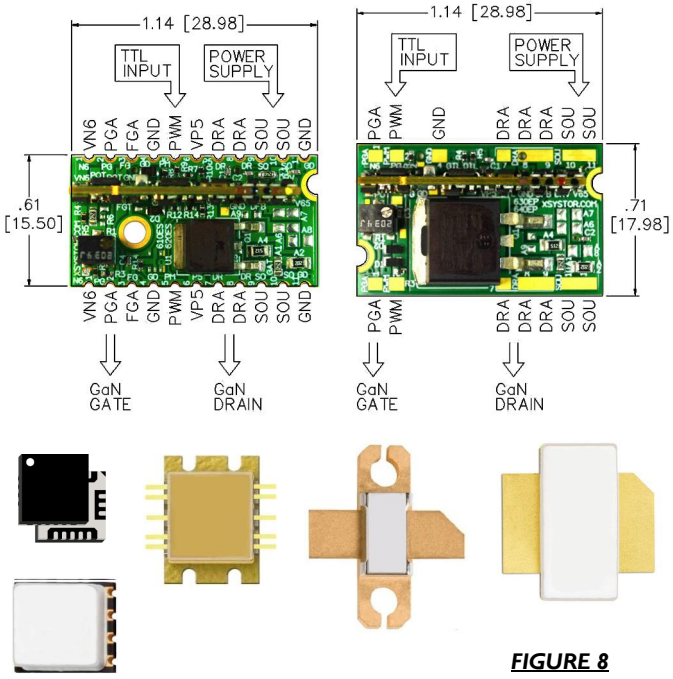

FIGURE 8

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5. Start-up and Operation

Prior to any power start-up, the following must be taken into account and double-checked.

- *Perform continuity tests of all connections leading to the gate and drain sides of the transistor.*
- *Disconnect all DC supplies and signal inputs. Then measure proper output levels. Prevent recall commands from instruments which could be inadvertently summoned with destructive results, like excessive drain & gate voltages as well as non-TTL signals.*
- *Refer to the I/O pin descriptions on the first page. As a default, leave unused pins open.*
- *Practice safe handling and prevent ESD damage.*

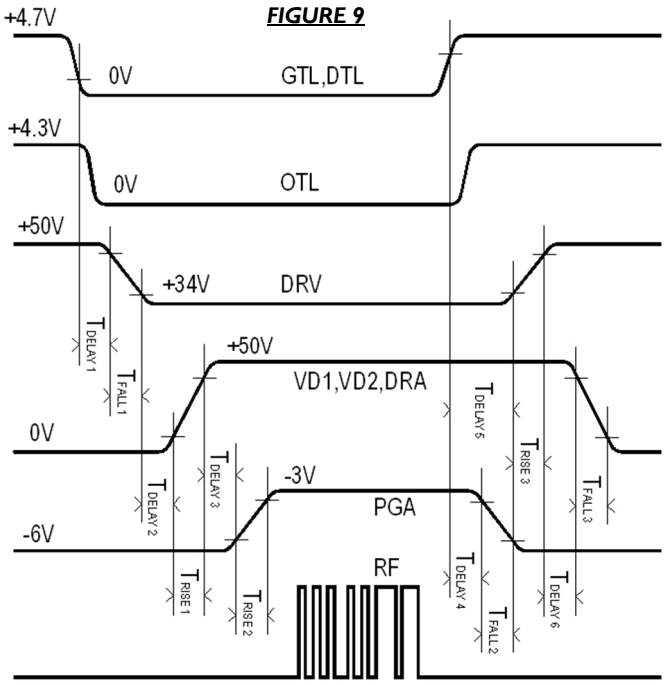
The controller will protect the GaN device from any sequence of power-up and power-down activity, provided the connection to device gate is solid. The negative supply is turned ON first. In cases where negative voltage is generated by the controller, the main power supply can be turned ON, but ONLY if power is disconnected firsthand from reaching the GaN drain physically. When the proper gate level is established with the potentiometer and measured at the device port, only then should drain voltage be turned ON or reconnected. As a matter of habit during operation, negative voltage should be first in and last out, and the controller may only provide back-up protection.

An alternative test method for initial operation of controller & switch is to temporarily take out the GaN device and replace with resistive and capacitive loads. As a starting point, refer to the spec sheets which assumes a gate load of 2.7KΩ + 500pF and drain load of 1.0KΩ + 500pF. Once the proper signals are established, the GaN device may be reinstalled.

6. Timing Diagrams

The timing sequence in Figure 9 illustrates a master-slave relationship of drain-gate switching with the 100 or 200 Series Controller connected to the 300 or 400 Series Switch. To do this, the gate switch enable pin (GTL) is tied or synchronized with drain switch enable pin (DTL), and then started up with an active-low TTL signal. The controller produces an optional TTL output (OTL) and an open-drain current drive (DRV). Then the MOSFET switch turns ON and supplies power to the transistor (from VD1, VD2, or DR).

FIGURE 9



Only with the presence of drain voltage would the gate switching feature activate (PGA), and finally turns on the GaN device for RF to transmit. The sequence is finished with the rising end of the TTL signal. The pulsed gate (PGA) goes back to pinch-off voltage and drain voltage (VD1, VD2, DR) shuts down thereafter. Note that the total ON propagation time from TTL to RF is the sum of time delays, rise times, and fall times shown in the diagram. Total propagation times of <500nsec are common.

FIGURE 10

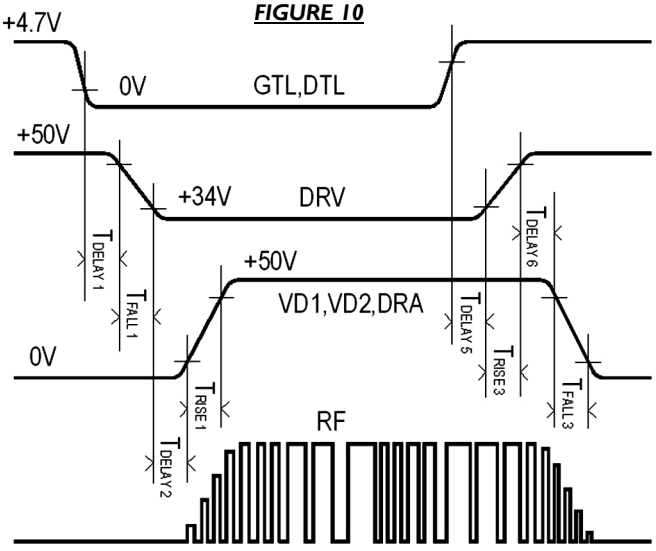


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Figure 10 has a timing sequence that's typical of sub-models like the 124/224 with no gate switching capability. Gate bias is left as a fixed value, so drain voltage activity turns the GaN device ON and OFF . This particular diagram shows a CW RF to be pulse modulated. In a different scenario when gate switching is available, we can fix the drain voltage to a steady state and pulse the gate bias instead to get a similar result. Either way, the gate (GTL) and drain (DTL) enable pins are really independent and will cater to various customer preference.

7. Temperature Compensation

This subject is best described in its own application note, but some general functionalities will be noted here. The 100 & 200 Controllers have two provisions to add temperature compensation. The first is adding a specific thermistor to the unit. This is a custom feature not included in the standard fare. Though handy, the sensing component is far removed from the base plate or heat source, and may require over-compensation to work.

The second way is installing a familiar temperature sensor IC or discrete circuit near the device and feed its resultant voltage to the controller input, POT. This same pin is also connected to the potentiometer that established the operating gate bias. Now the two signals are combined by an op-amp adder circuit to produce a composite negative voltage for the GaN device. Series resistors for each voltage inputs are first calculated to regulate the impact of the variable voltage from the sensor.

In general, typical temp sensors have positive voltage outputs; therefore, the 200 Series Controllers are more apt to the task to share the POT pin for positive inputs.

8. Mounting Considerations

The 100X/200X controllers and the 400X switch have very small footprints considering they are mounted upright on the receiving board. The I/O ports are castellated holes with a 50 mil pitch. The "L" models have a lower profile of 0.20" height with castellation at 60 mil pitch. The "T" models have 0.10" long terminal pins at 50 mil pitch that would make them stand on their own. Though reflow soldering is acceptable to mount them, care should be taken that a large temperature gradient at the top of the units may dislodge components or worst burn them. At this time, manual installation is recommended with lead-free solder at <230°C, otherwise the reflow process is appropriate at <195°C.

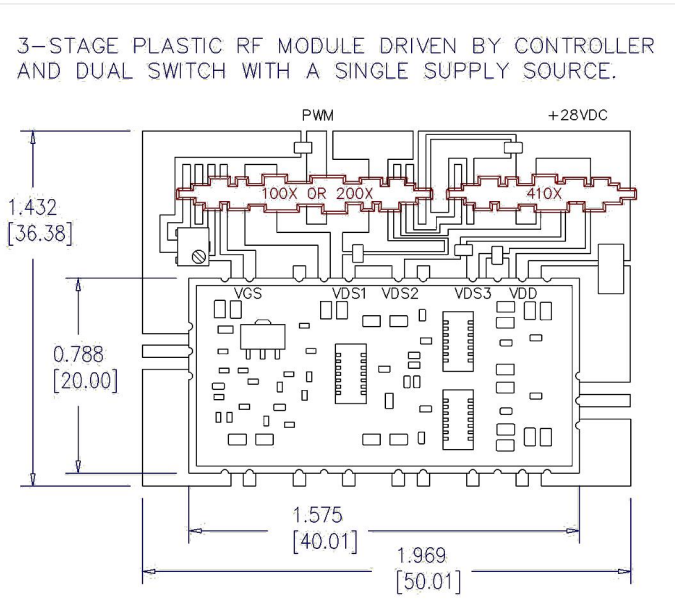
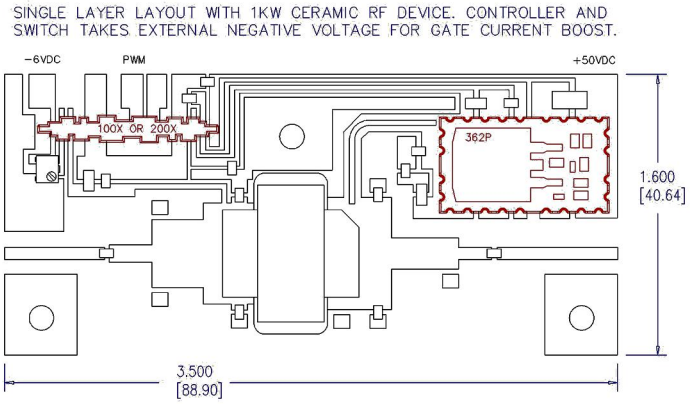


FIGURE 11

Ideal placement for controllers is on the gate side of transistor while MOSFET switches on the drain side, as shown on Figures 11 and 12. The units should be as close to the device to minimize parasitic inductance from supply lines. The drain side is especially susceptible to large voltage spikes if there's significant distance between the RF choke and the switch.

In cases where system requirements have tougher height restrictions from components, the 100X & 200X controllers are better suited to address this. The units can be installed in three ways, which are upright, slanted, and flat & buried. A resultant height of 0.10" [2.54mm] can be realized from the board surface. This is illustrated in the application note XAN-4: Mounting schemes for the Controller.



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9. Adjusting Gate Threshold Shutdown

The 100/200 Series Controllers come in presets of –2.6V, -2.0V, -1.4V, or -0.8V thresholds at the device gate, where drain voltage is shutdown when these levels are reached. The device gate operating voltage or quiescent voltage is typically 0.5V lower than these presets. The user has the option to adjust them when necessary to precisely trigger a shutdown event and protect the GaN transistor from excessive current or runaway. Figure 13 illustrates the tap points of resistors R1, R2, or R3 when increasing or decreasing the preset voltages with a single resistor. Refer to Page 1 for the pin descriptions. Always shutdown power to the Controller when soldering new components.

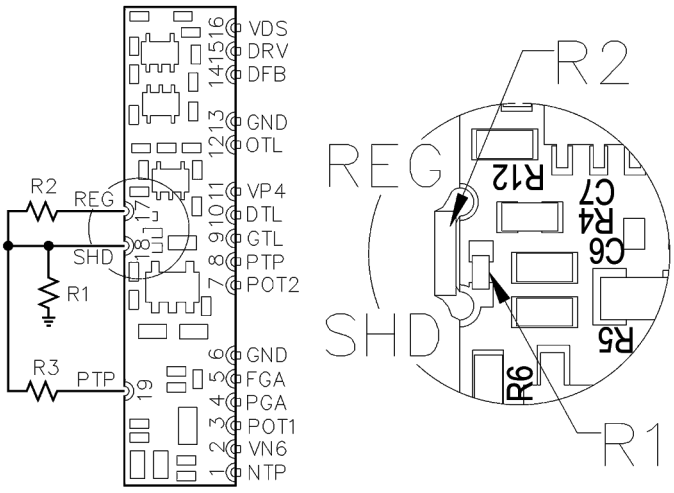

FIGURE 13

If chip resistors are preferred, the placeholder for R1 will fit an 0201 size. R2 will fit 0603 or 0805 size, and soldered on top of the unit between pins REG and SHD. On the other hand, a simpler approach to tapping these points is by using small axial resistors between 100KΩ and 1MΩ. The table below shows resistance values needed to increase or decrease the threshold presets.

	R1 (Ω)			R2 or R3 (Ω)		
ADJUST →	-0.4 V	-0.2 V	-0.1 V	+0.1 V	+0.2 V	+0.4 V
PRESETS↓						
-2.6 V	120K	240K	480K	620K	310K	150K
-2.0 V	140K	280K	580K	600K	300K	150K
-1.4 V	140K	280K	580K	500K	250K	125K
-0.8 V	140K	280K	580K	400K	200K	100K

10. Controller Selection Guide

MODEL	DESCRIPTION
100X, 100T, 100L	100X, 100T, & 100L ARE IDENTICAL FUNCTIONALLY BUT DIFFER STRUCTURALLY. SUFFIX 'T' STANDS FOR TERMINAL PINS AT 50 MIL PITCH, WHILE 'L' FOR LOW PROFILE AT 60 MIL PITCHED CONNECTIONS. 'X' IS STANDARD CONFIGURATION. THE 100X & 100L MOUNT ON PCB FROM CASTELLATED I/O PORTS. THESE UNITS CONTROL THE GaN TRANSISTOR BY SWITCHING THEIR DRAIN AND GATE SUPPLIES SEQUENTIALLY OR INDEPENDENTLY. A SINGLE SUPPLY OF UP TO +65V IS SUFFICIENT TO OPERATE. THE 100 SERIES HAVE NON-INVERTING INPUTS, WHICH MEANS IT TAKES NEGATIVE VOLTAGE TO PRODUCE NEGATIVE GATE BIAS TO THE
120X, 120T, 120L	SAME AS THE 100 SERIES BUT WITHOUT GATE SWITCHING CAPABILITY. A FIXED GATE BIAS VOLTAGE IS UTILIZED INSTEAD.
122X, 122T, 122L	SAME AS THE 100 BUT WITHOUT GATE SWITCHING AND VOLTAGE INVERSION. A NEGATIVE SOURCE IS SUPPLIED BY THE USER.
124X, 124T, 124L	THIS MODEL IS A BASIC GaN SEQUENCER/MODULATOR. THERE ARE NO GATE SWITCHING, VOLTAGE INVERTER, AND LOGIC SUPPLY. THE USER BASICALLY PROVIDES THE NECESSARY DC SOURCES THAT'S ALREADY IN THEIR SYSTEM.
200X, 200T, 200L	200X, 200T, & 200L ARE THE SAME AS THEIR COUNTERPARTS ABOVE EXCEPT THAT THEY HAVE INVERTING INPUTS. IT TAKES POSITIVE VOLTAGE TO PRODUCE NEGATIVE GATE BIAS TO THE
220X, 220T, 220L	SAME AS THE 200 ABOVE BUT WITHOUT GATE SWITCHING CAPABILITY. A FIXED GATE BIAS VOLTAGE IS UTILIZED INSTEAD.
222X, 222T, 222L	SAME AS THE 200 BUT WITHOUT GATE SWITCHING AND VOLTAGE INVERSION. A NEGATIVE SOURCE IS SUPPLIED BY THE USER.
224X, 224T, 224L	THIS BASIC SEQUENCER/MODULATOR HAVE NO GATE SWITCHING, VOLTAGE INVERTER, AND LOGIC SUPPLY. THE USER PROVIDES ALL DC SOURCES ALREADY PRESENT IN THEIR SYSTEM.

11. MOS Switch Selection Guide

MODEL	DESCRIPTION
332P	SINGLE 12A SWITCH MODULE FOR PULSED APPLICATIONS.
332N	ADD-ON TO 332P FOR A COMPLEMENTARY CONFIGURATION.
335CT	12A POWER CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
362P	SINGLE 36A SWITCH MODULE FOR PULSED APPLICATIONS.
362N	ADD-ON TO 362P FOR A COMPLEMENTARY CONFIGURATION.
365CT	36A POWER CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
392P	SINGLE 8A SWITCH, MINI-MODULE FOR PULSED APPLICATIONS.
395CT	8A MINI CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
410X, 410T, 410L	HAS DUAL 8A MOSFET SWITCHES FOR CW OR GENERAL PURPOSE OPERATION. 410X, 410T, 410L ARE IDENTICAL FUNCTIONALLY BUT DIFFER STRUCTURALLY. SUFFIX 'T' STANDS FOR TERMINAL PINS AT 50 MIL PITCH, WHILE 'L' FOR LOW PROFILE AT 60 MIL PITCHED CONNECTIONS. 'X' IS STANDARD CONFIGURATION. THE 410X & 410L MOUNT ON PCB FROM CASTELLATED I/O PORTS.
420X, 420T, 420L	HAS DUAL 8A MOSFET SWITCHES FOR PULSED APPLICATIONS. LIKE THE 410 AND 430, THEY ARE SMALLER THAN THE 100/200 CONTROLLER MODULES AND WORK WELL IN TIGHT SPACES.
430X, 430T, 430L	THE 8A P-CHAN & N-CHAN MOS SWITCHES ARE COMPLEMENTARY AND WORKS LIKE A PUSH-PULL. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE AND FALL TIME REQUIREMENT.