Implementing High Speed Novel Architecture of Maskable Adder using Hdl

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Abstract- Multimedia applications are becoming increasingly popular. a perfect result is not needed in some applications approximate result is also sufficient. Hopefully there are some approximate adders giving approximate result. There are some applications that can withstand error . one of the application we use is a search engine, and we get the approximate results.This is used to reduce disability.Here We provide approximation using Maskable signal. we get the approximate results. When the maskable signal is zero, we get both approximate and accurate results. We implement approximate adder with koggy stone adder which is parallel prefix adeder.koggy stone is a fast adder. We apply a masking signal at the initial pre computation stage, rather than using half adder. using this approach we achieve a high speed adder compared with the previous adders. We use Verilog tool to implement this method in the Xilinx tool

Keywords- Approximate adder ,maskable signal ,koggy stone adder, parallel prefix adder.

I. INTRODUCTION

Recent applications (Such as image recognition,audio,video which require battery power) created power consumption problems. Addition is the basic function in many applications.there are some error tolerant applications.these applications have tolerance for inaccurate values. So for these applications we can use approximate adders. currently these adders have major importance for such applications [3]. For the sake of quality, the computation requirements vary considerably depending on the execution time. It is desirable to develop a customizable quality system that operates according to application requirements, with qualitative and computational power [4] [5]. The earlier configuration offers increased delay [12].

In order to benefit such application, a low-power and high-speed adder for configurable approximation is strongly required. In this paper, we propose a high speed maskable configurable approximate adder. Which has the delay observed with the proposed adder is much smaller than that of the previous adder.

A customizable approach is required to develop a high speed adder.In this paper, we propose a high speed maskable approximate adder. The delay of the proposed adder is much smaller than that of the previous adder.

Our Primary aim is to achieve accuracy configurability the proposed adder achieved the optimization of delay. We implemented the proposed adder, with the koggy stone adder which is a parallel prefix form of CLA developed by Kogge and Stone in 1973. It creates a carry in O (logn) time. It is generally used in the industries as a high speed adder, we impement the design using 45nm library Verilog HDL.thus we evaluate the comparisions for the delay and area for the existing carry look a head adder to proposed koggy stone adder which has less delay.we implement the maskable half adder in pre computation stage of koggy stone adder

II. RELATED WORK

Gupta et al. [6] describe how to simplify the transistor cell level in a normal mirror head. Mahdiani et al proposed the lower or gate adder. Venkatesan et al. [8] proposed an adder represents the behavior of the approximate circuit.the above approximate designs are fail to meet the requirements of the circuit. Kahn et al. [4] proposed accuracy configurable adder using the pipeline structure .The correction scheme of the ACA proceeds from stage 1 to stage 4,, all the four stages should be performed. Motivated by the above, Ye et al. [5] proposed an accuracy gracefully-degrading adder which allows the accurate and approximate sum.Exiting approximate adder uses a carry look a head adder, consists of three parts: half adders for propagation generation., carry look-ahead units for carry generation, and XOR gates for sum generation using propagate and generate terms. It focus on the half adders for G and P signals in the circuit.using the maskable signal we get the approximate and approximate result.

When the maskable signal is ‘0’ carry will be zero we get the approximate result and when maskable signal is ‘1’ we get the accurate result .In propagation geneeration of half adders existing adder usesv a maskable half adder and uses the carry look a head adder for carry generation and then by using the xor gates generates the sum .but implementing the maskable half adder in the high speed adder like parallel prefix adderwe achieve the high speed adder.we propose a koggy stone adder with the maskable signal to get the accurate and approximate result

Exiting approximate adder uses a carry look a head adder, a CLA consists of three parts: (1) half adders for carry generation (G) and propagation (P) signals preparation, (2) carry look-ahead units for carry generation, and (3) XOR gates for sum generation. It focus on the half adders for G and P signals preparation in part 1.using the maskable signal we get the approximate and approximate result.

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III. PROPOSED APPROXIMATE ADDER

Adders are the basic components in the digital computer systems due to their fast functionality in their work. The main purpose of these adders is to calculate the address in quick time. Among all the adders Parallel Prefix Adder is the main useful adder. Kogge Stone Adder is one of the common types of parallel prefix adder. Kogge – Stone adder has been developed by Xilinx 14.3 software which is more advantageous and more developed. If the complete operation is leaded by the inputs of the initials, that is called prefix. If the operation is integrated in parallel This will be done by making the operation into some small pieces. The main benefit in this technique is that the operation or the calculation part will be completed in parallel direction. The former calculating techniques will make the calculations in one by one process. But in this technique the calculations will be considered in parallel condition. The lot of time can be saved. Parallel Prefix Adder (PPA) will be divided into three parts, i.e., prepossessing stage, carry generation network and post-processing. Prepossessing stage is to calculate, produce and spread the signals. Carry generation network is to calculate the values in parallel level and these calculations will be segmented in minute pieces. Finally, the Post-processing stage is to complete the calculation part by collecting all the bits.

Koggy stone adder has three stages

[1]. Pre- processing stage
[2]. Carry generation network
[3]. Post processing stage.

a) PRE-PROCESSING STAGE:

In the pre-processing stage, produce propagate and generate from each pair of inputs. The propagate gives the operations of XOR‖ of input bits and generates gives AND‖ operation of input bits.In the pre processing stage we use maskable adder instead of half adder.

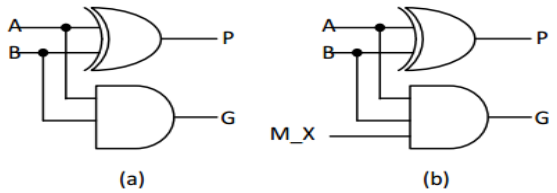

Fig.1: (a) an accurate adder and (b) a half adder with a select signal

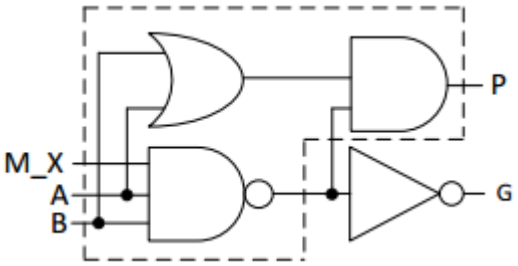

Fig.2: carry mask able adder

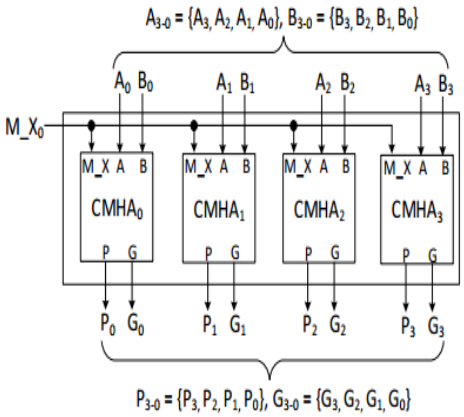

Fig.3: structure of a group of four CMHAs.

In other words, we can obtain the selectivity of S between the accurate and approximate sum if we can control G to be A AND B or 0.so we can achieve selectivity by adding a select signal. Figure 1(a) is a conventional half adder and Fig. 1(b) is a half adder to which the select signal has been added. Compared with the conventional half adder, we add a signal named "M_X" as the select using a 3-input AND gate to replace the 2-input one. When M_X = 1, the function of G is the same of a half adder .when

P = A xor B
G=A.B

when M_X = 0, P is equal to A OR B and G is 0. Thus, M_X can be considered as a carry mask signal.this process is done in the square box.

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a) CARRY GENERATION STAGE:

At this stage, every carry is generated for each bit and this is called as carry generate. The carry propagate and carry generate is generated for the further operation but final cell in the each bit process gives carry. The last bit carry will help to make sum of the next bit concurrently till the last bit. The carry generate and carry propagate are specified in below equations.

Cp= p1 and p0
Cg=g1 or (p1 and g0)

The above carry propagate Cp and carry generation Cg in equations is done in the black box.In the carry generation stage has two cells one is black cell and another one is gray cell.black cell have two outputs propagate and generate.gray cell generates only one output this is generate signal. The carry propagate is generated for the additional process but final cell present in the each bit operation gives carry. The last bit carry will help to create sum of the next bit concurrently till the last bit. This carry is used for the next bit sum procedure

b) POST-PROCESSING STAGE:

It is the last stage of the propagate bit is xored with carry bit generated in the carry generation stage then the output is given as sum and it is shown in equation

SUM = Pi xor gi pre_last

The proposed koggy stone adder uses maskable half adder in the square box which is the pre computation stage to generate propagate and generate signals and these signals are given to the blackdot which is used for carry generation ,buffer is used as wire signal it is usede to transfer signals from one to another.diamond is sed for the sum generation.the proposed adder has the less delay compared to the existing adder.

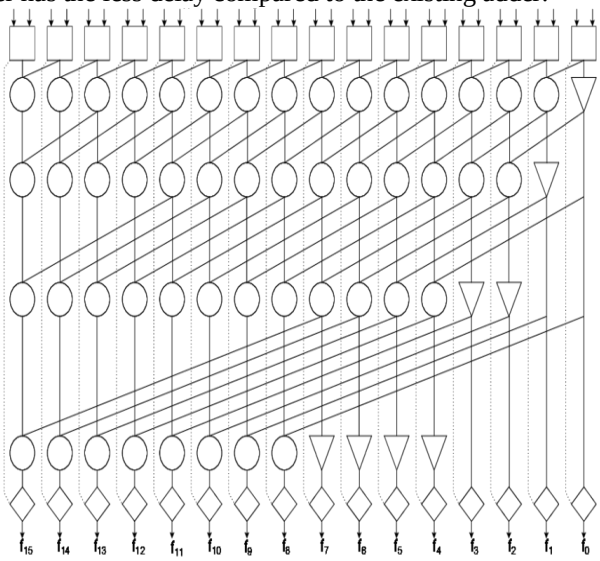


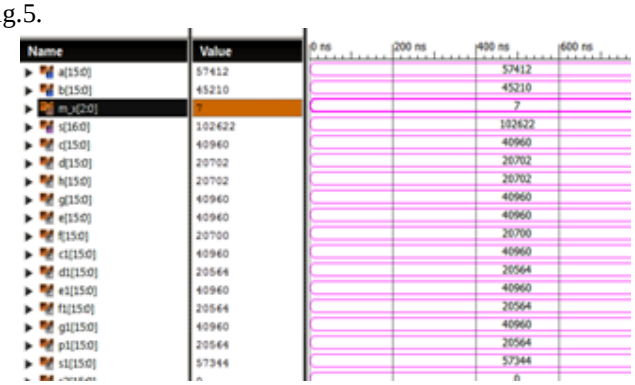
Fig.4: Block diagram of proposed adder

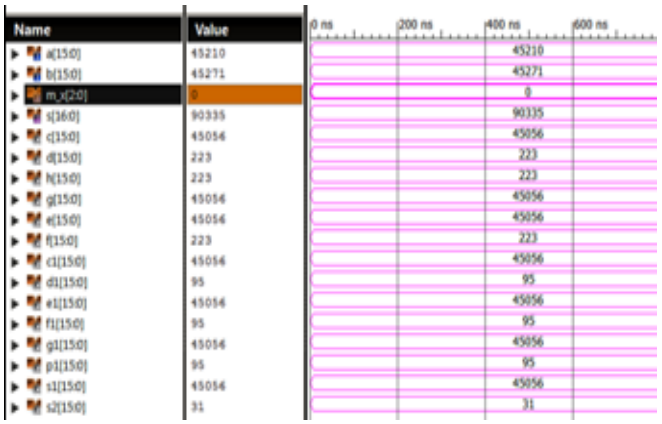
Koggy stone adder consists of square box which has the half adder to generate propagate and generate signals we are using carry maskable half adder which has a maskablesignal.when we apply masking we get approximate result when we remove masking we get the accurate result.we have blackdot which is carry generator it calculates the carry in a parallel way to reduce the delay.we use buffer to reduce the loading effect.at last this is post computation stage we use diamond to calculate the sum.

IV. RESULTS AND PERFORMANCE ANALYSIS

We have verified the proposed design and existing designs by writing the VHDL code, simulated and synthesized.

The simulation result of the koggy stone adder is shown in Fig.5.

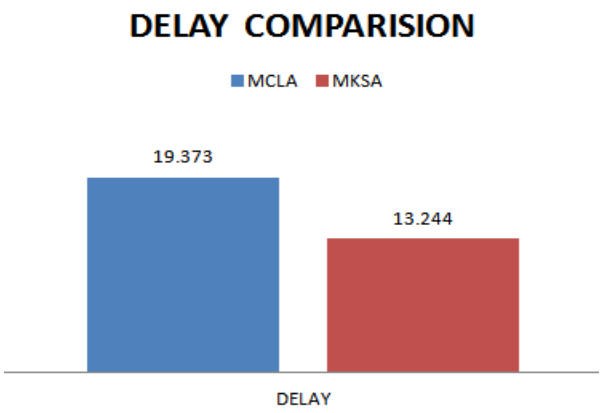


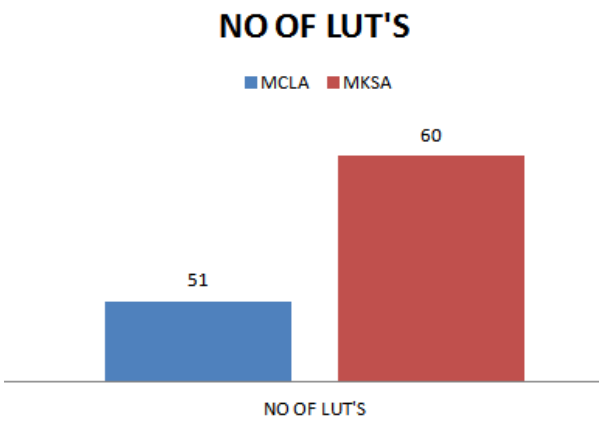


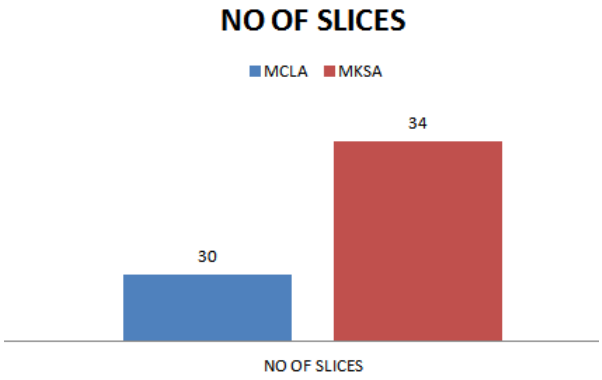
Device utilization of proposed approximate adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	34	8672	0%
Number of 4 input LUTs	60	17344	0%
Number of bonded IOBs	52	190	27%

Comparision results of delay for both existing approximte adder and proposed approximate adder koggy stone adder is shown in the below graph proposed koggy stone adder achives high speed when compared to existing approch.







V. CONCLUSION

In this paper,we propose a koggy stone adder which is of parallel prefix adder using maskable signal to achieve a high speed adder.it is a accuracy configurable adder which has the both approximate and accurate result by msking the bits we get approximate result.when we remove the maskable signal we get accurate result.compared to existing adders experimental results demostrate that proposed adder is a high speed adder which has less delay without sacrificing the accuracy.

VI. REFERENCES

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