HIGH PERFORMANCE SRAM CIRCUIT BASED ON TRANSMISSION GATE USING FinFET AND ADIABATIC LOGIC

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Abstract: In this paper, a high speed, low power dissipation, low average power consumption and low PDP (Power Delay Product) based SRAM cell is proposed. SRAM cell play an important role in storage devices and hence it is necessary to produce a better design for the optimal use in the portable devices. The MOSFET based conventional 6 T SRAM has high power and delay product with high short channel effects in 32nm technology. Hence, a solution is provided by the use of adiabatic logic and transmission gate logic. In this technique, use a transistor between Vdd and Virtual Vdd to improve the characteristics, it shows that Average power is decreased by 94.75%, delay is improved by 87.15%, power dissipation is improved by 88.78% and energy is decreased by 99.19% in adiabatic proposed circuit when compared to adiabatic FinFET based circuit and similarly the improvements in transmission gate based proposed circuit from simple transmission gate FinFET SRAM is improved by 55.24%, 50.28%, 68.63% and 75% on basis of Average Power, Delay, Power Dissipation and Energy. The proposed circuits is of 8 Transistors.

Keywords: - FinFET, 32nm Technology, SRAM, Low Power

I. INTRODUCTION

Memory cells assume a critical job regarding force, speed and execution in computerized circuits, for example, the System-on-Chips (So Cs), microchips and microcontrollers. These memory clusters possess impressive piece of the chip region. Consequently, these memories. Cells as a general rule contribute for a higher division of the chip control. A few literary works have exhibited different designs for the SRAM cell, with their principle centre around decrease of the cell territory, diminished gadget include and decrease in the spillage control. The preference to optimize the layout metrics of overall performance, strength, area, fee, and time to market (opportunity cost) has now not changed for the reason that progress of the IC enterprise. Advantage of FinFET contrasted with planar is way higher execution at a proportionate power spending plan, or equivalent execution at a far lower power spending plan. This basically gives originators the power to extricate the best execution for very shoddy power, a urgent improvement for powered gadgets. One element that creates the progress from thinking of with planar FETs to concocting with FinFET somewhat less confused is that the demonstrated actuality that the back-end of the strategy is essentially a proportional, piece of the arranging stream identified with the physical execution stays flawless.

II. IMPLEMENTATION

In this section, we propose the circuits for adiabatic and transmission gate logic based 9T SRAM cells. The circuit consists of one p type FinFET at VDD part of the base circuit. The circuit is controlled by the signal given in this circuit. The circuit is simulated in HSPICE Synopsys and the technology used 32nm.

Proposed Adiabatic based FINFET Circuit:

In the figure 1, the adiabatic logic is created by the use of MCPL logic, and also at Vdd an extra control transistor is added which decides when the circuit is on or off. The makes it in sleep or active mode.

Proposed Transmission Logic based FINFET Circuit:

In the figure 2, the transmission gate logic is created by the use of two transistors at WBL and ABL bar, and also at Vdd an extra control transistor is added which decides when the circuit is on or off. The makes it in sleep or active mode.

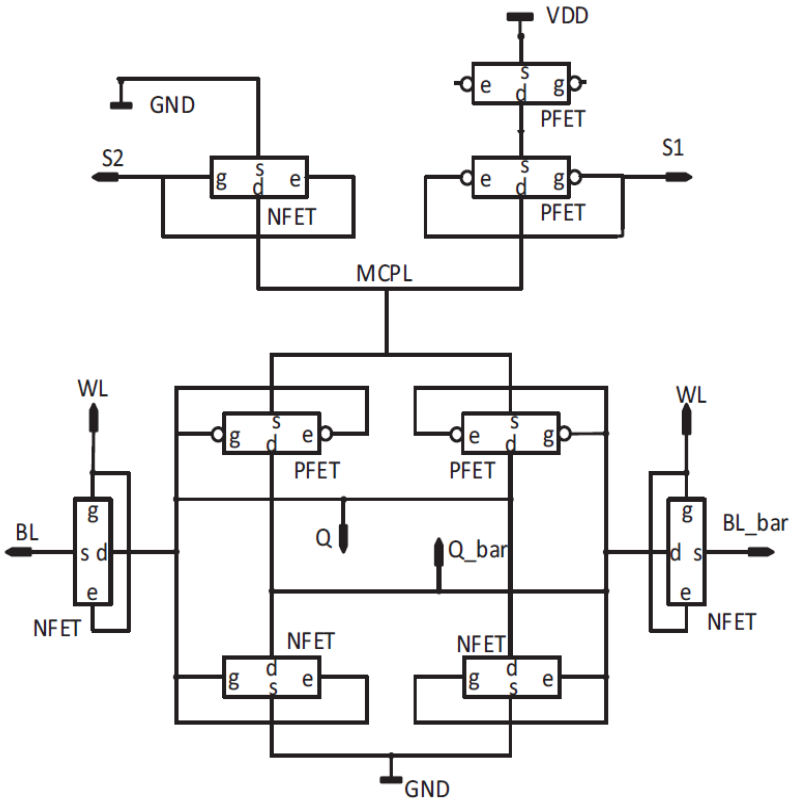

Figure 1: Proposed Adiabatic based SRAM cell FinFET

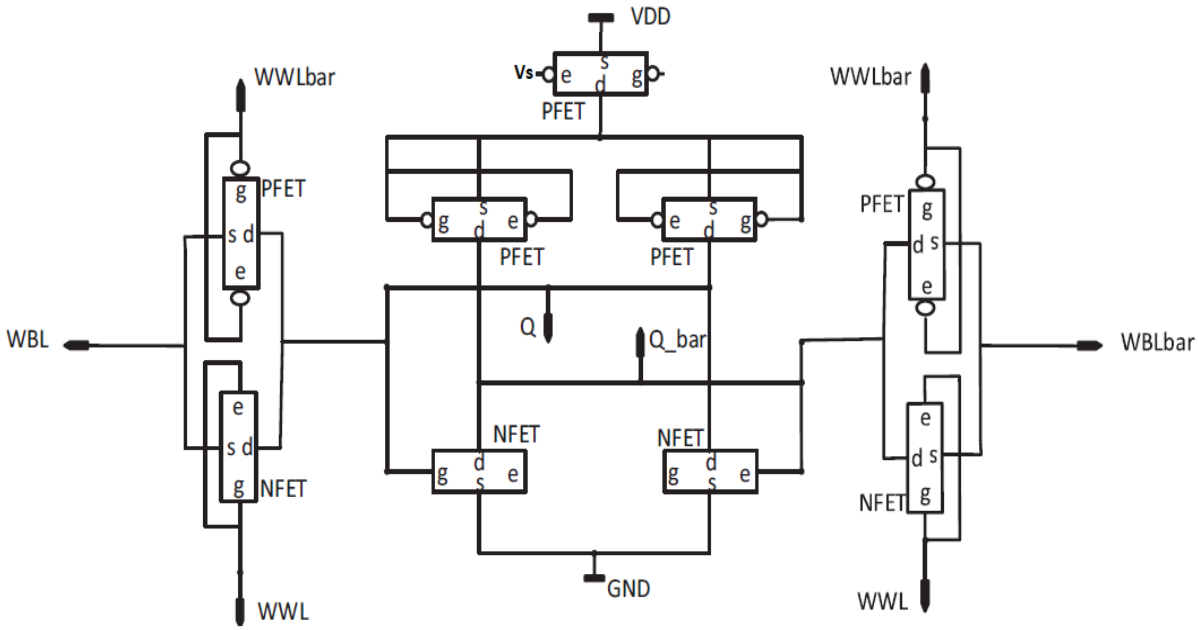

Figure 2: Transmission Gate Logic Proposed Circuit for SRAM

III. RESULTS

The results of the performance parameters are shown in fable 1 which clearly shows the enhancements in proposed circuits.

Table 1: Simulation Results

	sram adiabatic mos	**sram adiabatic mos proposed**	**sram adiabatic fin**	**sram adiabatic fin proposed**
Average Power	1.25E-07	1.04E-07	4.63E-09	2.43E-10
Delay	1.41E-07	1.41E-07	7.27E-11	9.34E-12
Power Dissipation	1.79E-07	1.06E-07	1.23E-11	1.38E-12
Energy	1.75E-14	1.46E-14	3.37E-19	2.27E-21
	sram TGL mos	sram TGL mos proposed	sram TGL fin	sram TGL fin proposed
Average Power	3.07E-08	7.08E-09	5.23E-12	2.55E-12
Delay	5.17E-11	3.33E-12	5.10E-11	2.60E-11
Power Dissipation	9.87E-08	8.57E-08	5.26E-12	1.65E-12
Energy	1.59E-18	2.36E-20	2.66E-22	6.65E-23

In figure 3 and Figure 4 shows the Average Power in Various circuits for adiabatic and transmission logic gate based. The proposed circuits shows better performance in Average Power Consumption.3

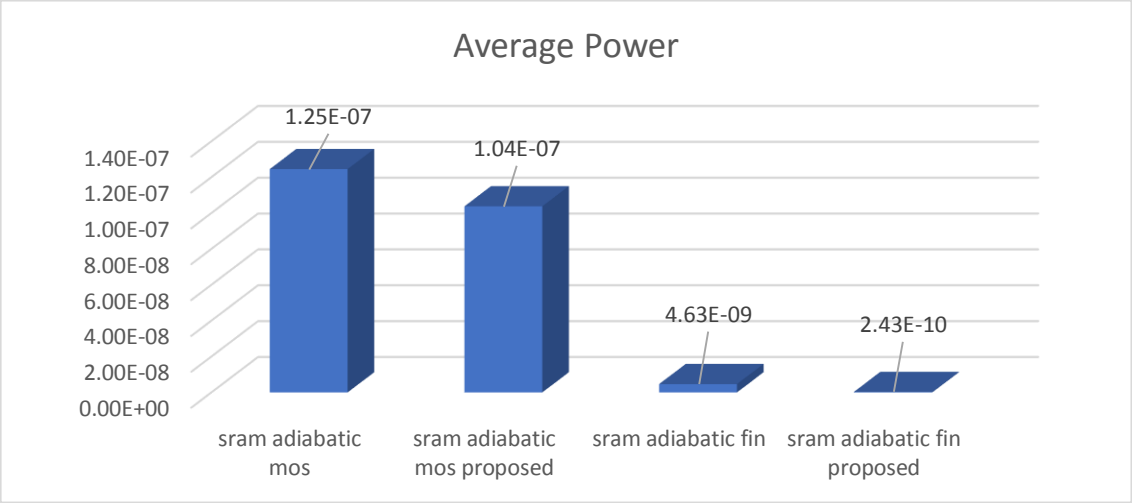

Figure 3: Average Power Consumption in Adiabatic SRAMs

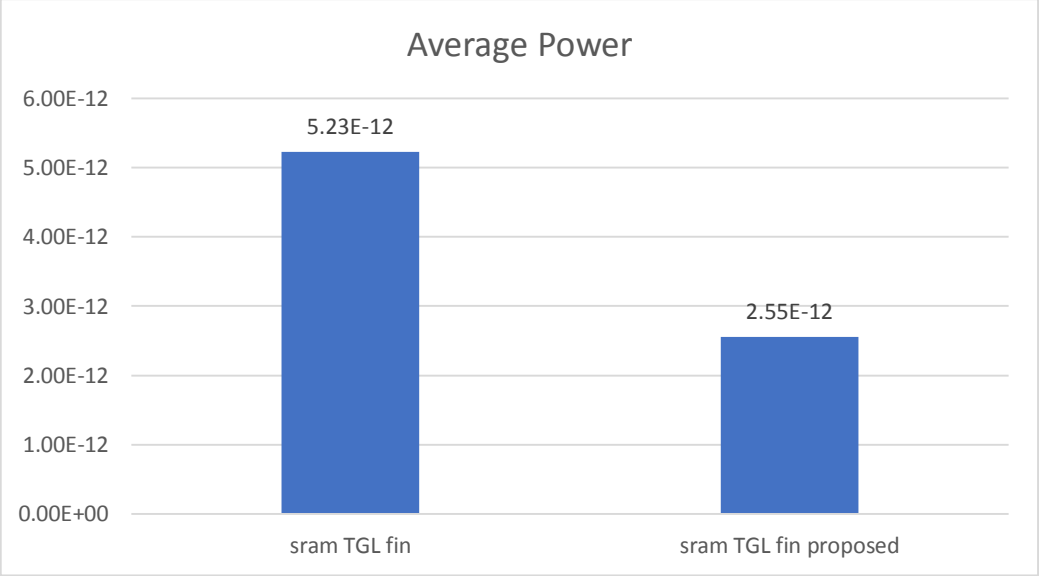

Figure 4: Average Power Consumption in TGL SRAMs

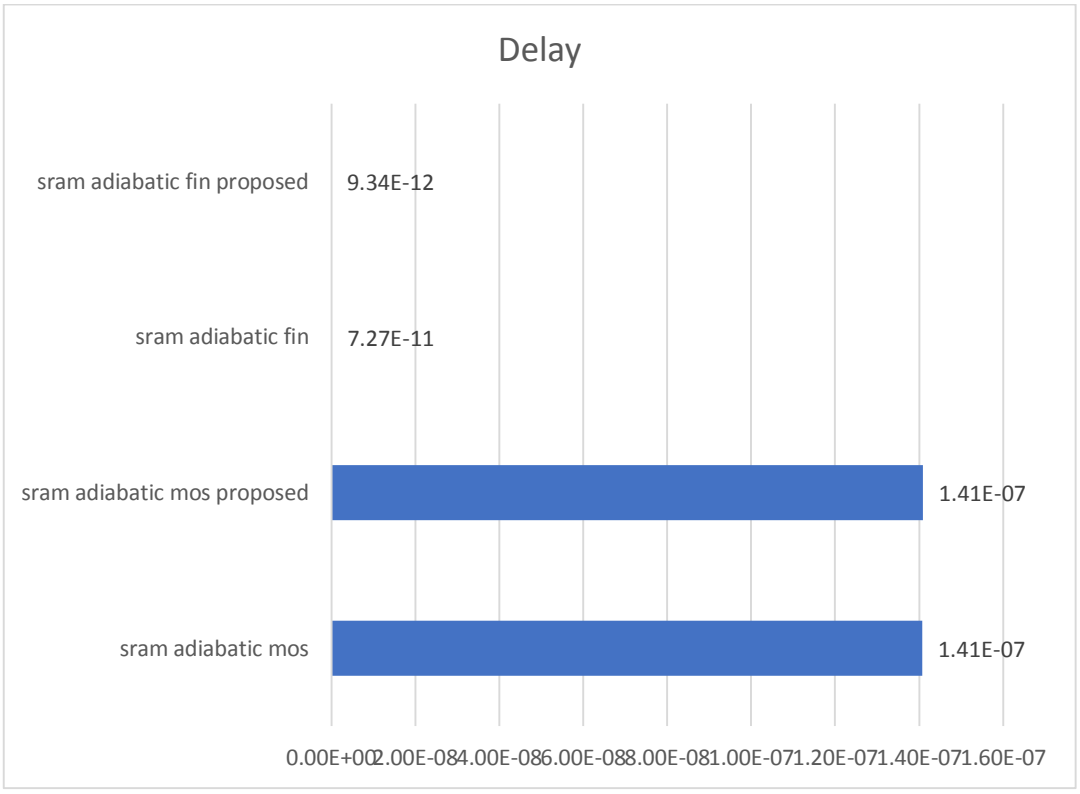

Figure 5: Delay in Adiabatic based Circuits

Figure 4.4 and Figure 4.5 shows the delay enhancements and Power dissipations enhancements in Adiabatic logic-based circuits respectively.

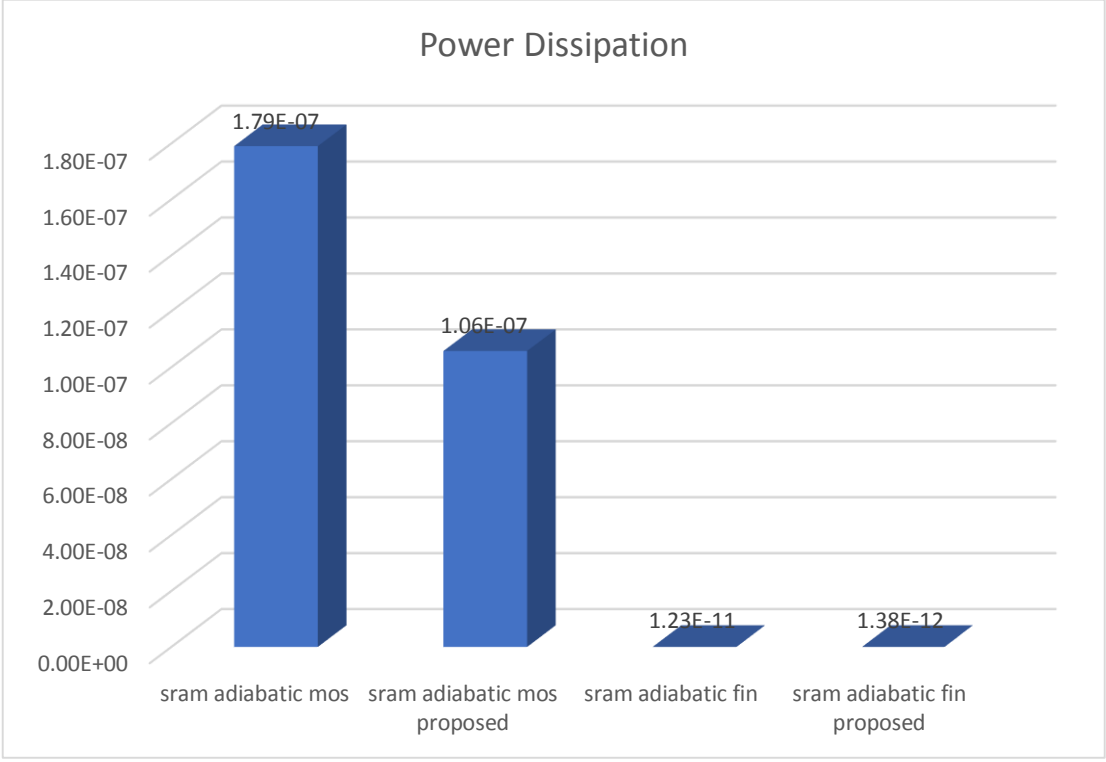

Figure 6: Power Dissipation in Adiabatic based Circuits

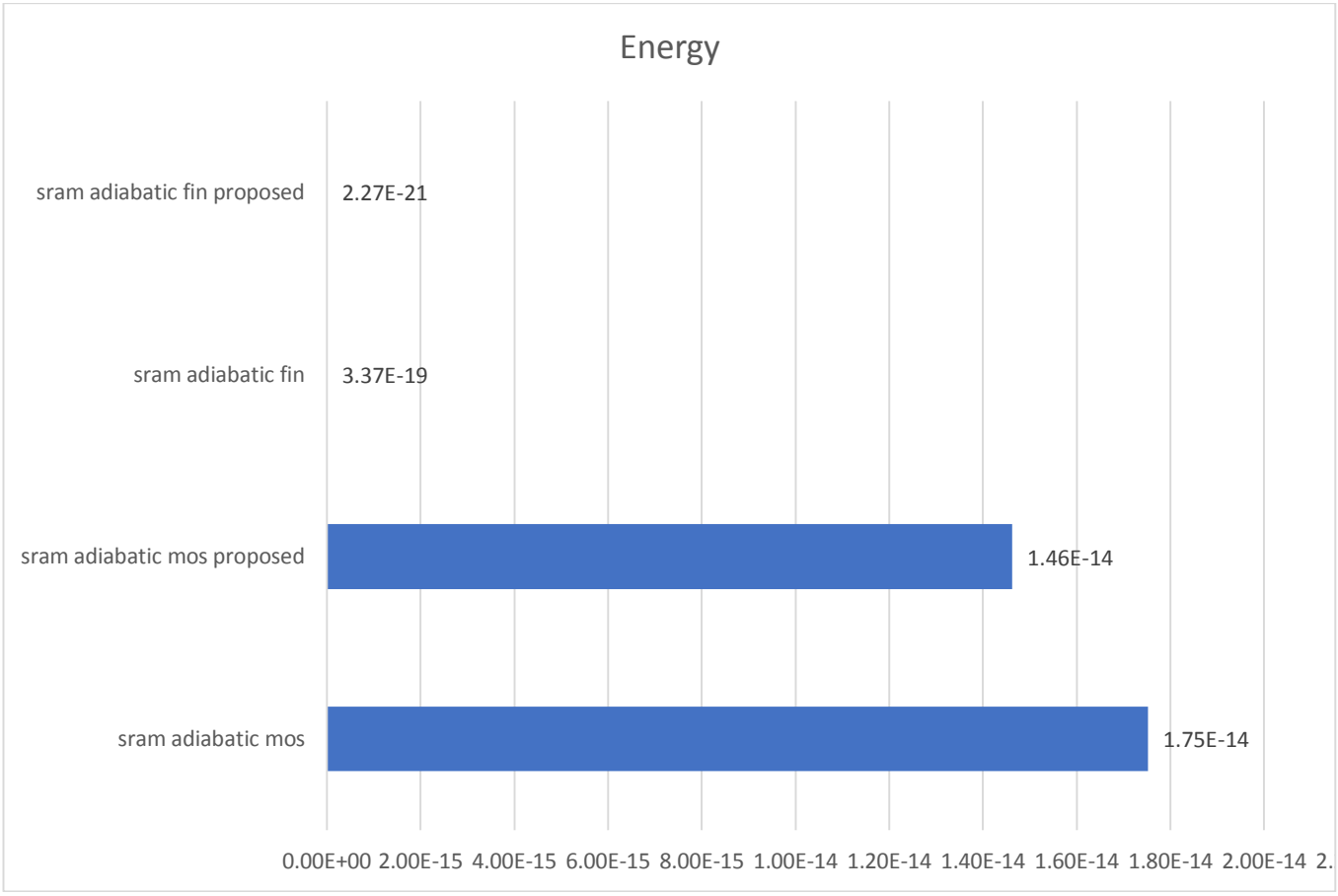

Figure 7: Energy in Adiabatic based Circuits

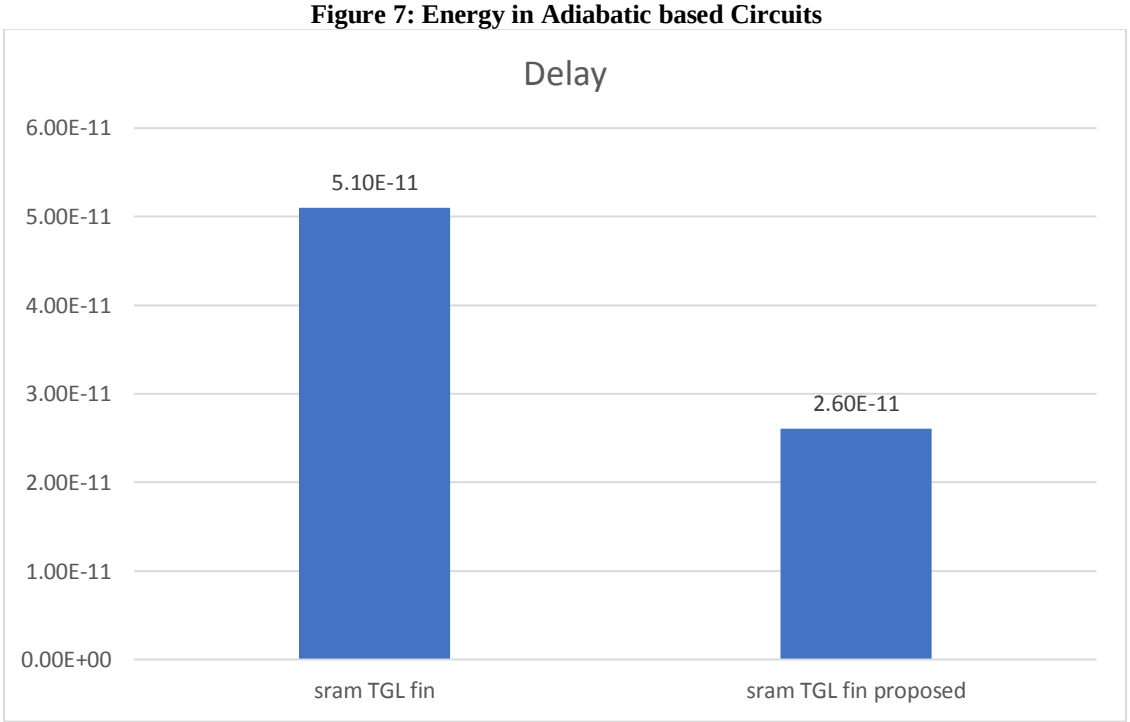

Figure 8: Delay in TGL based Circuits

Figure 7 and Figure 8 Energy in Adiabatic and Delay in transmission gate logic circuits in SRAM FinFET are represented.

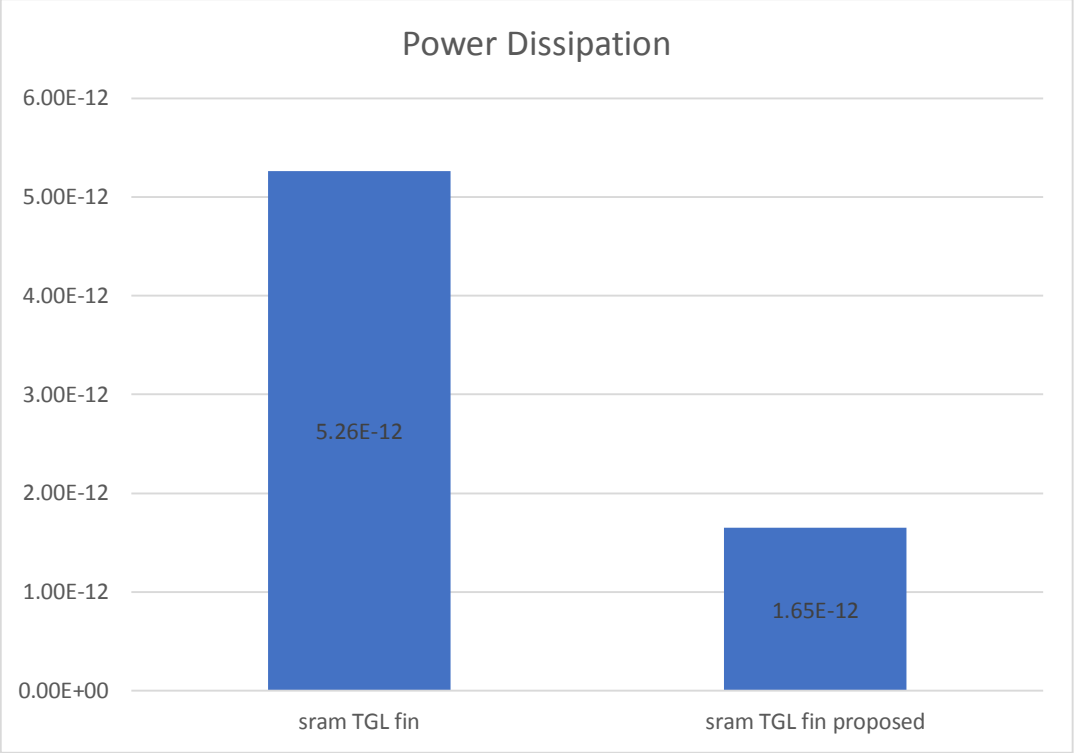

Figure 9: Power Dissipation in TGL based Circuits

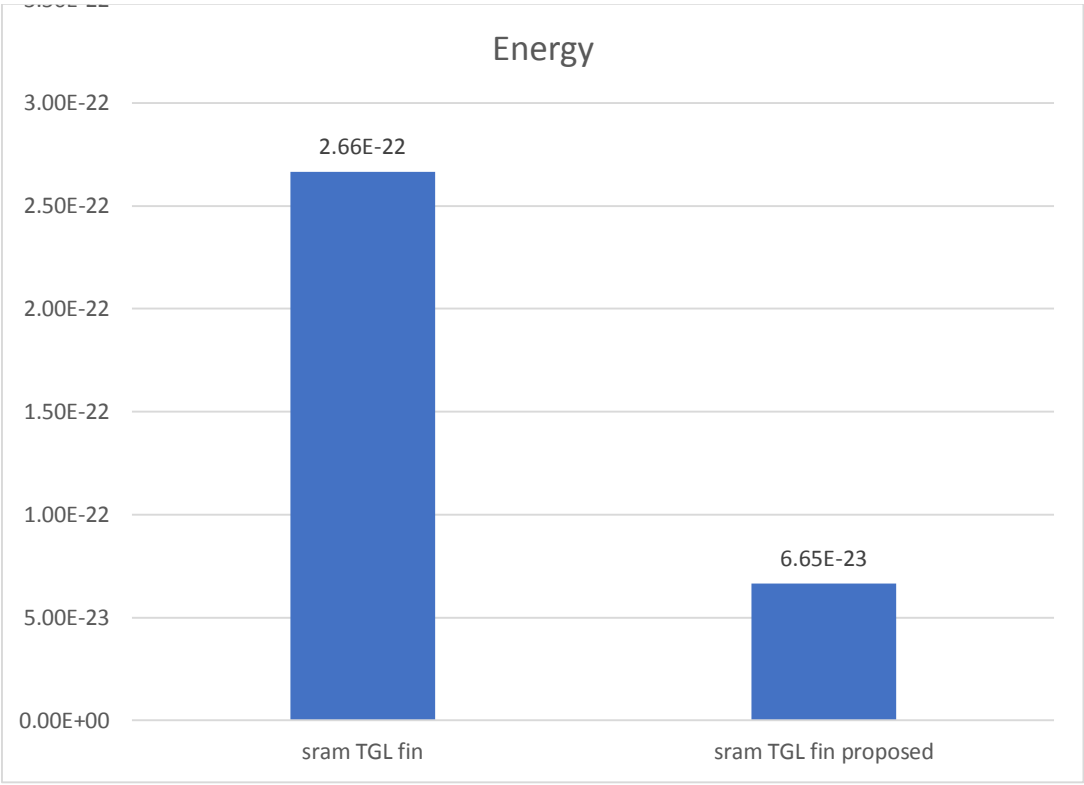

Figure 10: Energy in TGL based Circuits

Figure 9 and Figure 10 shows the Power Dissipation and Delay in TGL based circuits and shows that Proposed circuit is improved the performance.

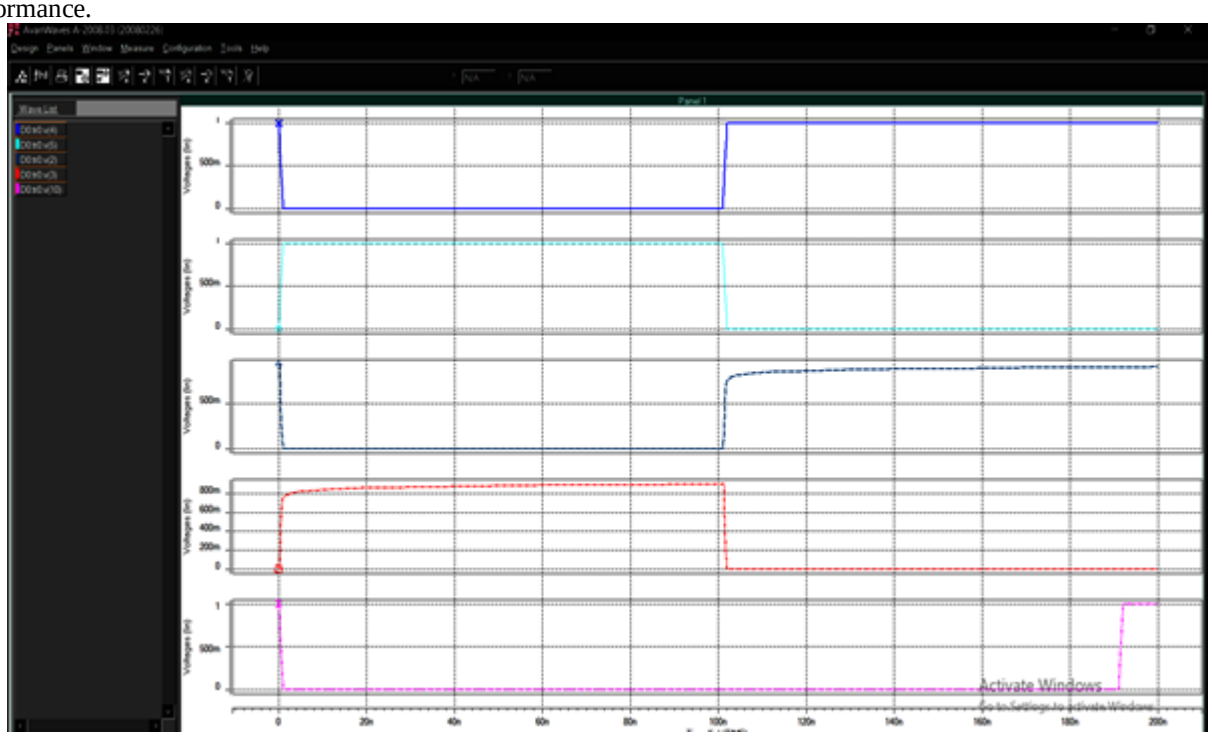

Figure 11: Waveform TGL

Figure 11 shows the waveforms for the TGL based circuits, the SRAM stores 0 and 1 efficiently.

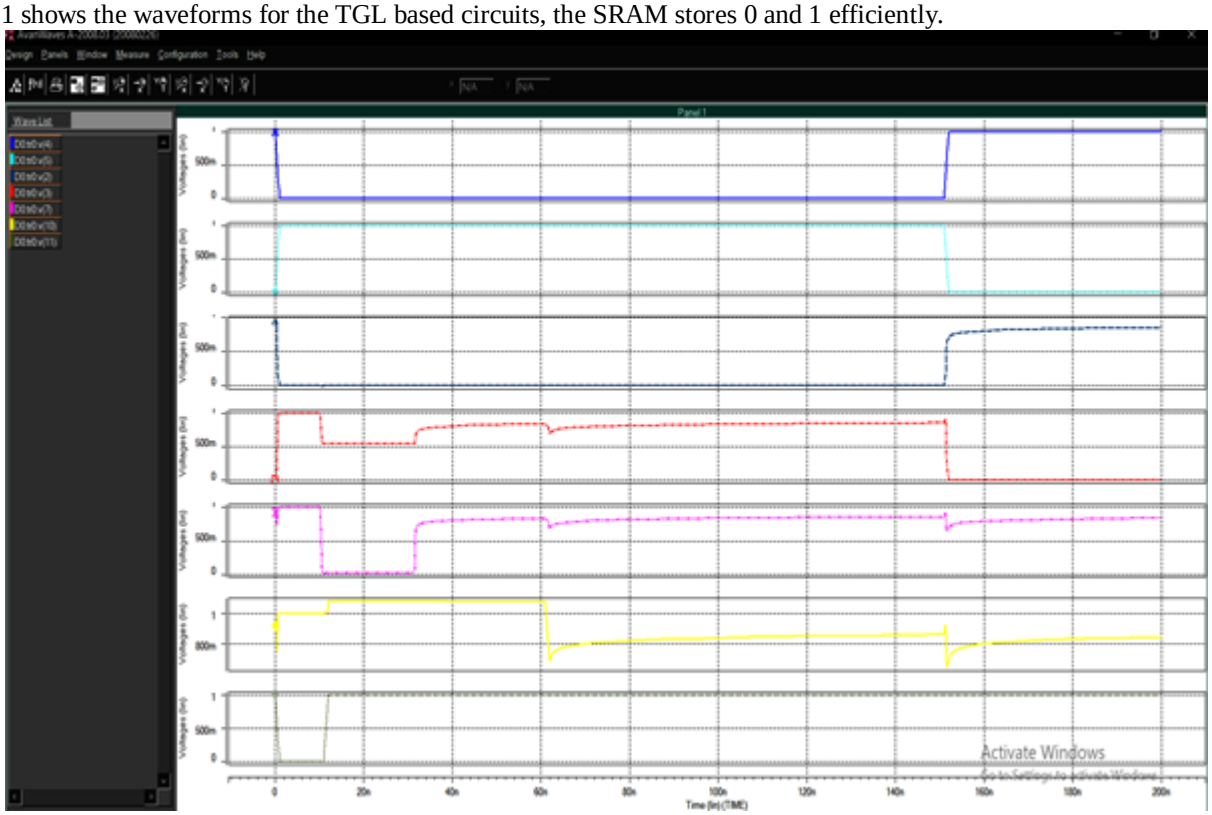

Figure 12: Waveform Adiabatic based Circuits

Figure 12 shows the waveforms for the Adiabatic based circuits, the SRAM stores 0 and 1 efficiently.

IV. CONCLUSION

Hence, we conclude that by use of transistor between VDD and the circuit virtual Vdd will improve the characteristics and performance of the circuit. The proposed circuit consists of 9T based FinFET. The improvement in the circuit are follows:
In adiabatic SRAM proposed circuit:

- Average power is decreased by 94.75%,
- delay is improved by 87.15%,
- power dissipation is improved by 88.78% and
- energy is decreased by 99.19%

In transmission gate based proposed circuit improvements are:

- 55.24% in Average Power
- 50.28% in Delay
- 68.63% in Power Dissipation
- 75% in Energy

V. REFERENCES

[1]. Sudarshan Patil , V S Kanchana Bhaaskaran "Optimization of Power and Energy in FinFET Based SRAM Cell Using Adiabatic Logic", 978-1-5090-5913-3/17/$31.00 c 2017 IEEE
[2]. Akshay Bhaskaret al.," Design and Analysis of Low Power SRAM Cells" International Conference on Innovations in Power and Advanced Computing Technologies [i-PACT2017], 978-1-5090-5682-8 /17/$31.00 ©2017 IEEE
[3]. Saurabh et al., "Low Power 6T -SRAM" Electronics and Communication Engineering The LNM Institute of information Technology Jaipur, India, 978-1-4673-3136-4/12/$31.00 ©l012 IEEE
[4]. Mohammad Ansaria, Hassan Afzali-Kusha, Behzad Ebrahimi, Zainalabedin Navabi, Ali Afzali-Kush, Massoud Pedram: A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies INTEGRATION, the VLSI journal, 2015.
[5]. Loveneet Mishra , Sampath Kumar V , Sangeeta Mangesh, et al., "Design and implementation of low power SRAM structure using nanometer scale" International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB16), 978-1-4673-9745-2 ©2016 IEEE
[6]. Pal, P.K.; Kaushik, B.K.; Dasgupta, S.," Low-power and robust 6T SRAM cell using symmetric dual-k spacer FinFETs," 2014 29th International Conference on Microelectronics Proceedings - MIEL 2014, vol., no., pp.103,106, 12-14 May 2014
[7]. T. Vasudeva Reddy, Dr B.K. Madhavi, k. Madhava Rao et al., "Design & Analysis of Single Bit Sub-Threshold SRAM Using Dtmos with Traditional SRAM Design under 32nm Design" International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887 Volume 5 Issue XI November 2017- Available at www.ijraset.com
[8]. Majid Moghaddam et al., "Ultra Low-Power 7T SRAM Cell Design Based on CMOS "2015 23rd Iranian Conference on Electrical Engineering (ICEE), 978-1-4799-1972-7/15/$31.00 c 2015 IEEE
[9]. Shunji Nakata, Hiroki Hanazono, Hiroshi Makino, Hiroki Morimura, Masayuki Miyama, and Yoshio in Read Noise Margin of Single-Bit Line SRAM Using Adiabatic Change of Word Line Voltage, IEEE transactions on very large-scale integration (vlsi) systems, vol. 22, no. 3, march 2014
[10]. Vasudha Gupta and Mohab Anis et al.," Statistical Design of the 6T SRAM Bit Cell" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 57, NO. 1, JANUARY 2010