

A 3*3 Multiplier Design using High Speed Energy Efficient Compressor Adder

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Abstract- In digital signal processing systems multiplier is an important element. Wallace tree multipliers are considered as one of the high speed and efficient multipliers. In this paper, a multiplier is implemented using architecture for a Wallace tree multiplier. The implemented design comprises of 4:2 compressors. We have used the Tanner EDA Tool with version 14.1 in 180nm technology. The 4-2 compressor adder is simulated for supply voltage ranging from 1v-3v and various parameters are calculated, such as, power, delay and power delay product (PDP). The multiplier circuit is simulated at 180nm technology at 1.8v.

Index Terms- Multiplier, Multiplexer, Compressor Adder, Tanner tool.

I. INTRODUCTION

The prominence and request of high speed electronic systems are ceaselessly expanding step by step. Thus the improvement of a quick and productive system design has been a subject of enthusiasm of VLSI design engineers over decades. A processing component called compressor is broadly utilized as a part of high speed system. In this way the popularity and request of high speed compressors are quickly expanding in numerous parts of a digital system, particularly in digital signal processors, digital filters, microprocessors, motion estimation accelerators and so forth. VLSI designers have designed different kinds of 3-2, 4-2, 4-3, 5-2, 5-3, 6-3, 7-2, 7-3 and so forth compressors. The normal interconnection and simple structure make the 4-2 compressor appropriate for quick digital computational circuits.

Adder compressors have been utilized to implement math and digital signal processing (DSP) circuits for low power and high performance applications. Compressors are additionally utilized as a part of multiplier designs. Multipliers are structured into three capacities: partial-product generation, partial-product accumulation and final addition. The primary wellspring of power, delay and zone originated from the partial-product accumulation stage. Compressors ordinarily implement this stage since they add to the diminishment of the partial products (decreasing the quantity of adders at the final stage) and furthermore add to lessen the critical path which is imperative to keep up the circuit's performance.

In this paper a 4*4 multiplier is designed using 4-2 compressor adder. In section 2, description and design of

compressor module using 8T XNOR/XOR is presented. The section 3 describes the multiplier designed by using 4-2 compressor and discusses the results, simulation and finally the paper is concluded by the Section 4.

II. COMPRESSOR ADDER

A 4-2 compressor is a combinatory device which compresses four partial products into two partial products. The block diagram of a 4-2 compressor is shown in Fig1. It accepts five inputs in particular M1, M2, M3, M4 and Cin; and generates three outputs, viz. Sum, Carry and Cout. Design of a 4-2 compressor with two 8T XOR-XNOR modules and four MUXs based on transmission gate logic is described. To implement the XOR-XNOR module a total of eight transistors are used.

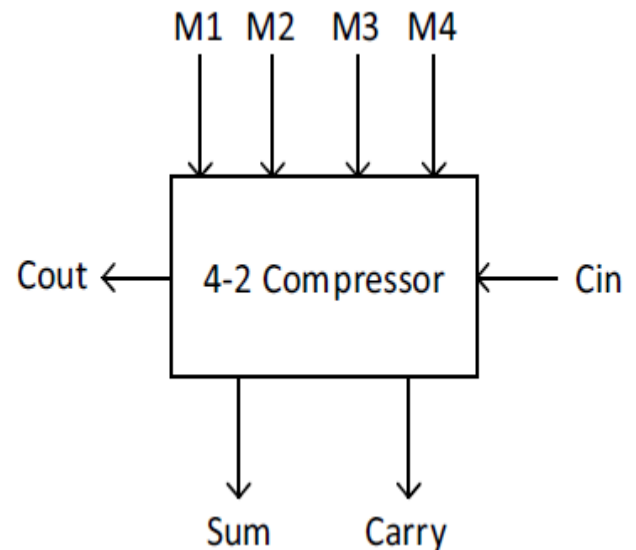


Fig.1: Block diagram of 4-2 compressor

In XOR- XNOR module, the inverter consisting of MP1 and MN1 transistors generates the complement of input Y. The output of this inverter controls the second inverter consisting of transistors MP2 and MN2. XNOR of X and Y is generated by the second inverter with a problem of voltage degradation for X=0, Y=1 and X=Y=1. Level restoring pass transistors MP3 and MN3 are used to avoid this problem. In this module when inputs X=Y=0, the transistors MP1 and MP2 are turned on and output (XNOR) is at logic high. When inputs X=0 and

Y=1, transistors MP2, MP3, MN1 and MN3 are turned on and a logic low is passed to the output node. Again for inputs X=1 and Y=0, transistors MP1 and MN2 are turned on and output node shows a logic low. Finally when inputs X=Y=1,

transistors MP3, MN1, MN2 and MN3 are turned on and output is at logic high level. A MUX implemented with transmission gate logic is shown in Fig2.

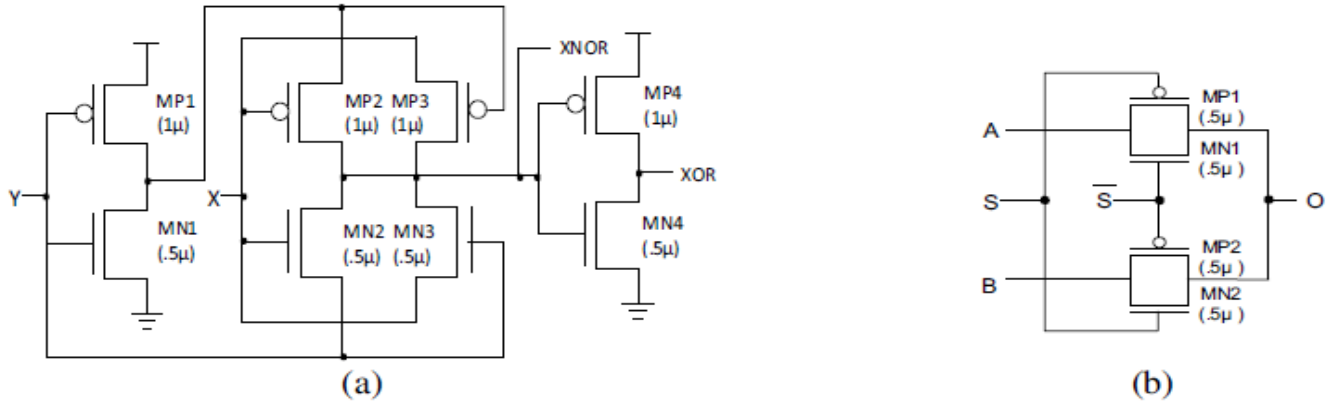


Fig.2: 8T XOR-XNOR module (b) Transmission gate MUX.

The Fig3 shows the schematic design of 4-2 compressor using XNOR/XOR gates and Mux's using Transmission Gate. The sum, carry, and Carry out is generated as shown in the fig

below. The compressor circuit consists of 36 transistors for sum,carry and cout operation.

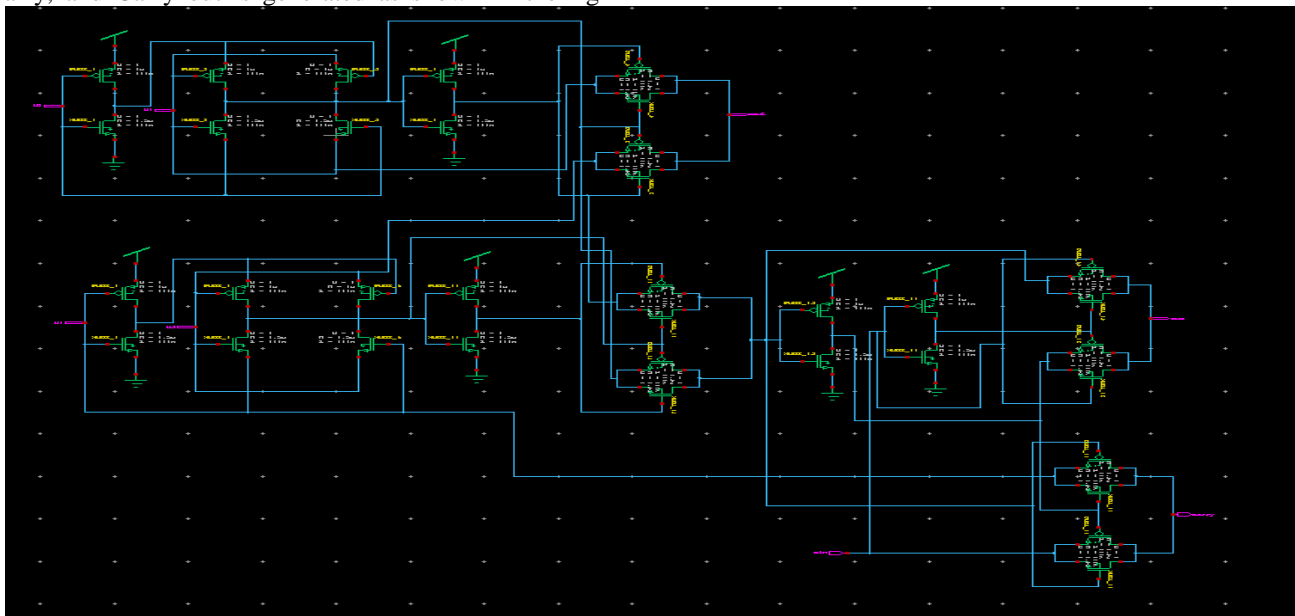


Fig.3: Schematic of 4-2 compressor adder

The waveform of the described architecture simulated at 1.8v is shown in the Fig4

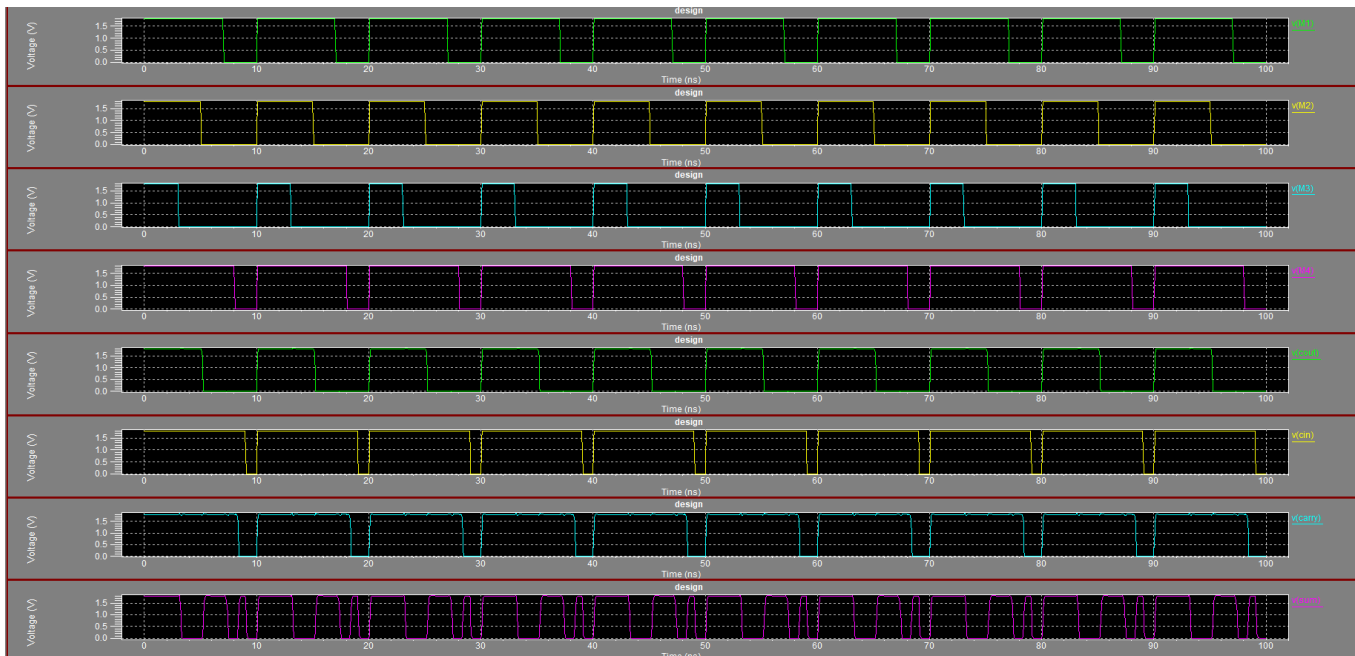


Fig.4: Waveform of 4-2 compressor adder

The table shows the 4-2 compressor parameters with supply variation ranging from 1v-3v at 180nm technology. The delay

,power, PDP, Energy, EDP are calculated and illustrated below

Table :1 Performance Comparison of compressor at various supply voltages

Parameters	1.0v	1.2v	1.4v	1.6v	1.8v	
Power (u)	12.093	18.364	25.916	34.641	44.490	
Delay_cout(n)	0.38880	0.27687	0.21625	0.17984	0.15788	
Delay_carry(n)	0.86374	0.65038	0.50044	0.40753	0.35163	
Delay_sum(n)	0.71364	0.46241	0.33738	0.26636	0.22162	
Energy (p)	1.2093	1.8364	2.5916	3.4641	4.4490	
EDP_cout (z)	0.47018	0.50846	0.56043	0.62298	0.70243	
EDP_carry (z)	1.0445	1.1944	1.2969	1.4117	1.5644	
EDP_sum (z)	0.86302	0.84919	0.87435	0.92269	0.98599	
PDP_cout (f)	4.7018	5.0846	5.6043	6.2298	7.0243	
PDP_carry (f)	10.445	11.944	12.969	14.117	15.644	
PDP_sum (f)	8.6302	8.4919	8.7435	9.2269	9.8599	
Parameters	2.0v	2.2v	2.4v	2.6v	2.8v	3.0v
Power (u)	56.759	70.220	86.275	104.42	124.18	148.61
Delay_cout(n)	0.14250	0.13330	0.12690	0.12198	0.11805	0.13757
Delay_carry(n)	0.31124	0.28186	0.26008	0.24340	0.22988	0.21977
Delay_sum(n)	0.19413	0.17322	0.16202	0.15411	0.14826	0.14482
Energy (p)	5.6759	7.0220	8.6275	10.442	12.418	14.861
EDP_cout (z)	0.80881	0.93604	1.0948	1.2737	1.4660	2.0445
EDP_carry (z)	1.7665	1.9792	2.2438	2.5415	2.8546	3.2661
EDP_sum (z)	1.1019	1.2164	1.3978	1.6091	1.8410	2.1522

PDP_cout (f)	80.881	9.3604	10.948	12.77	14.660	20.445
PDP_carry (f)	7.665	19.792	22.438	25.415	28.546	32.661
PDP_sum (f)	11.019	12.164	13.978	16.091	18.410	21.522

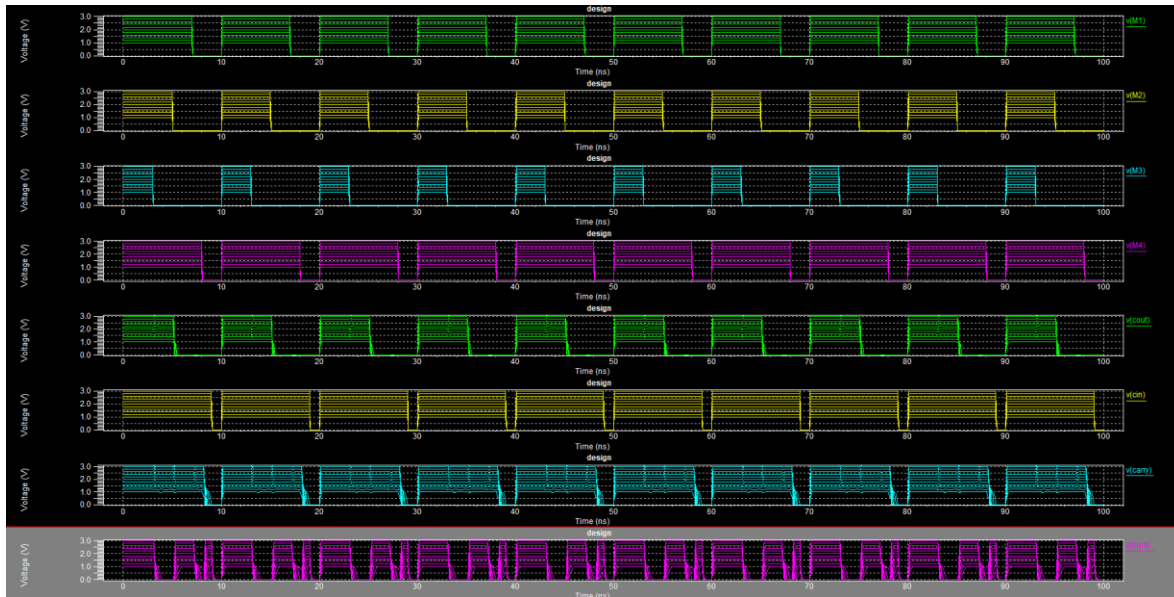


Fig.5: Simulated waveform of 4-2 compressor at various supply voltage

The Fig.5 shows the waveform of 4-2 compressor with supply variation from 1v-3v at 180nm technology

III. MULTIPLIER

A 3*3 multiplier is designed by using 4-2 compressor adder circuit as shown in Fig 6. The multiplier multiplies two 3-bit inputs and generates 6-bit output. The two 3 bit inputs are multiplied using AND gate. In Wallace tree multiplier bits are multiplied according to their weights. The weight of a wire is the radix (to base 2) of the digit that the wire carries. The multiplier module consists of AND gate, 4-2 compressor adder used as full adder. The compressor adder is used as the full adder by grounding the two bits of five bits. The first AND gate takes weight 0 i.e. a_0 and b_0 , and the first bit of the multiplication is taken from it. The second and third AND

gate takes bits of weight 1 i.e. a_0*b_1 and a_1*b_0 and this is given to the compressor as input. The compressor gives two outputs-sum and carry. The sum output of this compressor module is the second output bit of multiplication and the carry of the compressor adder is forwarded to the next compressor module in the next stage i.e. weight 2. The 6-bit output is calculated in the same way. 6th bit of the multiplication is taken from the final carry. The results are checked for 200ns with on and off time as 50ns at 1.8v and checked for 4 different combinations:

- 7*7
- 6*5
- 2*4
- 3*0

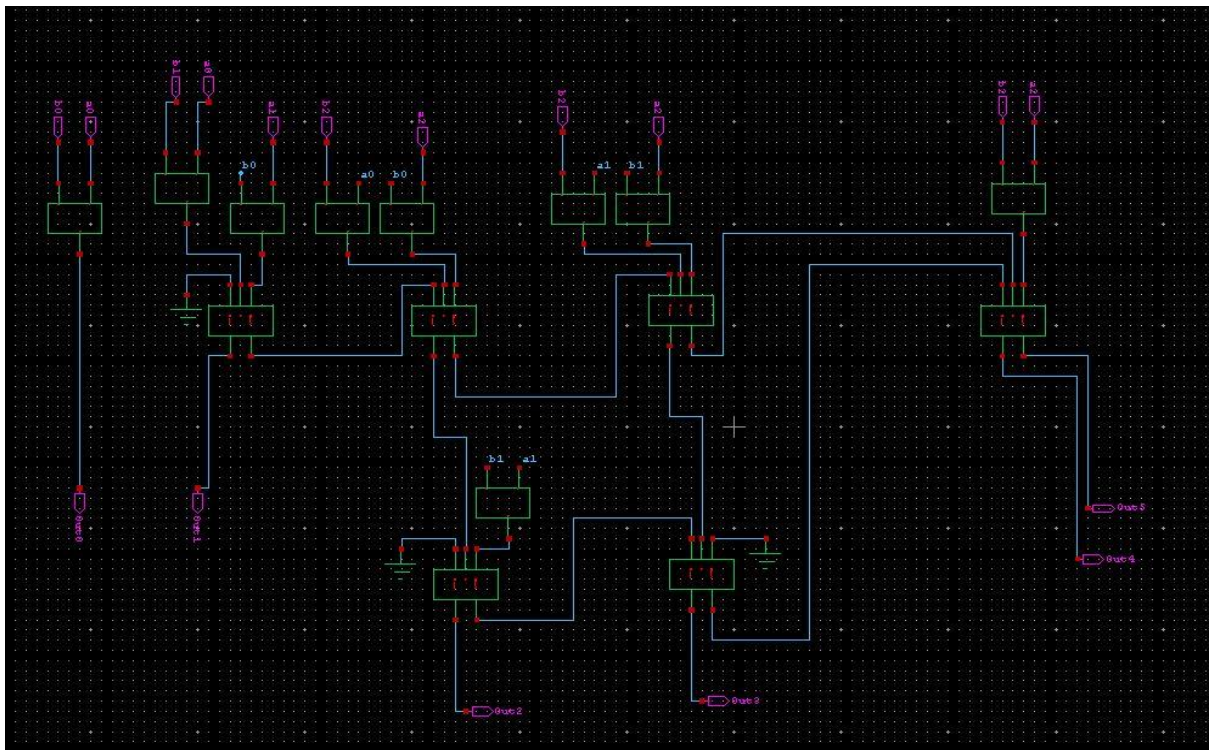


Fig.6: schematic for 3*3 multiplier using 4-2 compressor.

The Fig7 is the waveform of the multiplier for the four combinations stated above simulated at 1.8v for 200ns.

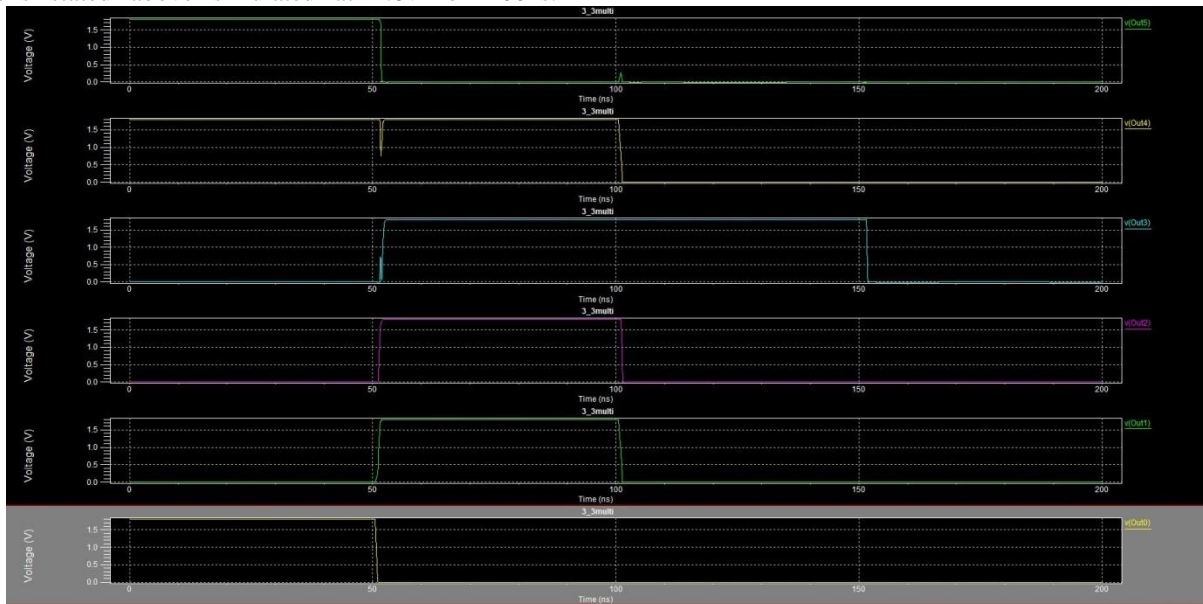


Fig.7: Waveform for 4*4 multiplier

IV. CONCLUSION

The Wallace tree multipliers can be solved & analyzed using a new modified method of Wallace tree construction using

compressors. This modified design of multiplier which consist of 4:2 compressor reduces the complexity and reduce the time

delay. Multiplier using Compressor have small increase in area and power but the time delay is less compare to conventional Wallace Tree Multiplier. As the Compressor order is increased the time delay reduces respectively. Hence for small delay requirement Wallace Tree Multiplier using compressor is suggested. The simulation is done using Tanner EDA tool with 180nm technology.

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