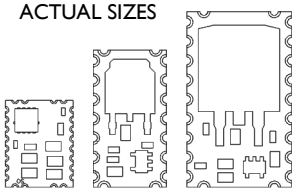
300PNC Series
CMOS Power Switch
For Ultra-High Speed Pulsed GaN Systems

ACTUAL SIZES



XSYSTOR

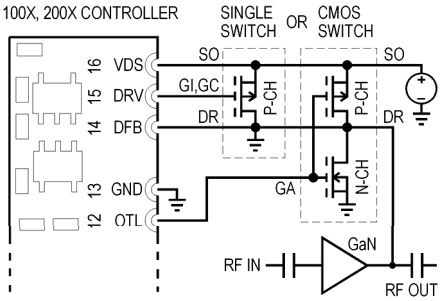
PRODUCT FLYER
July 2017

General Description

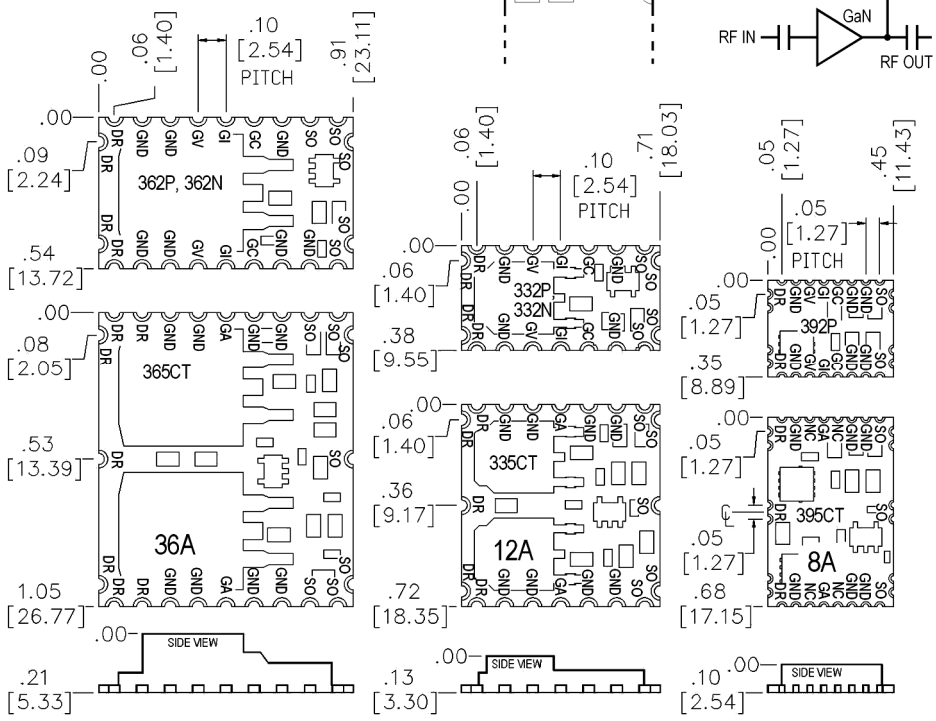
The Complementary MOSFET Switches of the 300PNC Series offers high-performance with ease of integration. Designed for Pulsed-mode, they have clocked speeds of <<200nsec for Rise and Fall Times. Its compact footprint allows direct placement near the RF Choke of the GaN drain. The MOSFETs on board are rated up to 36A Peak, and are safe from 3X the momentary current surges. With modular design introducing higher thermal resistance, the average current ceiling should be specified at half the rating. These switches are ideally driven by the 100 or 200 Series Controllers.

Features

- Rated for 100V
- Ultra-low Rds ON
- Operation up to 125°C, with derated voltage and current.
- Total switching times of <500 nsec when used together with 100 or 200 Series Controllers.
- Complementary P & N-channel MOS achieve Rise & Fall Times of <<200ns.
- Identical I/O Ports at opposite sides.
- RoHS* Compliant



Typical Connection Diagram



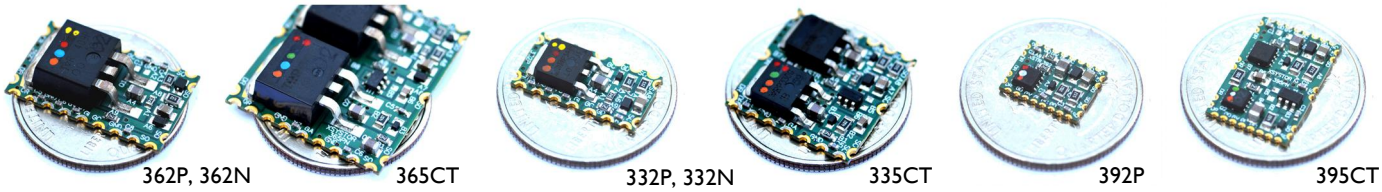
Specification Snapshot

Parameter	Min	Max
Source Voltage (SO)	+20 V	+65 V
Drain Voltage (DR)	+20 V	+65 V
Gate Voltage (GI) Open Drain	0 V	+20 V
Gate Voltage (GA) TTL High	+2.0 V	+5.0 V
Gate Voltage (GA) TTL Low	0 V	+0.8 V
Rds ON (12A Peak Switch)		0.22 Ω
Rds ON (36A Peak Switch)		0.07 Ω
Turn-ON Prop Delay (T_Delay 2)		100 ns
Turn-ON Rise Time (T_Rise 1)		70 ns
Turn-OFF Prop Delay (T_Delay 6) Complementary Pair Only		150 ns
Turn-OFF Fall Time (T_Fall 3)		100 ns
Period for Pulsed Signals		5 ms
Duty Cycle for Pulsed Signals		20 %
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of Drive Signal from Controller to 10% of Drain Voltage Output with load of 1KΩ. Faster speeds occur with decreased load resistance. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Ordering Information

332P0000	12A PEAK, 6A AVG MAX, PULSED
332N0000	COMPLEMENTS 332P ONLY
335CT000	12A PEAK, 6A AVG MAX, PULSED
362P0000	36A PEAK, 16A AVG MAX, PULSED
362N0000	COMPLEMENTS 362P ONLY
365CT000	36A PEAK, 16A AVG MAX, PULSED
392P0000	8A PEAK, 4A AVG MAX, PULSED
395CT000	8A PEAK, 4A AVG MAX, PULSED SWITCH POWER CMOS, TTL DRIVE



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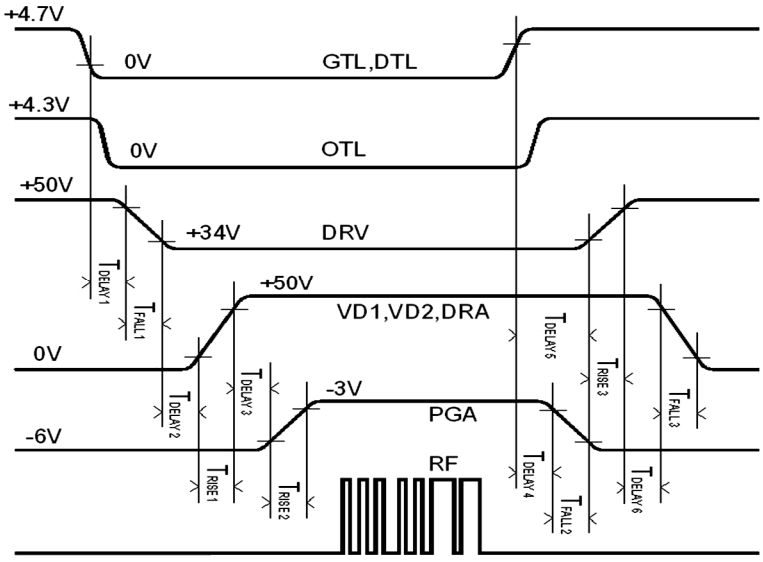
Switch I/O Pin Descriptions

GA is a gate input that receive TTL signals only from OTL output of Controller. Extra caution should be taken when handling TTL signals to prevent damage.
GI is a gate input connected to DRV of Controller. These ports are interconnected for P & N-Chan Pairs. For a Single Switch module GI is tied to GC.
GC is interconnected to like ports for P & N-Chan Pairs. It is only tied to GI for a Single Switch configuration.
GV is interconnected to like ports for P & N-Chan Pairs. Otherwise, leave port open for a Single Switch configuration.
DR are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
SO are source inputs that take up to +65V supply. Larger storage capacitance are attached here.
NC is no connection.

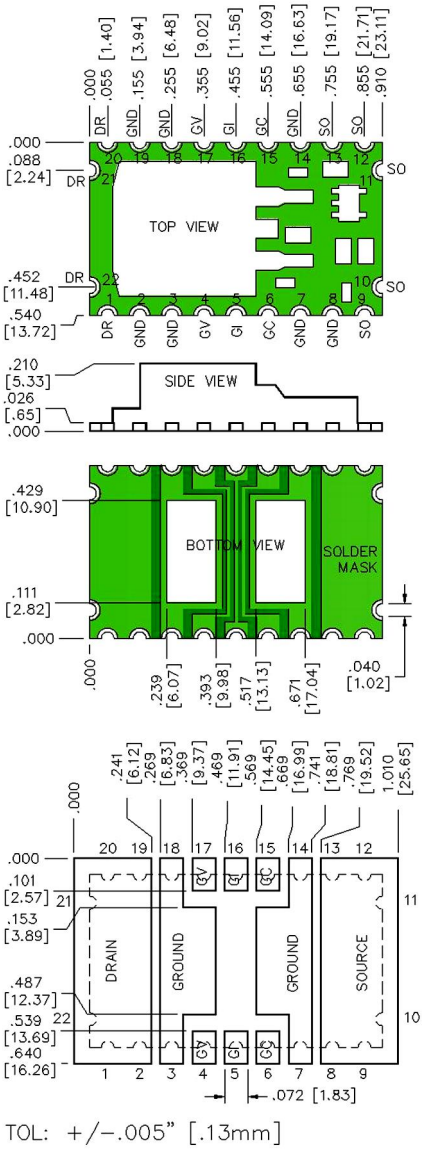
Typical Timing Diagrams



Refer to Application Note XAN-2 for further details.

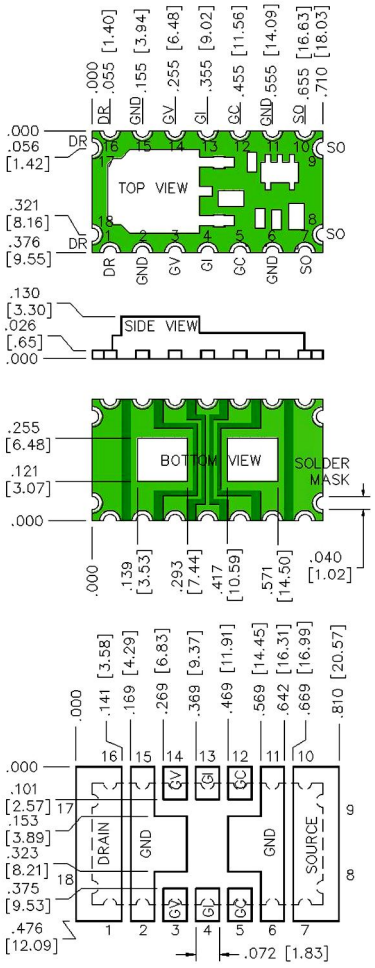
Outline & Land Pattern

362P, 362N



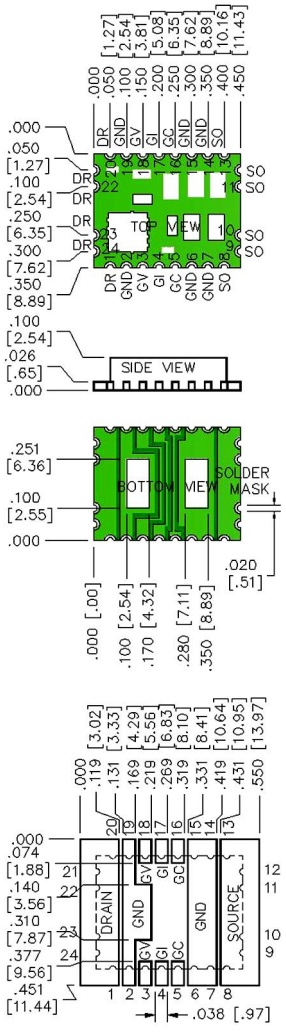
TOL: +/−.005" [.13mm]

332P, 332N



TOL: +/−.005" [.13mm]

392P



TOL: +/−.005" [.13mm]

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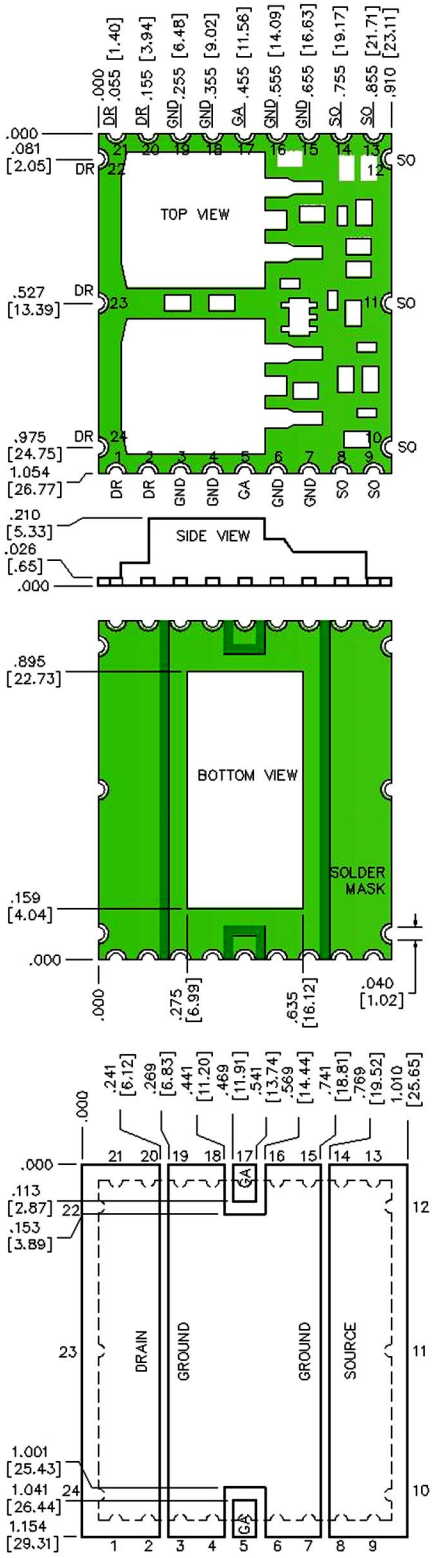
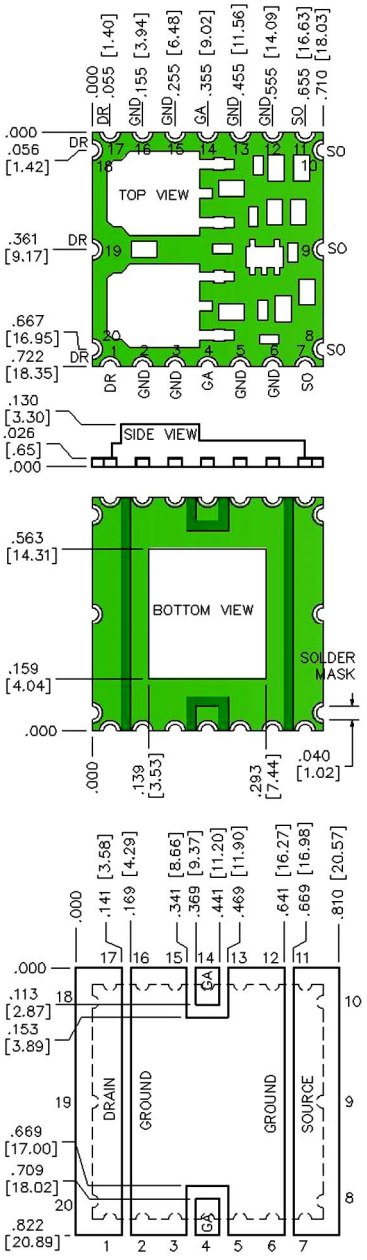
Outline & Land Pattern (continued)

365C



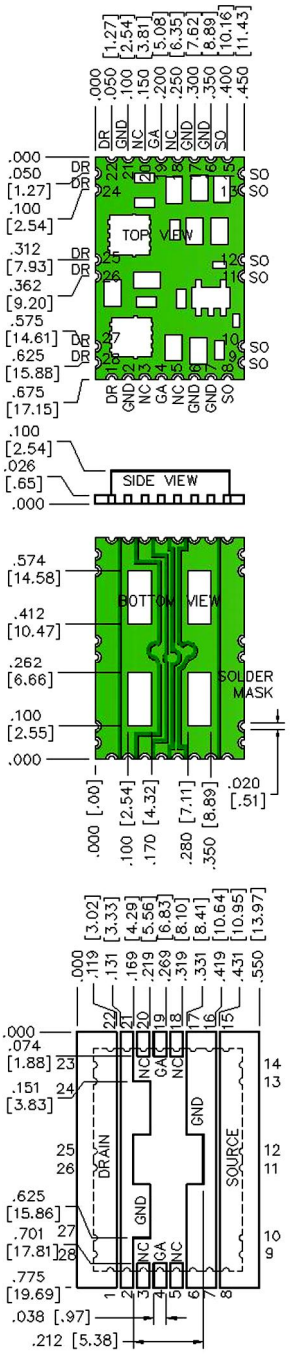
TOL: +/−.005" [.13mm]

335C



TOL: +/−.005" [.13mm]

395C



TOL: +/−.005" [.13mm]

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

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