MODIFIED ROUNDING BASED ACCURATE MULTIPLIER

A.DIVYA[1], I.V.PRAKASH[2]
[1]P.G Student, Department of Electronics and Communication Engineering
2 Professor, Department of Electronics and Communication Engineering, Siddhartha Institute Of Engineering And Technology.
(E-mail: divyaandhenani@gmail.com)

Abstract— In this paper we propose a Modified rounding based accurate multiplier (MROBA) which is more accurate than the conventional multiplier (ROBA). The main concept of multiplier depends on rounding of numbers. This multiplier can be applied for both signed and unsigned numbers. Three hardware implementations are proposed in which one implementation for unsigned and two for signed operations. The accuracy of the multiplier is compared with the conventional rounding based accurate multiplier (which are in 2n) where the modified rounding based accurate multiplier gives an exact output for the given inputs (irrespective of 2n) and various parameters like area, power delay, error significance, pass rates are been calculated and compared with conventional multiplier where, MROBA gives better results and with the MROBA MAC unit is implemented.
Keywords— Accurate multiplier; accuracy; MAC unit

I. INTRODUCTION

The crucial part of the arithmetic units are basically built by the multiplier hardware, so multipliers play a prominent role in any design. [1] If we consider a Digital signal processing (DSP) the internal blocks of arithmetic logic designs, where multiplier plays a major role among other operations in the DSP systems [1].So, in the design of multiplier and accumulate unit (MAC) multipliers play an important role. Next, important design in the MAC unit is the Adder. Adders also share the equal important in this design. By the appropriate function methods different kinds of adders and multipliers designs are been suggested. By the accurate computing the designer can make tradeoffs, accuracy, speed, energy and power consumption. In this paper we proposed the modified form of rounding based accurate multiplier which is low power design, high speed and energy efficient.

The multiplier designed was built using the conventional multiplier approach at the algorithm level by considering the rounded input values which are not in the form of 2n so, we call this multiplier the modified rounding based accurate multiplier. This multiplier can be applied for Signed and Unsigned operations by which three different architectures are implemented. The collection of this paper can be further classified has:

a) Describing the conventional rounding based approximte multiplier (ROBA) and its inaccuracy.
b) Proposed modified rounding based accurate multiplier (MROBA) and its hardware implementation.
c) With the MROBA MAC unit is designed

II. LITERATURE SURVEY

The design of accurate multipliers which were applied in image processing has many applications and they lead to less delay and power compared with the logarithm. Appropriate accuracy-configurable multiplier architecture [2] was proposed for many applications. DRUM6[3] which is having the segment size has 6 helps in the comparison of relative error and pass rates where rounding based accurate multiplier has the best results compared with it. The accuracy of the multipler is compared with the DSM8 [4] where it more accurate than the multiplier and has relative error smaller than 2%. Many of the error tolerant multipliers are been proposed by two parts one for the appropriate result and the other was for the accurate results. A 32-bit signed appropriate multiplier was designed which were used in many pipelined processors [5] DRUM6 and DSM8 are some of the accurate multiplier compared with the ROBA multiplier which yields in poor results in almost in all the cases. So, the design of MROBA helps in securing better results and with this MROBA MAC unit is been designed.

III. CONVENTIONAL ROBA

The main concept of conventional rounding based accurate multiplier [1] is selecting the rounded values for both the inputs which are in form of 2n and both the inputs should be in the form of 3x2p-1 (p is considered as arbitrary positive integer value which is greater than 1) in this case of the conventional approach the final value obtained by the multiplier would be less or more than the exact result obtained. Depending on the Ar (rounded input value of A) and Br (rounded input value of B) respectively and the result obtained is inaccurate. Considering the table 1 So in this paper we design a modified rounding based multiplier which produces the exact output for the given inputs based on the selecting the appropriate rounding values Ar and Br respectively.

Table 1: Inputs and rounded values of the conventional multiplier which producing an inaccurate result

Inputs	*Rounded value Ar*	*Rounded value Br*	*Result*
A=B	Larger value	larger value	Smaller value than the exact value
A>B	Large value	Larger value	Smaller value than the exact value
A<B	Larger value	Larger value	Larger value than the exact value

IV. PROPOSED MODIFIED ROUNDING BASED ACCURATE MULTIPLIER (MROBA)

A. Algorithm for MROBA multiplier

The main concept of the proposed modified rounding based accurate multiplier is to design the multiplier so that it takes all values which are irrespective of 2^n . The detailed explanation of the multiplier is described further. Initially let us consider Ar as the rounded input input value of input A and Br as the rounded input value of input B. Now the multiplication of the A* B is written has follows:

A * B= (Ar * B) (Br * B) + (Ar * B) + (Br *A) – (Ar * Br) - [1] ------ (a)

The basic key point to be considered is the product of (Ar * B) and (Br * B) is complex and the weight of the term would result in small values when compared with the exact numbers so the product of this term can omitted and it also leads to complex hardware design approach. Hence the multiplication can be performed by the following expression as

A * B = (Ar * B) + (Br * A) – (Ar * Br) - [1]

The product terms of (Ar * B), (Br *A), (Ar * Br) can be implemented by three barrel shifters of N bit and one adder is implemented by the parallel prefix koggestone adder of N bit and one Subtractor is also needed. If the values of A or B is equal to N where (N=1, 2, 3 ….N) it has two rounded values N+1 and N. depending on the inputs of A and B the rounded values can be chosen this kind of rounding values are applicable for both A greater B (A>B) and A less than B condition (A<B). Exception that for A equal B (A=B) the rounded input of A and B would be the middle number of N+1 and N i.e. (2N+1)/2 In the conventional rounding based accurate multiplier the numbers (which represents inputs of ROBA) in the form of 3x2p-2 (where p is arbitrary positive number which is greater than one) are considered and also we have two rounded values in the form of 2p and 2p-1 both the values lead to the same effect but in this case the larger value is considered as the rounded value for both the inputs because larger values leads in smaller hardware implementation. But the accuracy of this multiplier is poor and the exact result is not obtained in this case so, we consider the modified rounding based accurate multiplier which is applicable to all N (N=1, 2, 3……N) numbers and the exact output is obtained for the given input. Fig 1.

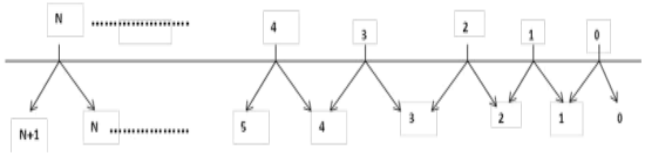

Fig 1: Top numbers represents inputs and below numbers represents the rounded values

B. Implementation of MROBA multiplier

Based on fig 2 we have the block diagram for the modified rounding based accurate multiplier. Initially we have a sign detector block where the inputs A and B are given. As in the case of the unsigned numbers the sign detector block can be applied to positive numbers. . But if the signed numbers are considered the absolute values are to be generated and then inputs are to be given. The input of A can have its rounded value has the larger value (N+1) or the smaller value (N). Similarly for input B the rounded value can either be the larger value or the smaller value.

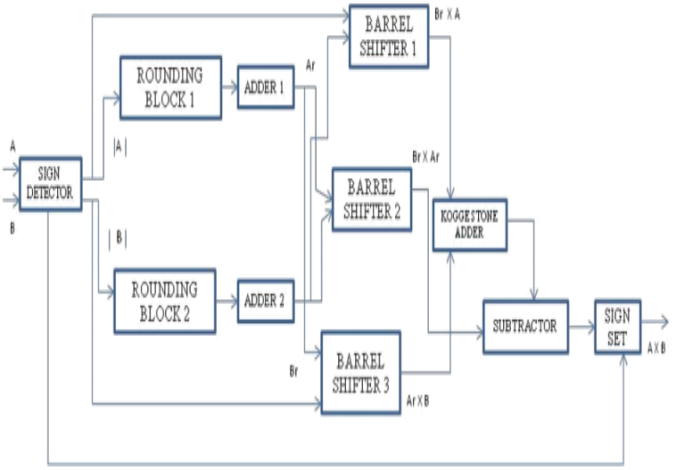

Fig 2: Block diagram of the modified rounding based accurate multiplier

This condition is applicable for both A greater than B (A >B) and for A less than B (A<B) condition. But for the A equal to B (A=B) the rounded values are considered according to (2N+1)/2. Consider table 2.

Table 2: Inputs and rounded values for all possible conditions for modified rounding based accurate multiplier

Inputs	*Rounded value Ar*	*Rounded value Br*	*Result*
A=B	Middle value	Middle value	Exact value
A>B	Larger Or smaller value	Larger or smaller value	Exact value
A<B	Larger Or smaller value	Larger or smaller value	Exact value

Next block we have a basic adder we can add +1 i.e. (N+1). Now we need three shifters to compute the product terms (Ar *B), (Br * A), (Ar * Br). The amount of shifting is basically done on no of bits we considered and the shifting operation is performed on the rounded values of Ar and Br respectively Then the output of shifter 1 and shifter 3 are given has the input to the adder basically we considered an kogge-stone adder. And the output of the adder and the output of the shifter2 is given has the input to the Subtractor block and finally we have a sign set block which is needed if we considered the signed numbers. For the unsigned it is not necessary and the final multiplication A*B is obtained the output is exact for the given input when compared with the conventional rounding based accurate multiplier it gives the exact result for the input in all the possible conditions.

SIMULATION RESULTS

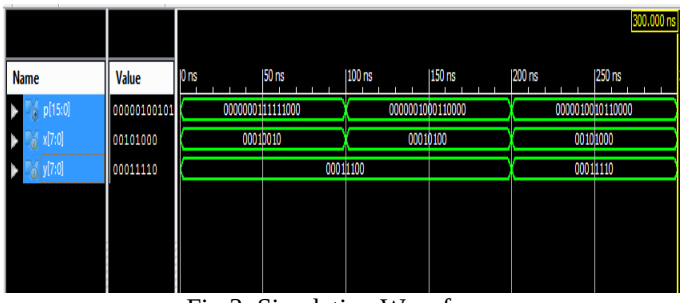

Fig 3: Simulation Waveform

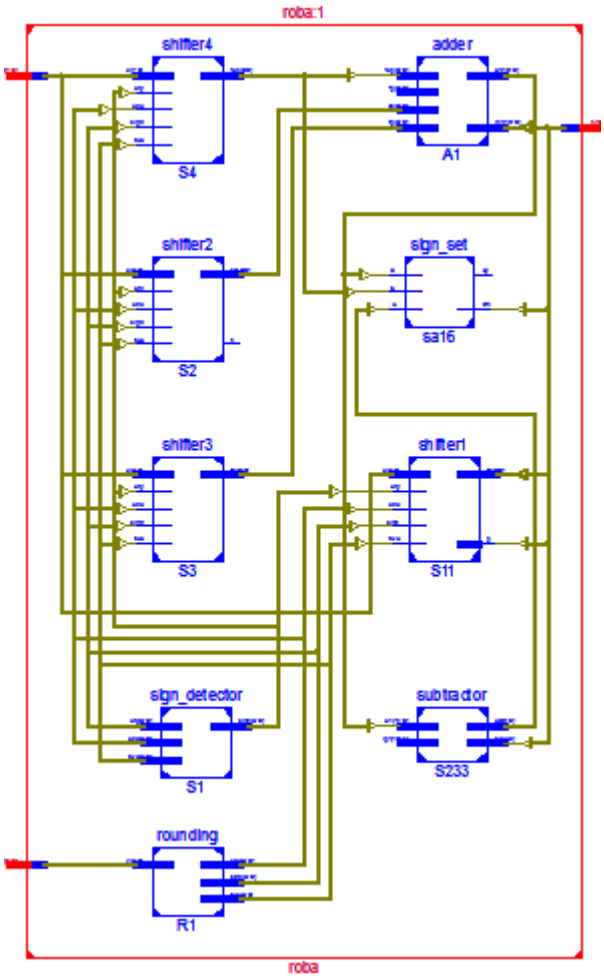

Fig 4: RTL Schematic

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Data Path: y<1> to p<14>
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O            33   1.218   1.438  y_1_IBUF (cry<0>)
   LUT4:I0->O            2   0.704   0.622  S11/p2/k_2_or0000 (S11/p2/k<2>)
   LUT4:I0->O            4   0.704   0.666  S11/p2/ca1 (S11/n<2>)
   LUT3:I1->O            2   0.704   0.622  S11/p4/Mxor_p_Result1 (fp<4>)
   LUT3:I0->O            2   0.704   0.526  A1/h2/m1/o1 (ip1<2>)
   LUT4:I1->O            2   0.704   0.482  S233/cla1/c_1_or00001 (S233/cla1/c<1>)
   LUT3:I2->O            2   0.704   0.526  S233/cla1/c_2_or00001 (S233/cla1/c<2>)
   LUT3:I1->O            2   0.704   0.526  S233/cla1/c_3_or00001 (S233/c2<0>)
   LUT3:I1->O            2   0.704   0.482  S233/cla2/c_0_or00001 (S233/cla2/c<0>)
   LUT3:I2->O            2   0.704   0.526  S233/cla2/c_1_or00001 (S233/cla2/c<1>)
   LUT3:I1->O            2   0.704   0.482  S233/cla2/c_2_or00001 (S233/cla2/c<2>)
   LUT3:I2->O            2   0.704   0.526  S233/cla2/c_3_or00001 (S233/c2<1>)
   LUT3:I1->O            2   0.704   0.482  S233/cla3/c_0_or00001 (S233/cla3/c<0>)
   LUT3:I2->O            2   0.704   0.526  S233/cla3/c_1_or00001 (S233/cla3/c<1>)
   LUT3:I1->O            2   0.704   0.482  S233/cla3/c_2_or00001 (S233/cla3/c<2>)
   LUT3:I2->O            1   0.704   0.420  S233/cla3/Mxor_n<3>_Result1 (p_14_OBUF)
   OBUF:I->O                 3.272          p_14_OBUF (p<14>)
  ----------------------------------------
  Total                     24.384ns (15.050ns logic, 9.334ns route)
                                     (61.7% logic, 38.3% route)
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Fig 4: Timing Report

2.1. On-Chip Power Summary

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.00	0	---	---
Logic	0.00	156	9312	2
Signals	0.00	146	---	---
IOs	0.00	32	232	14
Quiescent	80.98			
Total	80.98			

Fig 6: Power Report

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	86	4656	1%
Number of 4 input LUTs	156	9312	1%
Number of bonded IOBs	32	232	13%

Fig 7: Design Summary

Conclusion

In this paper we propose a Modified rounding based accurate multiplier (MROBA). By modifying the conventional multiplier for the accurate results. Compared with the conventional multiplier the modified multiplier gives exact result to the given inputs and the multiplier can also perform operations which are not in the form of 2n (as performed in the conventional method) so, the exact result can be obtained for the numbers irrespective of 2n . The MROBA is designed using Xilinx ISE 14.2 and results are shown above and other parameters like area power delay are been calculated using cadence encounter and the design of MAC unit is also implemented in Xilinx ISE 14.2.

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