# Comparative Analysis of 64-bits 6T SRAM Design using 90 nm and 180 nm Technology

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***Abstract*** - Ever rising demands of battery operated portable device in market is encouraging the VLSI manufactures to reduce the power leakage of the electronics devices so that battery backup can be increased. Due to the fast improvement for low voltage, low power memory design throughout recent years SRAM has become the issue of significant research to meet up the requirement for laptops, Integrated Circuit (IC) memory cards, notebooks and other electronics devices. Static Random Access Memory (Static RAM or SRAM) typically dominates the biggest share of the electronics system. SRAM have a broad range of applications, due to its many exceptional characteristics including huge storage density, small access time and high noise protection. The power consumption and speed of SRAMs are most significant matter that provides a clarification which describes various designs that optimize the utilization of power. This article is based on the motivation of reduction of the average power consumed in SRAM memory and focuses on the analysis in terms of power dissipation, delay and power delay product of the 6-transistors SRAM memory cell at 90 nm and 180nm CMOS technologies by using the Tanner tool which is having a supply voltage of 1.8 volts. The circuit verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit.

***Keywords*** - *Low power, delay, power-delay product, SRAM and CMOS.*

## I. INTRODUCTION

SRAM cell is composed of six MOSFETs namely M1, M2, M3, M4, M5 and M6 (refer Figure 1). Two cross coupled inverters are formed by four transistors (M3, M4, M5, and M6). Each bit in a memory is stored on these inverters. This memory cell has two stable states which are described as 0 and 1. Two extra access transistors (M1 and M2) control the access to a memory cell during read and write modes. In addition to such six-transistor (6T) SRAM, other varieties of memory cells use 4, 8, 10 (namely as 4T, 8T and 10T SRAM), or more transistors per bit. 4T memory cell is familiar in stand-alone SRAM devices used for CPU cache memory, executed in special processes with an additional layer of polysilicon, enabling for very high-resistance pull-up resistors. The major disadvantage of 4T memory cell is its increased static power due to the uninterrupted current run through one of the pull-down transistors [5].

In 1-bit 6T SRAM Cell, Bit Lines (BL and BLB) are used to store the data and its compliment. Word Line (WL) is used for allowing the access transistors M1 and M2 for write mode which, in turn, control whether the cell should be associated to the bit lines: BL and BLB. They are used to move data for both read and write modes. The size of an SRAM with y data lines and x address lines is 2x words, or 2x × y bits. Generally word size is 8 bits, which means that a single byte can be read or write to each of 2x different words within the memory chip. Various SRAM chips have 10 address lines (thus a capacity of $2^{10}$ = 1024 = 1K words) and an 8-bit word, so they are referred to as "1K × 8 SRAM".

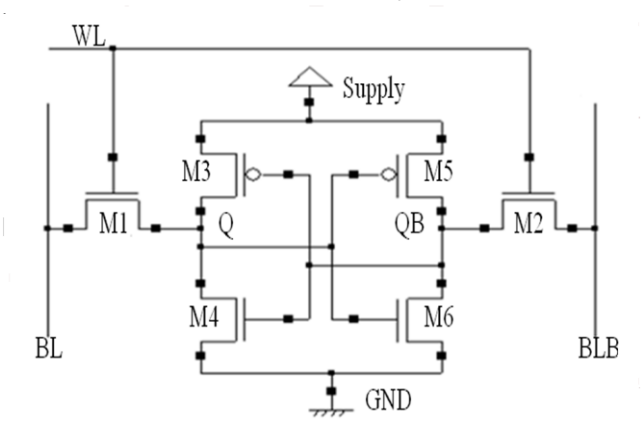


Fig.1: 1-bit 6T SRAM Cell [1]

## II. 1-bit 6T SRAM CELL OPERATION

An SRAM cell has three different states or modes namely standby (the circuit is inactive), reading (the data has been demanded) and writing (renewing the contents). These modes have been briefly discussed below:

### *A. Standby mode*

If the word line is not insisted, the access transistors M1 and M2 separate the cell from the bit lines. The two cross-coupled inverters formed by transistors M3, M4, M5 and M6 will

continue to support each other as long as they are connected to the supply.

*B. Reading mode*

In theory, reading process involves only insisting the word line WL and reading the memory cell state by a single access transistor and bit line, e.g. M2, BLB. The read cycle is in progress by precharging the peripheral module both bit lines BL and BLB, i.e. driving the bit lines to a threshold voltage (midrange voltage between logical 0 and 1). Then insisting the word line WL, permitting both the access transistors M1 and M2 due to which bit line BL voltage either a little falls or rises. It should be noted that if BLB voltage rises, the BL voltage falls, and vice versa. Then the BL and BLB lines will have a small voltage variation between them while getting a sense amplifier, which will sense which line has the higher voltage thus determining whether there was 0 stored or 1.

*C. Writing mode*

The initiate of a write cycle starts by submitting the value to be written to the bit lines. To write a 1, we would submit a 1 to the bit lines. A 0 is written by reversing the values of the bit lines. WL is then insisted and the value that is to be stored is latched in. For write mode one BL is high and the other bit line on low condition. For writing 0 BL is low and BLB is high (refer Figure 2). When we insist the word line high, transistors M1 and M2 are ON. Due to zero value at Q the M5 transistor is ON and M6 transistor is OFF and high value at QB the M3 transistor is OFF and M4 transistor is ON. Transistors M1 and M4 are ON so the charge stored in the BL goes to ground through transistors M1 and M4 path. Due to the M5 transistor is ON and M6 transistor is OFF so the charge is stored at QB.

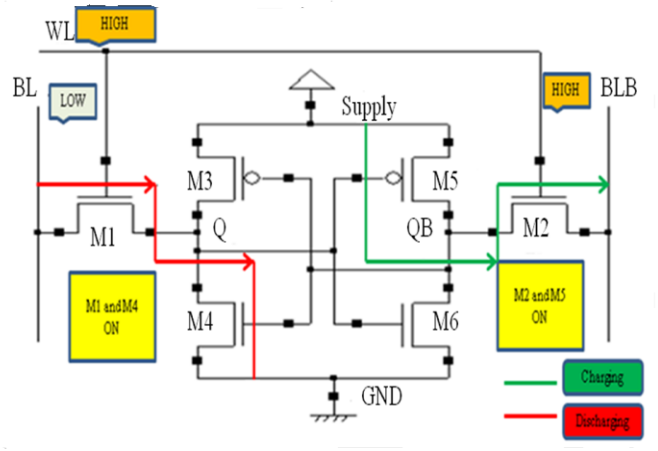


Fig.2: Write 0 Mode 1-bit 6T SRAM Cell

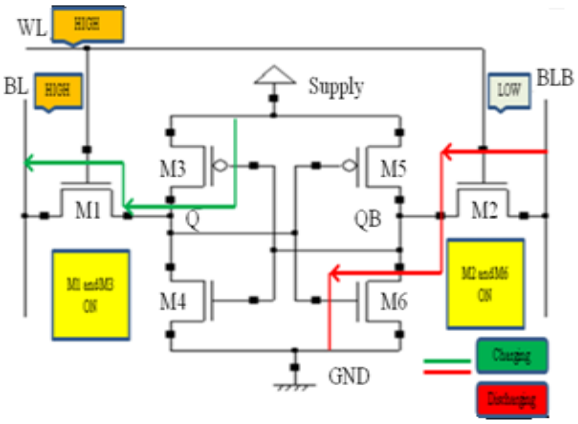


Fig.3: Write 1 Mode 1-bit 6T SRAM Cell

Similarly in the write 1 mode BL is high and BLB is low (refer Figure 3). When we insist the word line high, transistors M1 and M2 are ON. Due to zero value at QB the M3 transistor is ON and M4 transistor is OFF and high value at Q the M5 transistor is OFF and M6 transistor is ON. Transistors M2 and M6 are ON so the charge stored in the BLB goes to ground through transistors M2 and M6 path. Due to the M3 transistor is ON and M4 transistor is OFF so the charge is stored at Q [3].

## III. 64-bits 6T SRAM CELL OPERATION

In this memory cell, all the three different states or modes namely standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents) have same working as 1-bit 6T SRAM Cell, contains 384 transistors. Moreover, word line and bit lines are shared with each 64 SRAM cells which are held in the size of eight rows and eight columns (refer Figure 4).

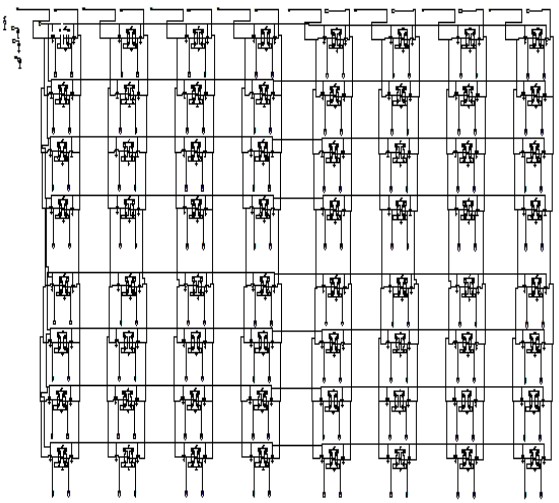

Fig.4: 64-bits 6T SRAM cell

## IV. PERFORMANCE PARAMETERS

### A. Average Power Consumption

Average power consumption has been classified as follows:

- *Dynamic power Consumption*

Dynamic power consumption is further separated into two categories i.e., one is short circuit power and second is power utilization during switching and has been briefly discussed as follows:

*Short circuit power*

The input signals are having finite slopes so that the direct-path currents flow through the gate of the transistor for a small time during switching operation. For this small interval of time, there is a direct path between voltage supply and ground because of which in turn cell consumes huge amount of power.

*Power Consumption during Switching*

When the input signal of CMOS inverter is low, the PMOS transistor switches on and the NMOS transistor switches off and the charge is transferred from supply voltage to the output of the inverter. The parasitic wire capacitances and the gate capacitances of the logic gates combined together make lumped capacitance which in turn is driven by the inverter [4].

When the input Signal of inverter is high, the NMOS transistor switches on and the PMOS transistor switches off. Now the charge stored on lumped capacitance is transferred to ground. This output capacitances use the power during switching and it is called as the dynamic power leakage.

- *Static Power Consumption*

Conventionally, the static element of power utilization has been insignificant in CMOS. But a number of leakage methods initiate to grow significance. Most of these methods are directly or indirectly due to the small device parameters [2].

### B. Propagation Delay

Propagation delay depends upon write delay and read delay and has been briefly discussed as follows:

- *Write delay:* Write delay is the delay between the word line signal and the time at which the data is really written [6, 9].
- *Read delay:* Read delay is the delay between the word line signal and the response time of the sense amplifier or the delay engaged in permitting the bit lines to discharge by almost 10 percent of the peak value [6, 9].

### C. Power-Delay Product

Power-delay product is the product of average power consumption and propagation delay between input signal and output signal. The unit of power-delay product is Watts-Sec [7, 8].

## V. SIMULATION RESULTS AND DISCUSSION

1-bit 6T SRAM cell and 64-bits 6T SRAM cell have been simulated using 90nm and 180nm technology using Tanner tool by taking supply voltage 1.8 V. To make the impartial testing environment all the circuits have been simulated on the same input patterns and different width of NMOS and PMOS transistors. Both the transistors are depending upon specific length λ. Where λ is length which used to find equal rise and fall time in the simulation waveform.

Table 1 shows that average power consumed in 1-bit 6T SRAM is low as compared to conventional 6T SRAM at 90nm and 180nm technologies.

Table 1: Comparative analysis of average power consumption (Watts) between conventional 6T SRAM and 1-bit 6T SRAM using 90nm & 180nm technologies

| Design Style | No. of Transistors | Minimum Length (nm) | Average Power Consumption (watts) |
|---|---|---|---|
| Conventional 6T SRAM [9] | 6 | 90 | 2.2e-004 |
| 1-bit 6T SRAM | 6 | 90 | 1.06e-005 |
| Conventional 6T SRAM [10] | 6 | 180 | 1.32e-004 |
| 1-bit 6T SRAM | 6 | 180 | 1.15e-005 |

Table 2 shows that propagation delay in 1-bit 6T SRAM at both the nodes A and B using 90nm technology are more as compared to conventional 6T SRAM. But in case of using 180nm technology, propagation delay in 1-bit 6T SRAM are less as compared to conventional 6T SRAM.

Table 2: Comparative analysis of Propagation delay (Sec) between Conventional 6T SRAM and 1-bit 6T SRAM using 90nm & 180nm technologies

| Design Style | No. of Transistors | Minimum Length (nm) | Propagation Delay (Sec) |
|---|---|---|---|
| Conventional 6T SRAM [9] | 6 | 90 | 1.9e-010 |
| 1-bit 6T SRAM | 6 | 90 | 9.03e-010 |
| Conventional 6T SRAM [10] | 6 | 180 | 9.6e-010 |
| 1-bit 6T SRAM | 6 | 180 | 7.03e-010 |

Table 3 clearly shows that power delay product at both the nodes A and B in 1-bit 6T SRAM are much lesser as compared to conventional 6T SRAM at 90nm and 180nm technologies.

Table 3: Comparative analysis of Power Delay Product (Watts-Sec) between Conventional 6T SRAM and 1-bit 6T SRAM using 90nm & 180nm technologies

| Design Style | No. of Transistors | Minimum Length (nm) | Power-Delay Product (Watts-Sec) |
|---|---|---|---|
| Conventional 6T SRAM [9] | 6 | 90 | 4.18e-014 |
| 1-bit 6T SRAM | 6 | 90 | 9.57e-015 |
| Conventional 6T SRAM [10] | 6 | 180 | 1.27e-013 |
| 1-bit 6T SRAM | 6 | 180 | 8.08e-015 |

Figure 5 shows output waveforms of 1-bit 6T SRAM cell using Tanner Tool. V(BLB), V(WL) and V(BL) are inputs given to 1-bit SRAM cell and corresponding outputs are V(A) and V(B) which are complements to each other.

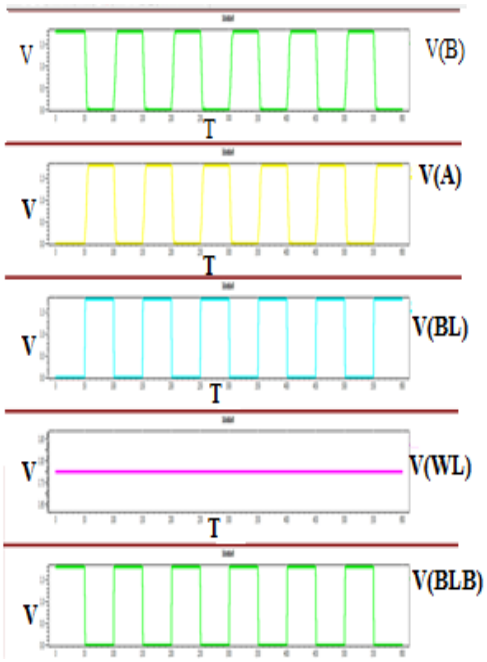


Figure 5 Input and Output waveforms of 1-bit 6T SRAM cell

Table 4 and Table 5 show average power consumption, propagation delay and power-delay product of 64-bits 6T SRAM cell using 90nm and 180nm technology respectively. It is observed that average power consumption, propagation delay and power-delay product at 90nm technology is much lesser than average power consumption, propagation delay and power-delay product at 180nm technology respectively which clearly reveals that scaling down the technology is directly proportional to low power, high speed SRAM circuits.

Table 4: Average power consumption, Propagation delay and Power-Delay product of 64-bits SRAM cell using 90nm technology

| | |
|---|---|
| No. of Transistors | 384 |
| Minimum Length (nm) | 90 |
| Average Power Consumption (Watts) | 6.90e-004 |
| Propagation Delay at A (Sec) | 1.18e-009 |
| Propagation Delay at B (sec) | 2.80e-009 |
| Power Delay Product at A (Watt –Sec) | 8.13e-013 |
| Power Delay Product at B (Watt –Sec) | 19.3e-013 |

Table 5: Average power consumption, propagation delay and power-delay product of 64-bits SRAM cell using 180nm technology

| | |
|---|---|
| No. of Transistors | 384 |
| Minimum Length (nm) | 180 |
| Average Power Consumption (Watts) | 7.50e-004 |
| Propagation Delay at A (Sec) | 1.60e-009 |
| Propagation Delay at B (sec) | 2.94e-009 |
| Power Delay Product at A (Watt –Sec) | 11.9e-013 |
| Power Delay Product at B (Watt –Sec) | 22.1e-013 |

Figure 6 shows output waveforms of 64-bits 6T SRAM cell using Tanner Tool. V (BLB), V (WL) and V (BL) are inputs given to 1-bit SRAM cell and corresponding outputs are V (A) and V(B) which are complements to each other.

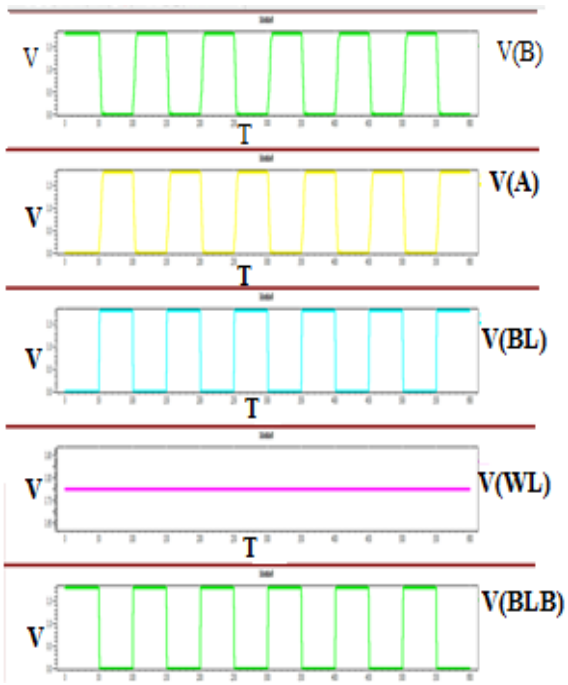


Figure 6 Input and Output waveforms of 64-bits SRAM cell

## VI. CONCLUSIONS

Simulation results indicate that 1-bit 6T SRAM memory cell has lesser average power consumption and power-delay product as compared to the conventional SRAM cell at 90nm and 180nm technologies. So it can be used as today's VLSI design technology. There is also an improvement in the delay in case of newly designed 1-bit 6T SRAM memory cell at 180nm technology as compared to the conventional SRAM cell but in case of 1-bit 6T SRAM memory cell at 90nm it takes more time in comparison to that in the conventional SRAM cell.

In case of 64-bits 6T SRAM memory cell, there is lesser average power consumption, propagation delay and power-delay product at 90nm technology as compare to 64-bits 6T SRAM memory cell at 180nm technology.

So in brief 1-bit 6T SRAM cell consume lesser power and perform the faster operation than the basic existing SRAM cell. Scaling down the CMOS technologies (90nm) gives better result than 180nm CMOS technology.

So this type of memory cell will be more useful in portable electronics and battery operated devices. Also it will require lesser costly heat sink to distribute the heat into the environment.

## IV. REFERENCES

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