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Research Article

Fault Diagnosis using Genetic Algorithm

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Abstract

VLSI testing is used to improve the reliability of the product. The diagnosis is used to identify the fault in the circuit. In this technique used fault table and genetic algorithm for the diagnosis of the circuit. That extends the speed of testing and fault coverage in the circuit. The benchmark circuits are used for the experiment. Reduce the number of test vector required to diagnose the fault. And increase the fault coverage.

Keywords: Diagnosis; Fault table; Testing; Genetic algorithm; Test vector.

Introduction

The physical defect in the circuit cannot be distinguished by the direct mathematical consistency. That physical defect may be designed error or physical defect. It can be modeled as the logical fault models [1]. The fault models majorly classified as structural fault model and functional fault model.

Strictly fault model used model fault in the structure of the circuit and interconnection between the circuits. Functional fault model is used to identify the fault in the function or behavior of the circuit. The circuit having the fault in the circuit is identified known as the faulty circuit. The identified faulty circuit during testing is replaced to increase the reliability of the product. This fault in the circuit is identified by the set of the inputs to the circuit that inputs are known as the test vector. If the test vector, not able distinguishes the two or faults in the circuit then that fault is called as the equivalent fault [2]. The fault that cannot be distinguished can be grouped in the class known as the fault equivalent. The only one fault used to represent an equivalent group of the fault known as the fault collapsing.

By using the fault collapsing [3] the number of test vector to identify the fault is reduced. Fault collapsing is done by fault dominance and fault equivalent. Because of the large scale of VLSI designs, it is impossible to search through the entire design with physical inspections. It is necessary to perform a fault diagnosis to narrow down the possible defect locations. Diagnosis algorithms can be roughly divided into two categories: effect-cause fault diagnosis and cause-effect fault diagnosis.

First, we present some background about diagnostic test generation, including definitions of the exclusive test. It does not require any running diagnostic ATPG [4] or adopting any circuit-modification [5], SAT-based approaches [6,7] or miter-based techniques. For a multiple output circuit, this definition is applied separately to each output. An exclusive test can classify mutually faults as long as they are not being detected at the equivalent outputs. Conceivably a more proper tenure would be a distinctive test. But it is the time-consuming process in testing.

Research methodology

In the proposed method generate a fault table for the circuit and use a genetic algorithm to get the optimal test vector. This genetic algorithm is a search-based optimization technique based on the principles of Genetics and Natural Selection. The flowchart used for the genetic algorithm is given in figure 1.

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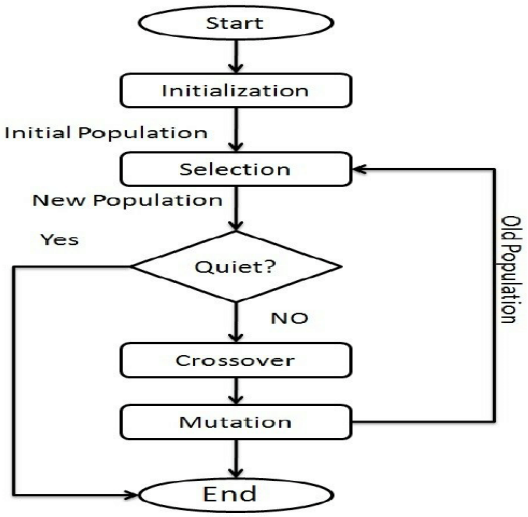

Figure 1. Flow chart for the GA

Pseudo code for GA

Algorithm: GA (n, x, u)
// Initialize generation 0:
t: = 0;
Pt: = a population of n randomly-generated individuals;
// Evaluate Pt:
Compute fitness(i) for each i ∈ Pt;
do
{
{ // Create generation t + 1:

// 1. Copy:
Select (1 − x) × n members of Pt and insert into Pt+1;
// 2. Crossover:
Select x × n members of Pt; pair them up; produce offspring; insert the offspring into Pt+1;
// 3. Mutate:
Select u × n members of Pt+1; invert a randomly-selected bit in each;
Compute fitness(i) for each i ∈ Pt;
// Increment:
t := t + 1;
}
while fitness of fittest individual in Pt is not high enough;
Return the fittest individual from Pt;

It starts with a random population of solution. In each of iteration, the reproduction of new solutions is done In order to get the optimal solution. Reproduction is done by applying the GA sophisticated operators (1) selection (2) crossover (3) mutation. By using the method number of test vector required is reduced .hence the test application time is reduced.

The selection is the first step in this algorithm from the set of solution a number of fitter individuals is selected. It is regularly used to uncover optimal or near-optimal solutions to thorny problems which or else would seize a life span to decipher. It searches for the optimal solution in the elucidation space.

Generated test vector for the benchmark circuits depending on the deterministic method is large. That results in an increase in the testing time. So it is necessary to reduce the test vector to reduce the testing time. In the proposed system using the genetic algorithm, the test vector size is reduced. That's while the testing time will be reduced. The proposed system tests vector, nearly having the nearly same fault coverage for the circuit.

Results and discussion

That will give the diagnostic ability of the test vector for the stuck-at fault in the percentage. For example, consider the benchmark circuit c499 .First step is to generate the test vector using the deterministic test vector. As shown in figure 2.

That shows how much the test vector is required and also gives the fault coverage. In next step generate the same circuit using the genetic method and specifies the mutation rate1 as the 0.001. Now it will give the reduced test vector compared to the previous method. Test vector generated by the proposed method results in figure 3.

This process continues until it satisfying the termination condition this termination condition usually it keeps the following termination conditions' fitness function should possess the following characteristics It must quantitatively measure how to fit a given solution is or how to fit individuals can be produced from the given solution. The fault table is constructed based on the test vector detection of the fault.

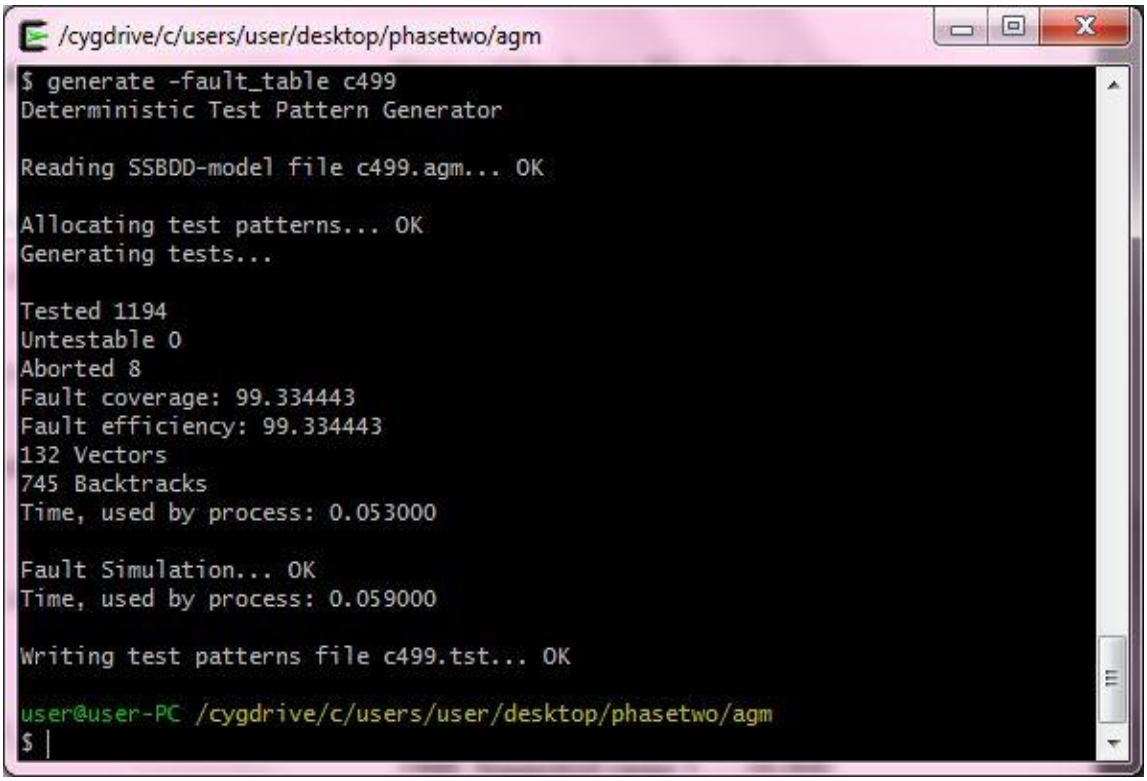

Figure 2. Deterministic test vector for c499

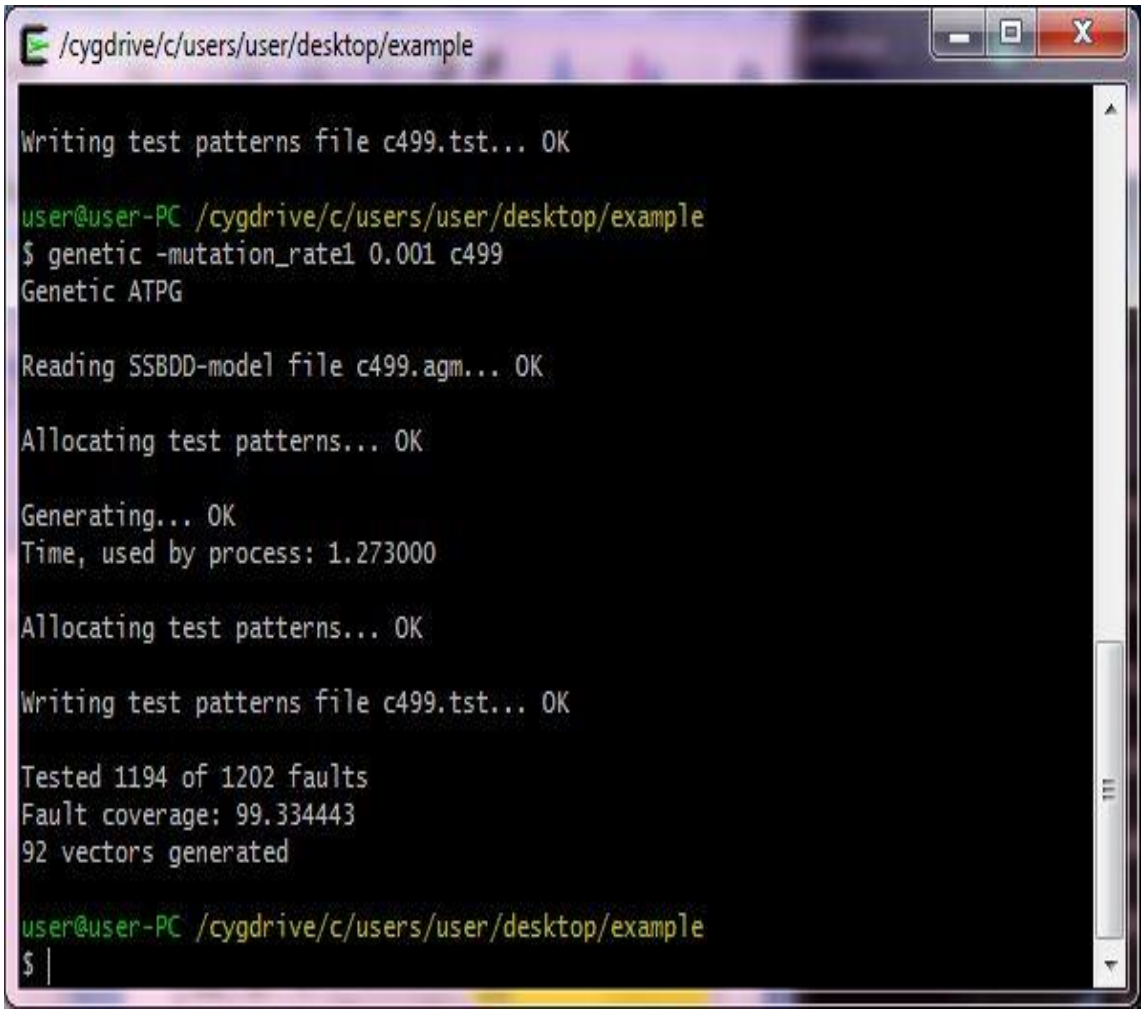

Figure 3. Test vector generated using the genetic algorithm for c499

If the fault is detected using the test vector then marked as 1.If the test vector not able to detect the test vector then it's marked as the '0'.For example, and X for the undetected fault . The termination condition of a Genetic Algorithm is important in determining when a GA will end. It has been pragmatic that primarily, the GA progresses dreadfully swift with enhanced solutions imminent to every iteration. Habitually desire an extinction clause such that our solution is close to the optimal, at the end of the run. For example, in a genetic algorithm, maintain an offset which keeps the way of the generations of the test vector for which there has been no enhancement in the population. Primarily, place this counter to zero. Every time don't produce off-springs which are better than the individuals in the population, increment the counter.

However, if the fitness any of the off-springs are better, then we reset the counter to zero. The proposed system diagnosing ability is measured using the diagnose tool. The reduced test vector for the benchmark circuit ISCAS 85 is given in table 1.

Table 1. Reduced test vector for the benchmark circuit ISCAS 85

S. No.	Circuit	Deterministic ATPG	Genetic ATPG
1	C17	7	4
2	C18	13	11
3	C432	72	52
4	C499	132	81
5	C880	77	47
6	C1355	126	82
7	C1908	139	102
8	C2670	151	66
9	C3540	190	122
10	C5315	167	110
11	C6288	45	22
12	C7552	212	122

Conclusions

By using this proposed method using the fault table and the genetic algorithm it reduces the number of test vector in order to reduce the testing time by using the proposed method. Hence it significantly diminishes the time of the test application time.it is achieved through the mutating and crossover of the test vector. It is even suitable for large circuits. For example, the bench circuit c499 circuit results are given. The future work can involve the multiple stuck at fault further.

Conflicts of interest

Authors declare no conflict of interest.

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