Review Paper on Comparison of Various Techniques in Digital Logic Design

Farah Buch[1], Mr. Anil Bharadwaj[2]
[1]MTech ECE, [2]Asst. Professor ECE
SMVDU

Abstract **-** In the present scenario the functionality and capability of the digital circuits is affected by various factors i.e. low power, size and frequency of operation. These factors are determined by the application for which design is to be considered. The evolutions of mobile systems and advanced deep sub-micron fabrication technologies have brought power consumption a crucial design factor. At present the scaling has done saturation of the devices to the lowest point. There is very less possibility of the scaling of the devices as further scaling of the devices have brought into effect Short Channel effects and Sub threshold Conduction into picture. The other technologies are still in development phase and may be come into existence in the near future. To continue use the present technologies in nanometer domain the new topologies need to be look for in the current regime. In this paper comparison of various design techniques is presented such as adiabatic logic, GDI (Gated Diffusion Input Method) and transistor stacking technique. This paper provides detailed analysis of various techniques so that a better understanding for the techniques can be obtained for the implementation in nanometer regime.

Keywords **-** adiabatic, gate diffusion input, low power dissipation, sub-threshold conduction, stacking**.**

I. INTRODUCTION

Low-power design is required for portable applications as well as high performance systems. As technology shrinks by 0.7/generation more and more devices are integrated on chip to improve speed of operation. Thus functionality of chip is improved and systems with high clock frequencies are emerging. The major issue related to high power dissipation is reliability. With the generation of on-chip high temperature, failure mechanisms are instigated. In VLSI the digital circuits are optimized for various quality metrics such as performance, power dissipation, cost and reliability. As stated "Power dissipation is defined as rate of energy delivered from source to system/device. In battery operated systems, the amount of energy stored within the battery is limited so the power dissipation is important for portable systems as it defines average lifetime of battery. Unfortunately battery technology is not expected to improve battery storage capacity more than 30% every 5 years" [1]. Power dissipation is also crucial for deep submicron technologies. According to Moore's law number of transistors double on chip after every 18 months and thus the operating frequency is also doubled every 3 years. [1] So according to this law we can have same functionality for less cost or more functionality for same cost. Consequently as the power dissipation per unit area grows, the chip temperature also increases. This increased temperature reduces reliability lifetime of circuit.

II. POWER DISSIPATION IN CMOS

As the power is expensive and needs to be minimized in circuit, the various power components contributing to dissipation of power and their effects must be identified. There are two main types of power dissipation. One is the power dissipation which is related to the peak of the instantaneous current and the other is the average power dissipation. The peak current effects supply voltage noise due to the power line resistance. It causes heating of the device, which results in performance degradation. From the battery lifetime point of view, the average power dissipation is most important parameter.

There are three power dissipation components within the CMOS inverter. These are:

A. Static power mainly caused by the leakage current and other Static current I*t due to the value of the input voltage.

B. Dynamic power which is the power dissipated during switching event i.e. when output node voltage of CMOS logic gate makes a logic transition.

C. Dynamic power caused by the short-circuit current during the switching transient where both transistors conduct simultaneously for short amount of time [2]. The short circuit power contributes only ten percent to total power dissipation.

The dynamic power consumption occurs due to the charging and discharging of the parasitic capacitors in the circuit.

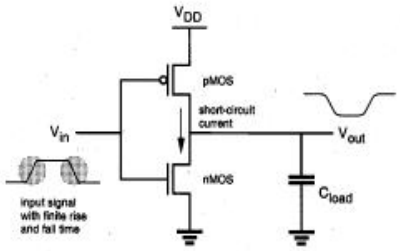

Fig: 1 Dynamic power dissipation

$$P_{avg} = C_L \bullet Vdd^2 \bullet N \bullet fclk \quad (1)$$

Switching power is dissipation occurs due to the energy drawn from power supply when output node capacitance is

charged. No energy is drawn from power supply during charge down phase or discharging of capacitor. The size of drain diffusion area influences the amount of parasitic capacitance at the output node.The average switching power dissipation is independent of size of transistors as shown by Equation(1). Delay time has no relevance to amount of power consumption during switching events.The switching power expression is derived by taking into account into account charging and discharging of output node capacitance.N in equation represents corresponding node transition factor or switching activity associated with node.

The short circuit power dissipation occurs because the gate of CMOS is driven by input voltage waveforms with finite rise and fall time.As both transistors conduct for a short span of time during switching forming a direct path between supply and ground.

$P_{short\text{-}circuit} = k \bullet (Vdd-2Vt)^3 \bullet t \bullet N \bullet f$

Where k is a constant that depends on the transistor size and the technologyV_t is the threshold voltage of the nMOS and pMOS transistors, t is the rise or fall time of the input signal,*N* is the average number of transitions in the inverter's output, and *f* is the clock frequency.The equation shows that short circuit power dissipation is linearly proportional to input signal's rise and fall time and also to the transconductance of transistors.

III. STATIC POWER DISSIPATION

It is usually a small fraction of total power dissipation.Unfortunately as Vth decreases and number of transistors per chip increases in sub nanometer technology the static power dissipation becomes important. In digital circuits, there are three main sources contributing to static power dissipation.

1) Diode leakage current
2) Subthreshold current due to low Vth.
3) Gate oxide leakage current.

Diode leakage occurs due to reverse biasing of p-n junction between drain and bulk of The resulting diode leakage current is given by -

$I=Ad*Js(e\ q*Vbias/KT-1)$

Where Ad is area of drain diffusion and Js is leakage current density.Vbias is the reverse bias voltage across the junction.Typical saturation reverse current density is 1-5pA/um.

Subthreshold leakage current is one of the main sources of static power dissipation in sub nanometer technology due to the carrier diffusion between source and drain regions of transistor in weak inversion region.It occurs under circumstances similar to diode leakage current.In inverter when pMOS is turned off even for Vgs=0V current flows in channel because Vds of pMOS= -Vdd.The Id versus Vds characteristic has an exponential relation in subthreshold region(Vgs<Vth).The magnitude of subthreshold current is determined by process, device size and supply voltage. The gate oxide leakage current also contributes to static power dissipation which can be reduced by changing value of K (dielectric constant)[2].

The actual power dissipation is divided into four major parts:

A. Logic circuits
B. Clock generation and distribution
C. Interconnections
D. Off chip driving

IV. VARIOUS IMPLEMENTED LOGIC TECHNIQUES

The choice of proper logic style at circuit level plays an important role in power saving at circuit level.The logic style is chosen on the basis of required output and the style governs power dissipation of the circuit.The logic style chosen plays a significant role in optimizing power and delay of circuit and also determines speed, size and wiring complexity of circuit.This paper provides insight on various techniques used at circuit level to improve power dissipation.

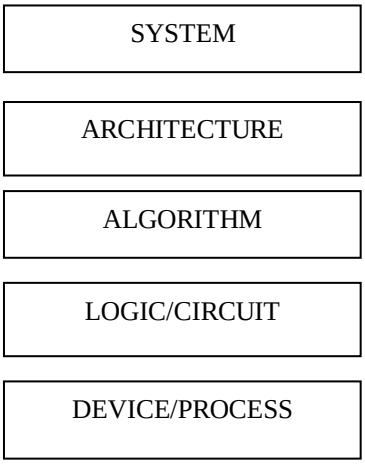

Fig: 2 Optimization at various levels

A. Pass Transistor Logic Styles - In PTL only one transistor is required to perform logic operation thus smaller number of transistors are used.As only nMOS transistors are used, area is reduced thus less delay as well as decrease in power dissipation is obtained.However there occurs threshold voltage drop at output ($V_{OUT} = V_{dd} - V_{th}$) for which swing restoration circuit is necessary at output to obtain exact logic state. Thus inverters are used at gate output leading to increase in area which increases power dissipation.The variable gate inputs are applied to nMOS transistors but only one gate input through each line must be active to avoid short between inputs .Since MUX requires complementary input signals the number of functions that can be implemented efficiently are limited.Thus additional nMOS networks are required which cancels the advantage of low transistor count.[4]

(i) Complementary Pass Transistor Logic - It obtains complementary inputs/outputs using nMOS pass transistor

logic with CMOS output inverter. In CPL, internal dual rail signals (p and p'*)* are typically generated simultaneously to minimize the propagation delay through each circuit block.However, when the outputs of the nMOS pass transistor network are logically high, they are at V_{dd}-V_t, which results in partial turn-off of pMOS in the inverters.Thus results in a high static current[11].

(ii) Double Pass Transistor Logic - It uses both nMOS and pMOS transistors in parallel.Thus full output swing is obtained.In DPL no level restoration circuits are needed and circuit robustness increases at the cost of increased number of transistors leading to more area as well as more power dissipation.

B. Domino Logic - It is one of the dynamic logic techniques where state is based on charge storage.The domino logic circuit operates in precharging as well as evaluation mode.During precharging CLK signal is low ,thus high output is obtained and during evaluation pull down logic block is evaluated based on input applied to transistors.The casacading in dynamic logic gives erroneous output for which buffer is introduced at the output of first stage.A feedback device is added to improve noise margin as well as to maintain logic state.It is mainly used in circuits where high power dissipation can be afforded for obtaining high speed.

C. CMOS - It consists of pMOS as well as nMOS network.The reason for switching from nMOS to CMOS was because less power dissipation is obtained in CMOS where output is either connected to V_{dd} or ground.The transmission gate which is the combination of an NMOS and a PMOS pass-transistor is mainly used for implementing multiplexers, XOR-gates, and flip-flops efficiently. Any logic function can be realized by using NMOS pull down and PMOS pull-up networks connected between the gate output and the power lines. [11].

D. Adiabatic Logic Circuits - In adiabatic circuits switching occurs in such a way that energy loss is less than C_L*$Vdd^2/2$.In adiabatic circuits less power dissipation is obtained at the cost of speed.During charging event the energy stored at output node is C_L*$Vdd^2/2$ where as other half is dissipated in pMOS network.In this case during discharging the energy instead of being dissipated in nMOS network is given back to supply.Thus there is recycling of energy which reduces the total energy drawn from power supply[5].As the process cannot be entirely adiabatic in nature,the recovery of full energy is not possible but part of energy is recovered. In adiabatic circuits load capacitances are charged by constant current sources not by constant voltage source. Thus energy dissipation decreases in circuits where T>2RC.

In two phase split clocked adiabatic static CMOS logic(2PASCL).It utilizes the principle of adiabatic switching and energy recovery.The split level sinusoidal power supply is used instead of V_{dd} and V_{ss} which significantly reduces power dissipation .As the switching activity is reduced power dissipation is also minimized[6].

The PFAL(positive feedback adiabatic logic)is one of the partially adiabatic logic techniques which uses sinusoidal voltage as supply voltage.It is a commonly used adiabatic technique which shows better performance in terms of energy consumption,frequency,range and robustness.It has four phases evaluation, hold, recovery and wait.During hold phase output is applied to succeeding stage.

Adiabatic circuits trade dynamic power for delay and require 50 %more area than static CMOS circuits.

E. Gate Diffusion Input - A new technique known as GDI is presented in this paper. It requires three inputs for a simple CMOS inverter.It is a triple input technique where instead of V_{dd} input P is connected to source/drain of pMOS and N input is connected to source/drain of nMOS.The bulk of pMOS is connected to P input and bulk of nMOS is connected to N input. For an n- input transistor the number of inputs in this case is n+2.It permits implementation of wide range of logic functions using only two transistors. For 50% of cases the GDI operates as buffer used for logic level restoration [7].

The main contribution in this paper is that two new cell designs are proposed based on GDI technique .One for modified two input OR gate and another for modified two input XOR gate to achieve implementation of complicated logic functions.Shannon expression can be used where each function is divided into two logic blocks H and J. The input x is used as an enable line of function.For a given value of input one of the function blocks is implemented.The modified GDI cell proposed reduces short circuit component of power consumption to a very small value. Thus using input as feed instead of Vdd and V_{ss} results in huge saving in power consumption [8].

F. Stacking Technique - As the technology is scaled down to subnanometer range, the threshold voltage decreases drastically due to which subthreshold current increases resulting in increase in leakage power.Due to scaling of device short channel effects further decrease the threshold voltage.The scaling of technology also impacts gate oxide thickness.Due to the reduction in thickness tunneling current flows through insulator leading to further dissipation of power.The gate oxide leakage can be reduced by changing value of dielectric constant K.

In MTCMOS scheme, both high threshold as well as low threshold transistors are used in circuit.The threshold voltage of transistors is set in such a way that the output of circuit is not affected.

A new leakage power reduction technique named "sleepy stack." is introduced which obtains ultra low power at sub nanometer regime. During active mode or normal mode the transistors given sleep as input are ON and during standby mode the transistors are OFF cutting circuit from power rails.It combines forced stack technique and sleep transistor

technique.In forced stack technique each transistor is divided into two equal half sized transistors [9]. In sleep stack technique static power dissipation is reduced due to combination of FST and sleep transistors in parallel to one of the transistors where sleep transistors are either in cut off state during sleep model or active mode during normal operation of circuit. Thus ultra low power is achieved at sub nanometer technology. The sleep technique reduces power but cannot retain logic state. By combining the two techniques there is decrease in power dissipation as well as state is saved.

In this paper there is comparable analysis of various leakage reduction techniques.The advantages of various techniques are combined and two novel techniques namely leakage feedback and sleepy stack with keeper are presented.In leakage feedback technique each transistor of base case is replaced by three transistors i.e. stack approach with sleep transistor in parallel. The output is obtained in inverted state which is given as feedback to transistors connected in parallel to sleep transistors [10].

In sleepy stack approach each transistor is divided into three equal sized transistors. Although the state of transistor is retained there is penalty in terms of area. In sleepy keeper approach, an additional nMOS is connected in parallel to sleep transistor which connects output of pull up network to Vdd during sleep mode [12]. The output is strong 1 despite using nMOS in parallel to PUN because output is already stored by sleep transistor during active mode. Similarly pMOS is connected in parallel to pull down sleep transistor which is the only source of ground for pull down network. Thus low power consumption is obtained and area is also reduced.

G. MOS Current Mode Logic - MCML is based on differential pair circuit. In this paper improved design metrics of MCML full adder is obtained compared to CMOS full adder. The MCML full adder consists of replica bias circuit and voltage swing controller which is a proposed load controller. The reference voltage is given as input to voltage swing controller. The voltage of replica bias circuit fluctuates around references voltages until desired output voltage swing is obtained. The reduced voltage swing leads to reduced voltage drop across load leading to decrease in power dissipation [13]. The high speed is achieved as circuit operates in subthreshold region which uses low supply voltage.

H. Dynamic Current Mode Logic - In dynamic logic families high speed is obtained. This technique is implemented using MCML with dynamic logic such that power dissipation as well as delay is reduced. It uses a dynamic current source with virtual GND to eliminate static power and to overcome side effects caused by conventional static source .A 16 bit DyCML is fabricated in this paper managing to attain delay as low as 1.24 ns and power dissipation of 19.2mW at frequency of 400MHZ[14].

Logic style	Advantage	Disadvantage	Trade off	Application
[15][16] Domino	)	There is gate level loading and clock loading in standard domino	Speed and robustness	For simple gates AND, OR. Used in high performance microprocessor for implementing circuits.
	Reduced input capacitance			
	Low switching threshold voltage.			
CPL	Small stack height using only nMOS pass transistor with CMOS output inverter	Quickly degrades output and eats into noise margin	Speed, area, power v/s design time	High frequency application
		Performance degrades due to hot carrier effect by increasing Vth.		
	Internal node low swing which results in reduced current drive but contributes to lowering power dissipation.	Slower operation at reduced supply voltage		
		Increased delay		
CMOS	Least affected as technology scales down.	No bipolar	More delay High power dissipation	Effective in implementing monotonic gates
	Optimal Vth is used in static and dynamic circuits	Some circuits are not practicable		
	Performance is expected to approach Dynamic gates while controlling noise margin	Increased frequency of operation increases power dissipation.		
GDI	Allows implementation using only 2 transistors.	If bulk terminals are not properly biased there will be variation in Vt. Because of floating bulk cells can be improved in SOI which increases cost of fabrication.	Cost v/s perform-ance	Suitable for past low power circuits. PDP and transistor count are lower.
	Reduced power consumption			
	Reduced propagation delay and area of digital circuits.			
MOS CURRENT MODE LOGIC	Small R makes it fast Less parasitic and input capacitance	Complexity of MCML. Constant current source not suitable during Standby.	Speed and power dissipation	Suitable at high operational frequencies. More on design consideration in amplifiers
	Low switching noise	Minimum EDP		
	IR(2*differentially)			
Dynamic current mode logic	Lowest delay among all logic styles	Clock power contributes to 35 % of total power dissipation.	Speed and power dissipation	Used in differential logic styles and are area efficient
	No static power dissipation.	Toggle frequency is higher than conventional CMOS circuits.		Used in implementing arithmetic circuits and XOP based logic design

[17] Adiabatic	Prevents losses due to increase of clock frequency	One logic family has large area implementation required	Less power dissipation at the cost of more delay	Used in devices where power saving is more important
	Charge flows back to trapezoidal or sinusoidal power supply lowering power dissipation.	More delay due to more number of transistors		
		Voltage supply is complex to design in fully adiabatic circuits		
	High noise immunity	Vulnerable to Vth variation.		
	Output voltage swing is IR(2*differentially)	Large load resistance suitable.		

Table1: Comparison of various logic stylesFor low power digital VLSI design

V. RESULTS FROM LITERATURE

Full adder type	Dynamic P.D(in watts) E-6	Static pd(in watts)E-10	Power delay product(sum) E-10	PDP (carry)E^{-8}
CMOS	8.11	2.01	1.76	1.00
CPL	3.99	2.52	1.72	1.00
TGA	2.11	1.82	5.91	1.00e

Table II: Simulation results comparing CMOS with other pass transistor logic styles

Frequency MHz	Supply voltage	Avg. power CMOS(uW) in PFAL
100	1	2.19
100	1.8	8.30
200	1	4.29
200	1.8	16.40

Table III: Simulation results comparing CMOS with adiabatic PFAL at 180nm technology

Design	Delay10^{-11s}	Power10^{-6} W	PDP 10^{-17} J
CMOS	6.793	3.2199	21.86
CPL	5.7385	4.1831	24.0047
GDI-MUX	1.0398	1.0398	3.8186

Table IV: Simulation results for full adders in 0.13um with f=100MHZ and 1.2V V_{dd} at 180nm technology

Techniques	130nm	180nm
Base case	2.29E-07	6.35 E-07
Sleep	8.85E-08	2.2 E-07
Zigzag	9.89E-08	2.55 E-07
Stack	9.74 E-08	3.08 E-07
Sleepy stack	1.34 E-07	3.7 E-07
Sleepy keeper	7.27E-07	3.63 E-07
Sleepy stack with keeper	6.39E-08	1.57 E-07
LF with stack	1.29 E-07	3.3 E-07

Table V: Simulation results showing average power dissipation for full adder using sleep transistor in 0.13um technology using Vdd=1V and pMOS and nMOS of high Vth

VI. DISCUSSION

Various investigations have been carried out and reported in literature to obtain low power dissipation [9] [10][18] [19] [20].

Efficient full adders are crucial in many applications since these are building blocks and often the critical one. Full adder CMOS with only 28 transistors exists but using other logic style better speed, size and improved power dissipation is obtained.

Table II shows slight improvement in power delay product in CPL over CMOS but CPL is not preferred in low power applications because of reduced current drive .In Table III at 180nm technology one of the partially adiabatic techniques is implemented and average power dissipation is dramatically reduced in PFAL. Table IV shows in case of GDI-MUX device count as well as PDP is improved than CPL and CMOS. Table V shows stacking technique in which static power dissipation is dramatically reduced at low scale technology where static power almost approaches dynamic power. The logic style is dependent on the application, the kind of circuit to be implemented, and different performance aspect becomes important, disallowing the formulation of universal rules for optimal logic style.

VII. REFERENCES

[1]. A textbook on Low-Power Digital VLSI Design Circuits and Systems Authors: Bellaouar, Abdellatif, Elmasry, Mohamed.

[2]. Thesis report on New Methodologies for Low Power High Performance Digital VLSI Design by Mohamed W.Allam

[3]. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," in IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079-1090, Jul 1997

[4]. K. Yano, Y. Sasaki, K. Rikino and K. Seki, "Top-down pass-transistor logic design," in *IEEE Journal of Solid-State Circuits*, vol. 31, no. 6, pp. 792-803, Jun 1996

[5]. Nazrul Anuar et al. Faculty of Engineering Gifu University Adiabatic Logic versus CMOS for Low Power Applications.

[6]. P.Bhati and N. Z.Rizvi, "Adiabatic logic: An alternative approach to low power application circuits," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 4255-4260.

[7]. A. Morgenshtein, A. Fish and I. A. Wagner, "Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization," *2002 IEEE International Symposium o and Systems. Proceedings pp. I-477-I-480 vol.1.*

[8]. P. Balasubramanian and J.Joh, "Low power digital design using modified GDI method," International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. Tunis, 2006, pp. 190-193.

[9]. J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 11, pp. 1250-1263, Nov. 2006 P. K. Pal, R. S. Rathore , A. K. Rana and G. Saini, "New low-power techniques:

[10]. Leakage Feedback with Stack & Sleep Stack with Keeper," 2010 International Conference on Computer and Communication Technology (ICCCT), Allahabad, Uttar Pradesh, 2010, pp. 296-301

[11]. R.P.Varma and R.Chandel, "Design and analysis of source coupled logic circuits," *International Conference for Convergence for Technology-2014*, Pune, 2014, pp. 1-6.

[12]. S. H. Kim and V. J. Mooney, "Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design," *2006 IFIP International Conference on Very Large Scale Integration*, Nice, 2006, pp. 367-372

[13]. Manisha Guduri .“Current mode circuit level technique to design summing circuit for ultra low power applications**”** Springer-Verlag Berlin Heidelberg 2016

[14]. M. W. Allam and M. I. Elmasry, "Dynamic current mode logic (DyCML): a new low-power high-performance logic style," in *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 550-558, Mar 2001. .

[15]. J.Benschneider et al. "A 300-MHz 64-b quad-issue CMOS RISC microprocessor," in IEEE Journal of Solid-State Circuits, vol. 30, no. 11, pp. 1203-1214, Nov 1995

[16]. A. Chamas et al., "A 64 b microprocessor with multimedia support," Solid-State Circuits Conference, 1995. Digest of Technical Papers. 41st ISSCC, 1995 IEEE International, San Francisco, CA, USA, 1995, pp. 178-179

[17]. D.Maksimovic V. G.Oklobdzija, B. Nikolic and K. W. Current, "Clocked CMOS adiabatic logic with integrated single-phase power-clock supply," in IEEE Transactions on Very Large Scale Integration (VLSI)

[18]. Vahid Forouzan, Mohammad Reza Taheriz, Keivan Navi, Arash Azizi Mazreah, Design of two Low-Power full adder cells using GDI structure and hybrid CMOS logic style, Integration, the VLSI Journal, Volume 47, Issue 1, January 2014, Pages 48-61, ISSN 0167-9260.

[19]. Arpan Singh Rajput, Rajesh Parashar "VLSI Design and Performance Analysis of Different Full Adder Topologies at 0.25 Micrometer Technology Node "International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 8, August 2014

[20]. Uming Ko, T. Balsara and Wai Lee, "Low-power design techniques for high-performance CMOS adders," in IEEE. Transactions on Very Large Scale

.