International Journal of Modern Science and Technology *Vol. 2, No. 6, 2017. Page 243-248.*
http://www.ijmst.co/ ***ISSN: 2456-0235***.

Research Article

Design of area efficient and low power carry select adder

S. Sivaranjani*, G. Kavitha

Department of Electronics and Communication Engineering, Arasu Engineering College, Kumbakonam - 612501. India.

*Corresponding author's e-mail: sivaranjanisiva15@gmail.com

Abstract

High performance digital adders with less power consumption and reduced area are a fundamental design issues for advanced processors. Carry select adders is one of the fastest adder in many processors to perform fast arithmetic function. The speed of operations such an adder is limited by carry propagation from input to output. This project discusses about the implementation of Carry Select Adder (CSLA) with Binary to Excess-1 Code converters (BEC) and Multiplexer. The BEC is used to improve the speed of addition. The main advantage of BEC logic comes from the lesser number of logic gates than the Full Adder structure. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The CSLA are simulated and synthesized using Xilinx ISE 12.1v software.

Keywords: Carry Select Adder; Ripple Carry Adder; Binary to Excess Code converters; Multiplexer.

Introduction

Design of area and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. The design architecture of high speed and low power VLSI needs efficient arithmetic processing units, which are optimized for the performance parameters i.e. speed and power consumption. Addition is one of the basic fundamental arithmetic operators. Adders are the important components which are commonly found in many different blocks of microprocessors, microcontrollers and digital signal processing chips. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position [1].

Ripple Carry Adder (RCA) uses the simple design but it has the main drawback of Carry Propagation Delay [2]. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux) [3].

Research methodology

Ripple Carry Adder

The Ripple carry adder is constructed by using cascading full adder (FA) blocks in series. The basic computation elements are a full adder (FA) [4]. It accepts three binary and carry in respectively and the two outputs are the sum and the carry-out (Cout). A Ripple carry adder is built by connecting the full adder, so that the carry out from each full-adder is the carry-in to the next stages, the sum and carry bits are generated sequentially starting from the LSB, the speed of the RCA is determined by the carry propagating time. The main advantages of this RCA are low power computation and compact layout design smaller chip area.

Multiplexer

A multiplexer is a device used to select one of the several analog or digital inputs. This input is then fed to the output line. The selection of the particular input depends on the select lines. A multiplexer with 2n inputs will have n select lines. The combination of these select lines determines the input which has to be routed to the output. A multiplexer is also known as data

Received: 28.05.2017; Received after Revision: 05.06.2017; Accepted 05.06.2017; Published: 25.06.2017

selector. The multiplexer can select the carry out will be 0 or 1.

Binary To Excess 1 Converter

A Binary to excess-1 code converters (BEC) to improve the speed of addition [5]. This logic can be implemented with any type of adder to further improve the speed. Using BEC instead of RCA in the regular CSLA we can achieve lower area and power consumption[6]. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder structure.

The basic work is to BEC in the regular CSLA to get lower area and improved speed of operation. This logic is replaced in RCA with Cin=1. This logic can be implemented for different bits which are used in the modified design. The major advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder structure. As stated above the main idea of this work to use BEC instead of the RCA with Cin=1 in order to decrease the area and increase the speed operation in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, an n+1 bit BEC logic is required. The function table of a 6-bit BEC are shown in table 1.

Table 1. Function table of the 6-bit BEC

B[5:0]	X[5:0]
000000	000001
000001	000010
000010	000011
111111	000000

The Boolean expressions for the 8-bit BEC logic are expressed as,

X0 = ~B0.
X1 = B0^B1.
X2 = B2^ (B0 & B1).
X3 = B3^ (B0 & B1 & B2).
X4 = B4^ (B0 & B1 & B2 & B3).
X5 = B5^ (B0 & B1 & B2 & B3 & B4).
X6 = B6^ (B0 & B1 & B2 & B3 & B4 & B5).
X7 = B7^ (B0 & B1 & B2 & B3 & B4 & B5 & B6).

Carry Select Adder

Conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path [7]. However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder [8].

BEC is used to improve the speed of addition [9]. This logic can be implemented with any type of adder to further improve the speed. Using BEC instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder structure. The basic idea of the proposed work is by using n-bit BEC to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using instead of RCA in the regular CSLA we can achieve lower area and power consumption [10]. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder structure. The Carry Select Adder using Binary to Excess-1 Converter is shown in figure 1. Finally, the multiplexer can find the carry out 0 or 1.

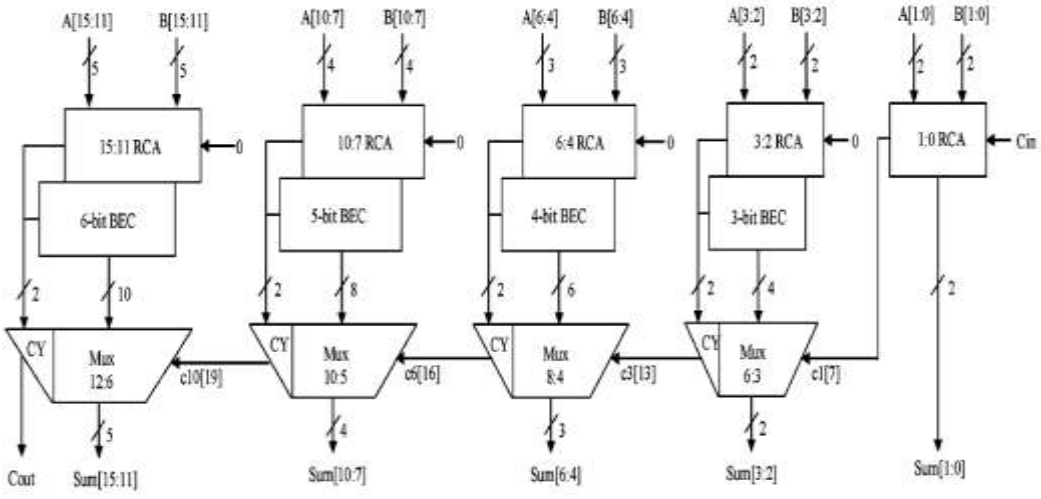

Figure 1. Block Diagram for CSLA using BEC

Results and discussion

Proposed Carry Select Adder

The proposed carry select adder waveform is shown in figure 2. The a[10:0], b[10:0] and Cin are the inputs. The sum[10:0] and Cout are the outputs. The input of a[10:0] and b[10:0] is given as “11110010001” and “01101010011” and Cin is “1”. The output of sum[10:0] is “01011100101” and the carry out is “1”.

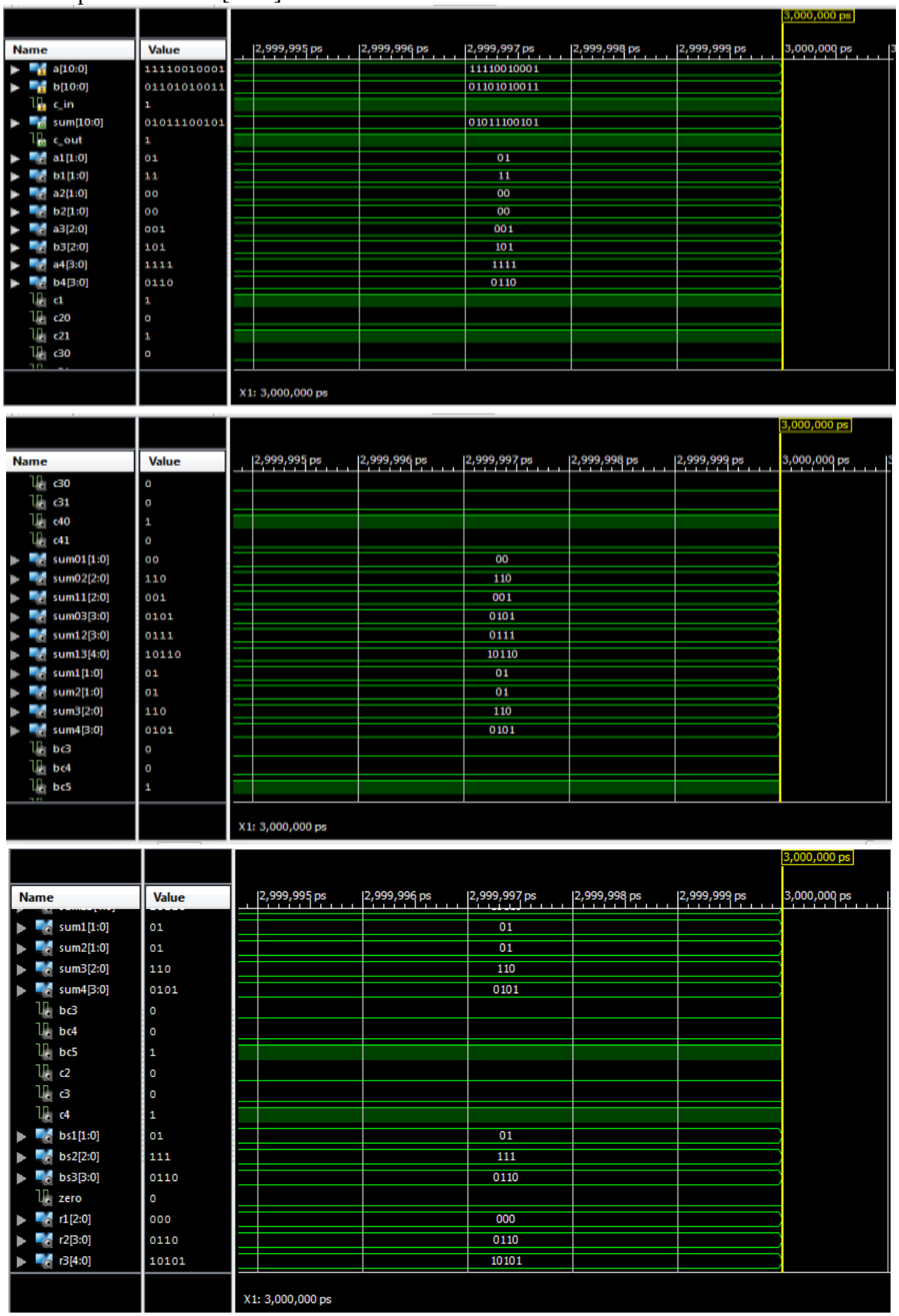

Figure 2. Various Output Waveform for Carry Select Adder

RTL View for Carry Select Adder

The RTL view of the carry select adder is shown in figure 3. The a(10:0), b(10:0) and Cin are the inputs and the sum(10:0) and Cout are the outputs. The number of multiplexer and the binary to excess-1 code converters are shown in figure 4.

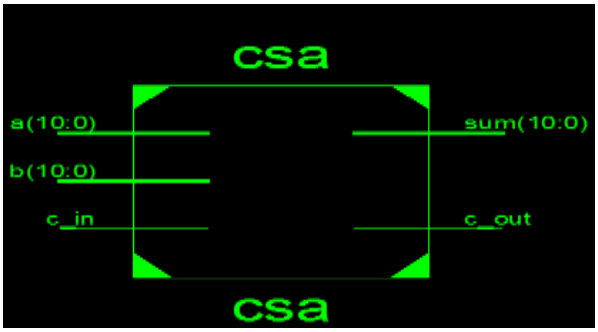

Figure 3. RTL View for Carry Select Adder

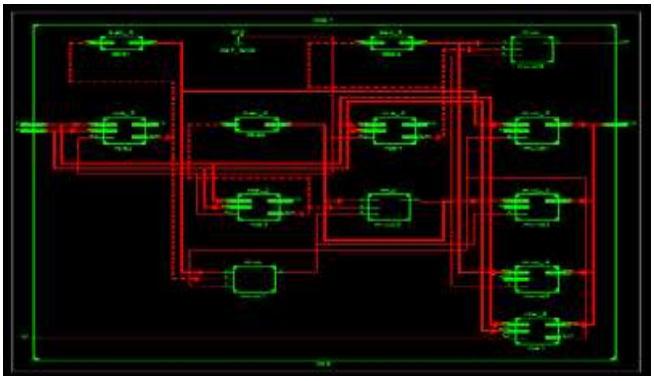

Figure 4. Multiplexer and the binary to excess-1 code converter

LUT'S used in CSLA

The technological schematic of a proposed carry select adder is shown in figure 5. The technological schematic is obtained only after completing the synthesis process to the targeting phase. It tells about the design by using logic elements in terms of LUTs, carry logic, I/O buffers and other logical components. By viewing this it allows you to see a technology-level representation of HDL optimized for architecture, it will help us to discover design issues early in the design process. adder. The technological schematic is obtained only after completing the synthesis process to the targeting phase. It tells about the design by using logic elements in terms of LUTs, carry logic, I/O buffers and other logical components. By viewing this it allows you to see a technology-level representation of HDL optimized for architecture, it will help us to discover design issues early in the design process. The number of LUT's are used in the carry select adder. But in the proposed carry select adder only 33 LUT's are used as shown in figure 5.

Floor Plan for CSLA

The floor plan for carry select adder is shown in figure 6.

Area Report

The table 2 shows the design utilization of carry select adder. The number of 4 input LUT's are available 9,321 but in the proposed carry select adder is only 33 4-input LUT's are used. The total number of occupied slices are 4,656 but in the proposed carry select adder is only 19 slices are used.

Power Report

The figure 7 shows the power result for carry select adder. The 0.139 watts total power can be used in the carry select adder and the Max. Temperature and the ambient temperature is 96.2 and 28.8.

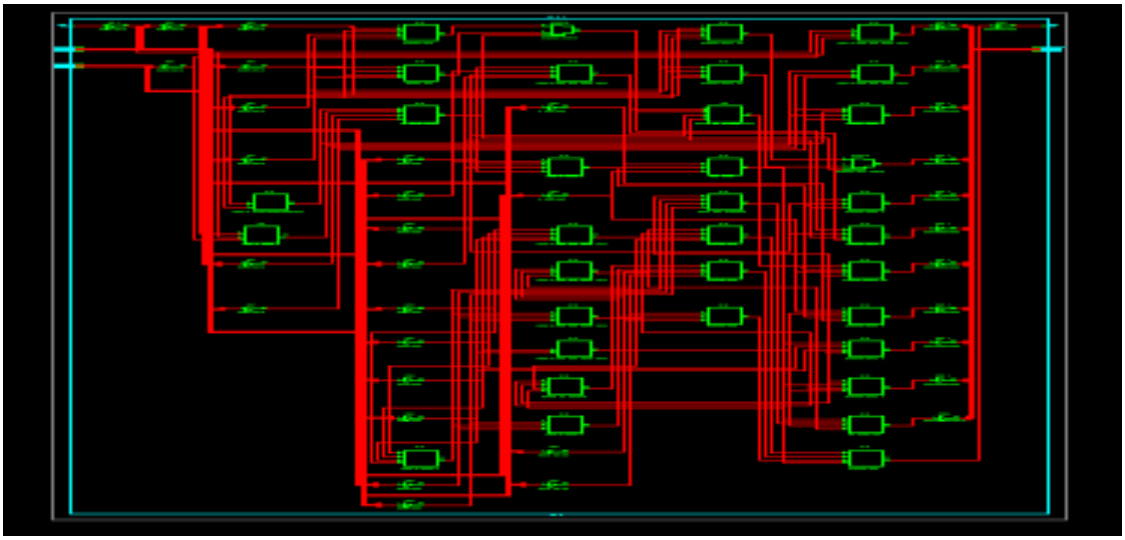

Figure 5. Number of LUT's used in CSLA

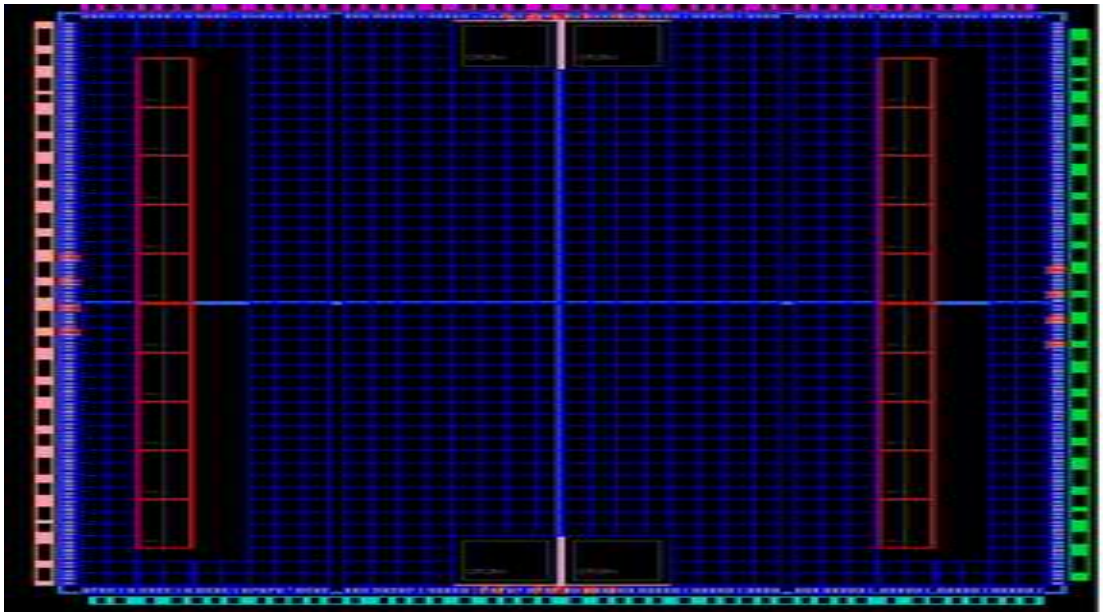

Figure 6. Floor Plan for CSLA

Table 2. Design Utilization of Carry Select Adder

Logic utilization	Used	Available	Utilization
Number of 4 input LUT's	33	9,321	1%
Number of occupied slices	19	4,656	1%
Number of slices containing only related logic	19	19	100%
Number of slices containing only unrelated logic	0	19	0%
No. of bonded IOBs	35	232	15%

Device	
Family	Spartan3e
Part	xc3s500e
Package	fg320
Grade	Industrial
Process	Maximum
Speed Grade	-4

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-23-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	33	9312	0.4
Signals	0.000	54	---	---
IOs	0.000	35	232	15.1
Leakage	0.139			
Total	0.139			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	26.1	96.2	28.8

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.041	0.000	0.041
Vccaux	2.500	0.034	0.000	0.034
Vcco25	2.500	0.004	0.000	0.004

	Total	Dynamic	Quiescent
Supply Power (W)	0.144	0.000	0.144

Figure 7. Power result

Conclusions

The main idea of this project is to introduce the high performance and power efficient Carry Select Adder can be designed by using binary to excess-1 converter and a multiplexer. A Binary to Excess-1 code converters improved the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full

Adder structure. Therefore, the proposed Carry Select Adder is low area, low power, simple and efficient for VLSI hardware implementation.

Conflicts of Interest

Authors declare no conflict of interest.

References

[1] Ramkumar B, Harish MK. Low-Power and Area-Efficient Carry Select Adder. IEEE Transactions on Very Large Scale Integration Systems. 2012;20(2):371-375.

[2] Padma Devi, Ashima Girdher, Balwinder Singh. Improved Carry Select Adder with reduced area and Low power Consumption. International Journal of Computer Applications. 2010;3(4):14-18.

[3] Raut VG, Ashwini L. Design of Carry Select Adder for FIR Filter. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering. 2015;4(3):1348-1351.

[4] Charan Kumar B, Uday Kumar A. A 64-bit kogge stone carry save adder is designed for reducing area by using zero finding logic. International Journal of VLSI System Design and Communication Systems. 2017;5(1):8-11.

[5] Deepak Kumar P, Raksha C, Minal S. An Efficient VLSI Architecture for Carry Select Adder Without Multiplexer. International Journal of Computer Applications. 2015;127(93):37-40.

[6] Golda Hepzib K, Subha CP. A novel implementation of high speed modified brent kung carry select adder. 10th International Conference on Intelligent Systems and Control. Coimbatore, India. 2015.

[7] Nithin P, Udaya Kumar N, Bala Sindhuri K. Implementation of 16-bit Area Efficient Ling Carry Select Adder. International Journal of Advanced Information Science and Technology. 2016;5(9):57-63.

[8] Nithin P, Udaya Kumar N, Bala Sindhuri K. Implementation of 32-bit Carry Select Adder using Brent-Kung Adder. India Journal of Science and Technology. 2016;9(44);1-7.

[9] Shanigarapu L, Shrivastava BP. Low-Power and High Speed Carry Select adder. International Journal of Scientific and Research Publications. 2013;3(8);1-9.

[10] Sajesh Kumar U, Mohamed Saloj KK, Sajith K. Design and Implementation of Carry Select Adder without using Multiplexers. 1st International Conference on Emerging Technology Trends in Electronics, Communication and Networking. 2012.127(9);37-40.

****

