Power and Delay Optimization in a component of a Ring-VCO based Sub-Sampling PLL.

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***Abstract*—**This paper presents a component (tunable delay cell) of ring-voltage-controlled oscillator (ring-VCO)-based sub-sampling phase locked loop (PLL) at 65-nm technology.we have designed a 8T Tunable delay cellutilizing complementary-metal–oxide–semiconductor (CMOS) logic.The Tunable delay cell is first simulated and compared with traditional results at 65nm technology. We have used the Tanner EDA Tool with version 14.11 in 65nm technology and calculated the various parameters, such as, power, delay and power delay product (PDP), and compared with the existing design circuit. The circuit is simulated for 0.8V-1.2V supply at 65-nm technology, the normal power utilization was observed to be to a great degree low with reasonably low delaywere reported. The power and delay are calculated as39.766 uW and 46.988ps at 65-nm and 1.2V supply voltage.

***Index Terms*—PLL, Complementary MOS, Tanner tool, ring-voltage-controlled oscillator.**

I. INTRODUCTION

To increase the level of integration of phase-locked loops(PLLs) in silicon chips, ring voltage-controlled oscillators (VCOs) arethe most preferred choices than LC VCOs.With the wireless communication industry developing rapidly, CMOS circuits which are low-cost, low-power, high stability become the best wireless communication system solutions. In the communication system, the voltage controlled oscillator (VCO) is the important component, especially in the PLL circuit, clock recovery circuit and frequency integrated circuit, so it is the top priorities. According to oscillator principle, oscillator can be divided into two categories: One is the LC oscillation which is composed of the active devices, coupled with LC resonant circuit. Another one is the loop ring oscillator which is composed of delayed cascade units with a positive feedback.

Tunable digital delay elements are widely used in integrated circuits; e.g. in DLLs and PLLs to generate accurate clocks , in delay-line-based time-to-digital converters, in asynchronous systems processing bundled data to ensure correct system timing , and in continuous-time signal processors (CT-DSP) to set the frequency response . Delay cells are expected to have some or all of following attributes:

♦ Wide tuning range;
♦ Good matching between identically laid out cells;
♦ Low jitter;
♦ Signal-independent delay;
♦ Robust communication, in order to guarantee correct propagation of every input event.

Timing elements, such as D-flipflops (DFF) and latches, are the most critical components in sequential circuits. Their principal function is to sequence operations. The performance of the system is limited by their setup and hold times. For instance, reducing the setup time of a DFF often allows synthesis tools to reduce the physical size of gates in the logic cone that feed the D-input, which can lead to significant reduction in area and power.

II. Ring-VCO-based SSPLL

a. D-Flipflop

D-flipflop is designed by using 8 NAND gates and two inverter circuits as shown in the Fig.1.The circuit is simulated for 1.2V at 65-nm technology. The power and delay for the circuit are 3.6775 uW and 102.89 ps.

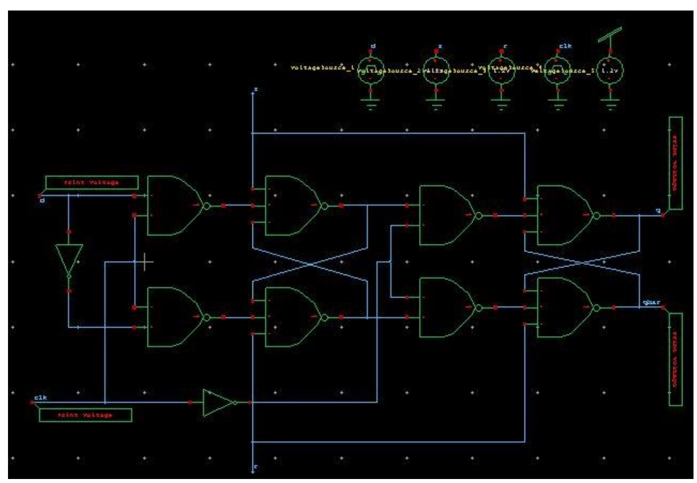

Fig.1. Detail circuit diagram of D-flipflop.

The waveform for D-flipflop is shown in Fig2.

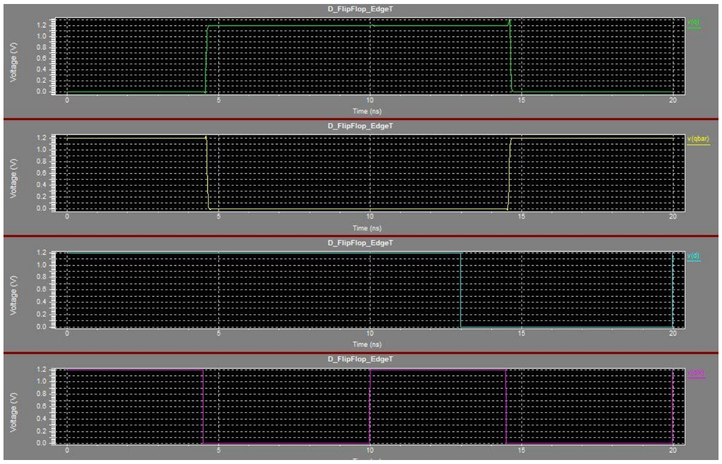

Fig2 waveform of D-flipflop

b. Pulser

The Fig3 below shows the schematic of pulser. The pulser originates the pulse with a reference clock and pulse width can be controlled by *Vtune*.

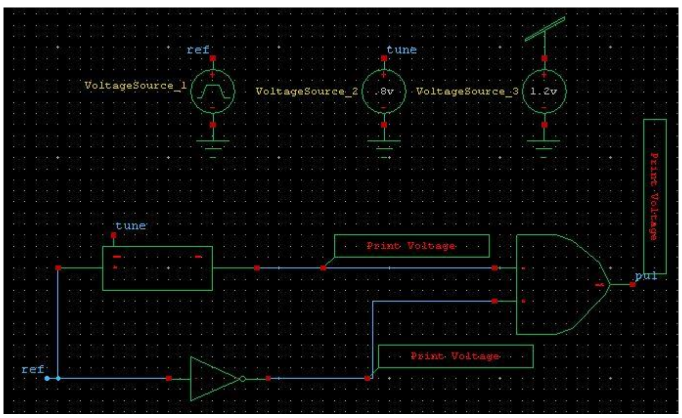

Fig3. Circuit diagram for Pulser.

The pulser circuit is simulated for 1.2V at 65-nm technology and power consumption and delay are 4.9247 uW and 113.87 ps.The waveform for pulser is shown in Fig 4.

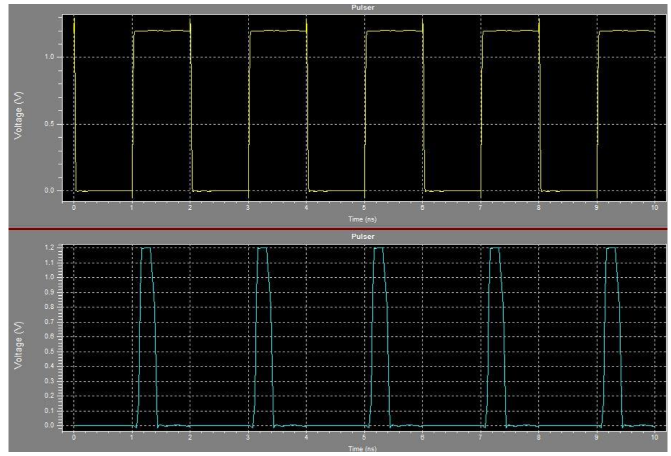

Fig4.waverform for pulser

c. Sub-sampling PD

The sub-sampling PD is designed by using two Nmos with gate connected to ref input and two capacitors of 1fF.The Fig5 shows the circuit of sub sampling PD.

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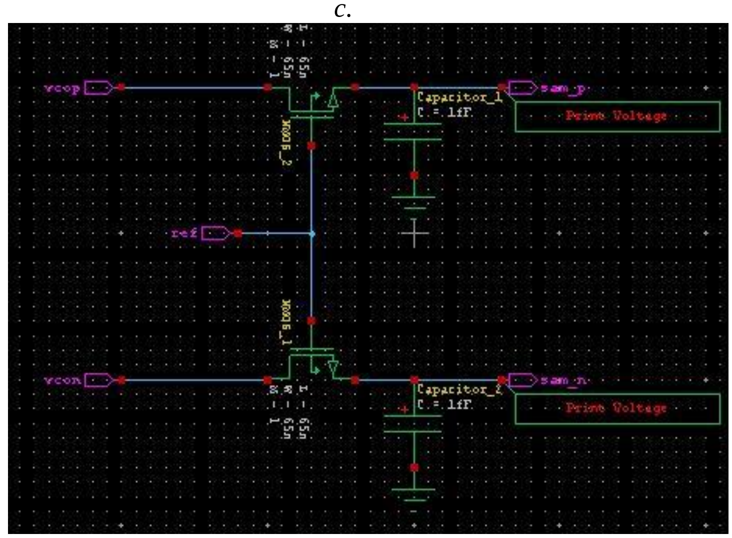

Fig5 circuit of sub-sampling PD

The Fig6 shows the waverform of sub-sampling PD circuit simulated for 1.2V at 65-nm technology.

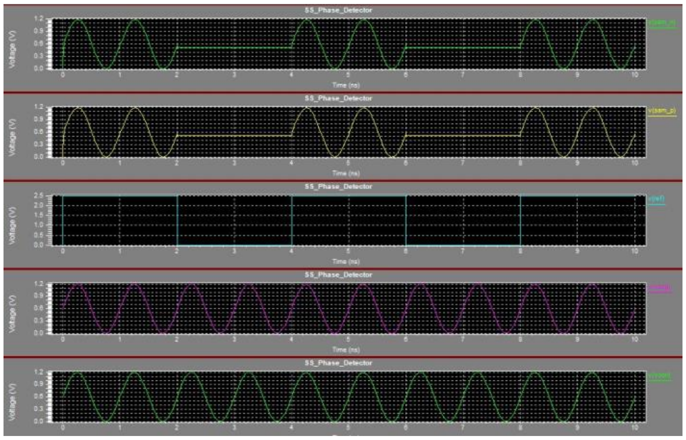

Fig6 waveform of sub-samplingPD

d. Delay cell

The delay cell consists of 9 Nmos and 9 PMOS structures shown in Fig7.

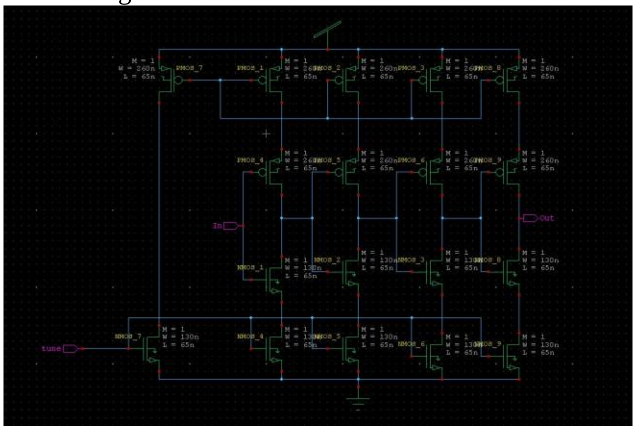

Fig7.circuit for Delay cell.

The waverform for Delay cell is shown in Fig8 simulated for 0.8V-1.2V at 65-nm.

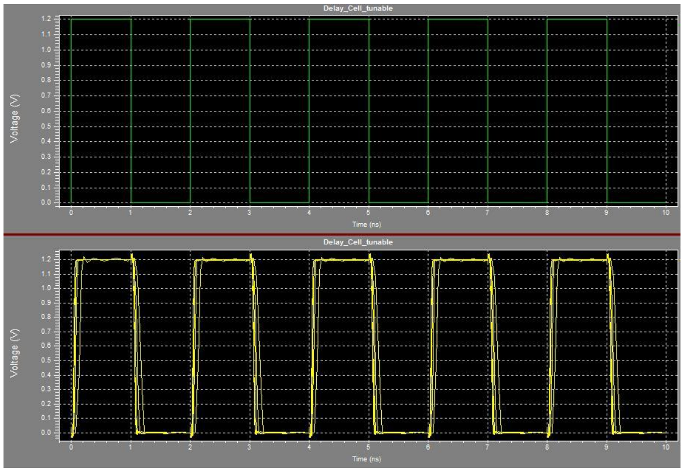

Fig8 waverfom of Delay cell.

III. PROPOSED DELAY CELL

As we know the main building block of an VCO is delay cell. It consumes most of power, So to make VCO circuit low power consuming and high speed applicable we need to modify the Delay cell block. Here we have proposed a Tunable Delay cell with only 8CMOS transistors. So it will consume less power and delay in circuit with less area occupancy. The Fig9 shows the circuit diagram for tunable delay cell.

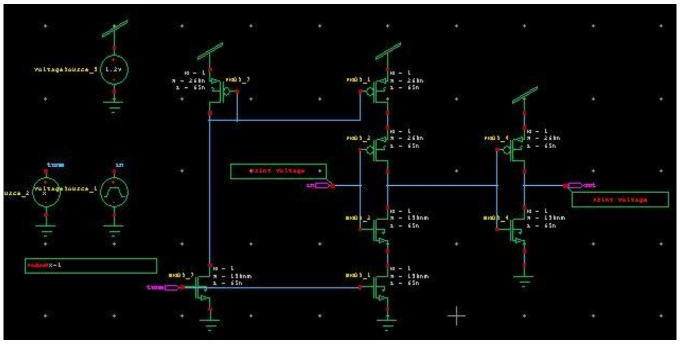

Fig.9 The proposed Tunable delay cell circuit.

The waveform for Tunable delay cell is given in Fig10 and simulated for 0.8V-1.2V at 65-nm technology.The power consumption and delay is calculated for the tunable delay cell circuit and compared with the traditional delay cell circuit.

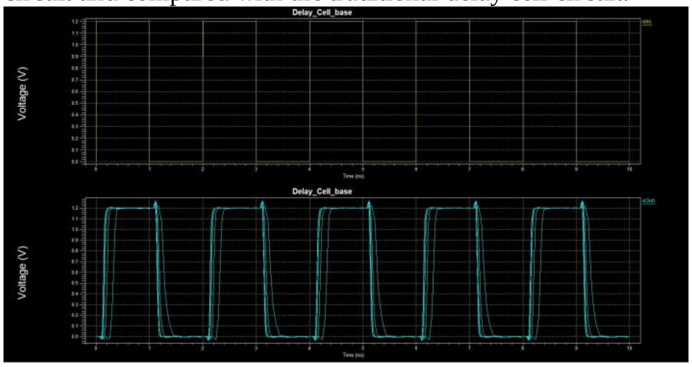

Fig10. Waveform of Proposed Tunable delay cell.

IV. RESULT

The proposed Tunable delay cell circuit also dissipates less power and consumes less area as the number of transistors are reduced. Simulation has been done for power dissipations,delay, power delay product for the proposed tunable delay cell circuit and the results of the proposed circuit are compared with those of traditional delay cell. Result is carried out in 65-nm.

Table 1Results for traditional Delay cell at 65nm Technology

Supply voltage	Power (u)	Delay (p)	PDP(f)	Energy(f)
0.8V	12.813	323.25	4.1417	128.13
0.9V	21.819	204.53	4.4626	218.19
1.0v	31.696	163.61	5.1857	316.96
1.1v	41.746	146.57	6.1186	417.46
1.2v	51.705	137.88	7.129	17.05

Table 2 Results for tunable delay cell circuit at 65nm Technology

Supply voltage	Power (u)	Delay (p)	PDP(f)	Energy(f)
0.8V	8.1517	142.20	1.1592	81.517
0.9V	15.558	80.604	1.2540	155.58
1.0v	23.884	60.863	1.4536	238.84
1.1v	32.186	51.608	1.6610	321.86
1.2v	39.766	46.988	1.8685	397.66

V. CONCLUSION

The simulation doneusing Tanner EDA tool with 65nmtechnology and compared with traditional design approaches. The simulation results showed that the proposed tunable delay cellgives improved delay, power consumption, PDP and Energy compared with the traditional designs. The efficient tunable delay cell with less number of CMOS transistors leads to fast switching speed. The proposed tunable delay cell offered 23.09% improvement with respect to the traditional design of delay cellin terms of Power Consumption (65-nm technology at 1.2 V). The design is simulated at extremely low voltage of 0.8 V at 65nm technology and the power consumption calculated is improved by 36.37% with respect to traditional delay cell. The delay for the proposed circuit is calculated to have been improved by 65.92% at 1.2V and 56.009% at 0.8V.

VI. REFERENCES

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