XSYSTOR

GaN Solutions at your fingertips

CATALOG 2017

Sequencers, Controllers, and Switches for GaN Transistors

Application Checklist
Start design here

System Requirements	100 Controllers	200 Controllers	300 Switches	600 / 700 Eval Board
I prefer to use negative analog input for gate bias	⇩			●
I prefer to use positive analog input for gate bias		⇩		●
I only have one power supply available to the transistor	100X	200X	●	●
I have an additional negative supply available	122X	222X		●
I can provide negative and logic supplies also	124X	224X		●
I need both drain and gate dynamic switching	100X	200X	●	●
I do not need gate switching	120X 122X 124X	220X 222X 224X	●	●
Overall height must be less than 0.25" [6.35mm]	100L	200L		
I want to lay the module flat down to 0.10" [2.54mm] height	100X	200X		
My transistor has CW operation or > 5msec period	●	●	●	●
My transistor has Pulsed operation at < 5msec period with typical pulse width up to 500usec	●	●	332P 362P 392P	●
I have Rise/Fall Time requirements of 200nsec & propagation time of 200nsec in pulsed mode	●	●	335CT 365CT 395CT	●
I want to use multiple switches with just one controller	●	●	●	●
I don't have time to put everything together. I just want to drop-in the whole solution next to my GaN test board				610E 620E 630E 640E
Give me your fastest controller and switch to evaluate. Then I want to remove and reuse the modules for a real application				735E 765E 795E

INDEX

A Quick Summary of our Products…..

Electrical Benefits of the Controller

- It is a sequencer. The primary job is to protect the GaN device from any order of supply and signal voltage turn-ON.
- It stabilizes the transistor. GaN maybe superior but it has a flaw; a tendency to oscillate at low voltages. To avoid instability when ramping or pulsing the drain, the gate is allowed to switch ON & OFF ONLY if drain voltage has reached a safe level. It just takes one TTL enable to activate.
- Operate your GaN from either gate or drain. They have independent control, so you choose based on your application or preference.
- It's a modulator. You can do pulse-width modulation with the gate or dynamic envelope switching with the drain.
- Got Negative? No matter. A single power supply is all that's needed. Onboard inverter produces -4.3V at 30mA. If not enough, then attach another negative source and boost to -6V at 100mA.
- One for all, and all for one! A single controller can switch several GaN devices at once, with about 200mA of total switch loads. However, use op-amp or LDO buffers at each gate for best results.
- Very fast! It can do <<200 nsec Rise, Fall, or Propagation times when used together with our power CMOS Switch products.

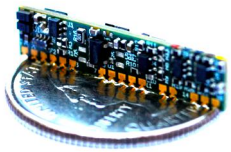
Mechanical Benefits of the Controller

- Half the size of a nickel? At ¼ square inch, it can fit in the most demanding footprint and height restriction. Mount it upright, slanted, or flat.
- Place it anywhere, any direction. Unlike our competitors, our in-line, castellated port design makes it possible to orientate the module 360° with no printed line crossover.

To our valued customers

Thank you for your interest in XSYSTOR products. We make peripheral circuits for the GaN device. They are sequencers, controllers, modulators, and switches that are frequency neutral and can operate devices in L, S, C, X, Ku & Ka-bands. We offer solutions for Broadband Amplifiers, Radar, Milcom, Satcom, Point-to-point radio, and Telecom. In addition to our standard products, our principals have 25 years of RF/Microwave amplifier design experience to offer custom products as well.

100X, 100L, 100T
GaN Controller Module
Power Sequencer, Non-Inverting Analog Input



XSYSTOR

PRODUCT FLYER
July 2017

General Description

The 100 Series GaN Controller is capable of operating and protecting all depletion-mode transistors. The non-inverting analog input accepts negative voltage to produce buffered negative gate bias. It allows 360° board placement with little or no line crossovers in the main board. A single power supply is enough for the 100 to provide dynamic control. Little or no filtering is needed in heavy RF environments. The 100 works seamlessly with 300 and 400 Series MOS switches that have compact footprints for locating near the transistor drain choke. It comes in evaluation boards that are ideal for fast prototyping.

Features

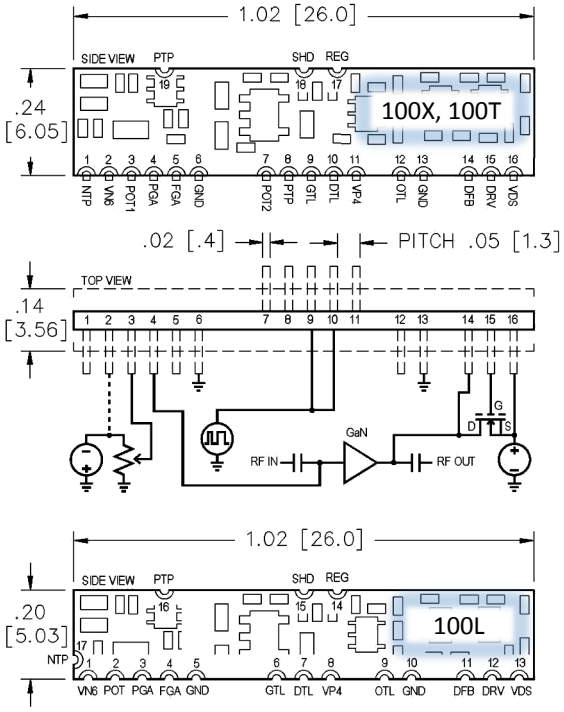
- Protects GaN devices from any power sequence of voltage supplies.
- Internal Negative voltage with 30mA OR external supply for 100mA boost.
- Bias Voltage has Fixed Gate OR Pulsed Gate configuration.
- Simultaneous Gate-Drain sequencing OR Independent Gate/Drain control.
- TTL OR Open Drain (<300mA) output drive for MOSFET switches.
- Temp compensation from local OR remote temp sensor feedback.
- >25dB EMI/RFI Rejection at all I/O ports except from auxiliary taps.
- <500 nsec total delay from V_Logic to V_Drain with applicable switch.
- RoHS* Compliant

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+20 V	+65 V
Supply (-) Voltage, Optional	-6 V	0 V
TTL Voltage Logic High	+3.6 V	+5.0 V
TTL Voltage Logic Low	0 V	+1.4 V
Internal (-) Supply V, Gate Pinchoff	-4.3 V	
Internal (-) Supply I	-30 mA	
Gate Bias Voltage Range	-4.3V	-0.5 V
Out Switch Drive, Open Drain (V)	0 V	+60 V
Out Switch Drive, Open Drain (I)		300 mA
Output ON Prop Delay (T_Delay 1)		120 ns
Output ON Fall Time (T_Fall 1)		120 ns
Output OFF Prop Delay (T_Delay 5)		80 ns
Output OFF Rise Time (T_Rise 3)		80 ns
Gate ON Prop Delay (T_Delay 3)		160 ns
Gate ON Rise Time (T_Rise 2)		60 ns
Gate OFF Prop Delay (T_Delay 4)		160 ns
Gate OFF Fall Time (T_Fall 2)		60 ns
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Open Drain Output with pull-up resistor. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Typical Connection Diagram

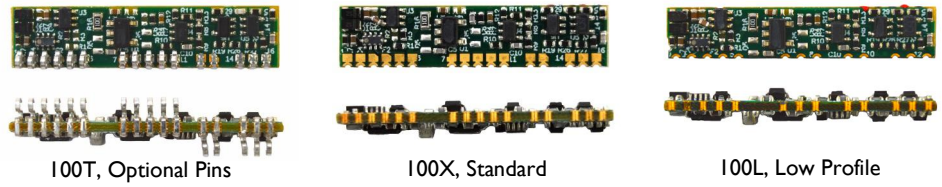


LABEL	PIN 100X 200X	PIN 100L 200L	DESCRIPTION
NTP	1	17	Aux Negative Voltage Tap
VN6	2	1	Optional Neg (-) Supply
POT	3	2	Gate Voltage Input Adjust
PGA	4	3	Pulsed Gate Voltage Out
FGA	5	4	Fixed Gate Voltage Out
GND	6	5	Ground
POT	7		Connected to Pin 3
PTP	8		Aux Positive Voltage Tap
GTL	9	6	Gate Pulse Logic Enable
DTL	10	7	Drain Pulse Logic Enable
VP4	11	8	Optional Logic (+) Supply
OTL	12	9	Active-Low TTL Driver
GND	13	10	Ground
DFB	14	11	MOS Drain Feedback
DRV	15	12	Open Drain MOS Driver
VDS	16	13	High Voltage Supply
REG	17	14	Aux Regulator Output
SHD	18	15	Aux Gate Threshold Adj
PTP	19	16	Aux Positive Voltage Tap

Ordering Information

Model ^	
100_02R6 100_02R0 100_01R4 100_00R8	UNIVERSAL GaN CONTROLLER: NEGATIVE ANALOG INPUT, SINGLE DC SUPPLY, VGS SHUTDOWN AT -2.6V THRU -0.8V**. INDEPENDENT OR SEQUENTIAL SWITCHING OF DRAIN AND GATE
120_02R6 120_02R0 120_01R4 120_00R8	DRAIN CONTROLLER: 100_ WITH NO GATE SWITCHING CAPABILITY
124_02R6 124_02R0 124_01R4 124_00R8	BASIC SEQUENCER: 100_ WITH NO GATE SWITCHING, NO INTERNAL NEGATIVE AND LOGIC (+5V) SUPPLIES

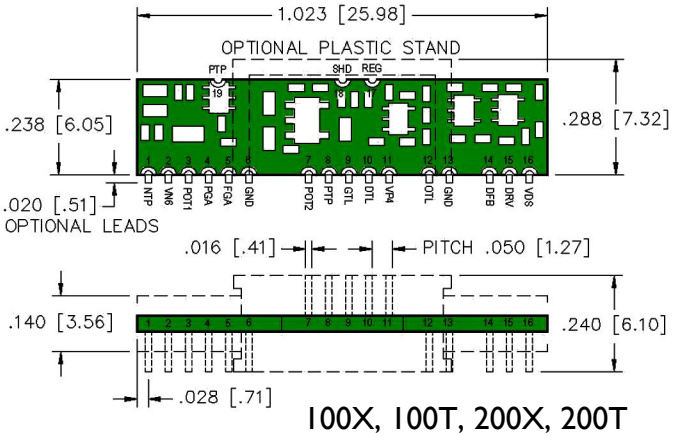
^ Select type X, L, or T
** All models have provisions for adjusting Vgs shutdown threshold to desired level.



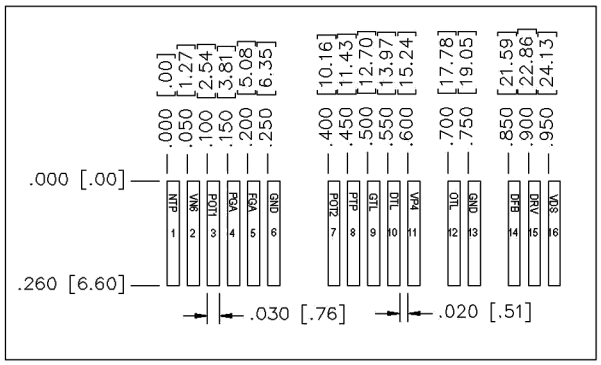
100T, Optional Pins | 100X, Standard | 100L, Low Profile

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

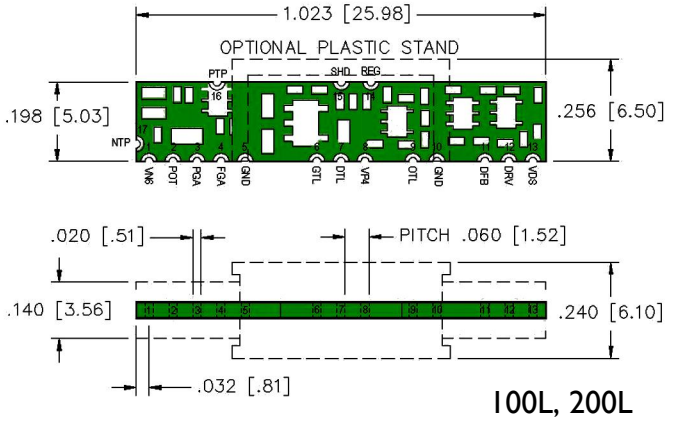
Outline & Land Pattern



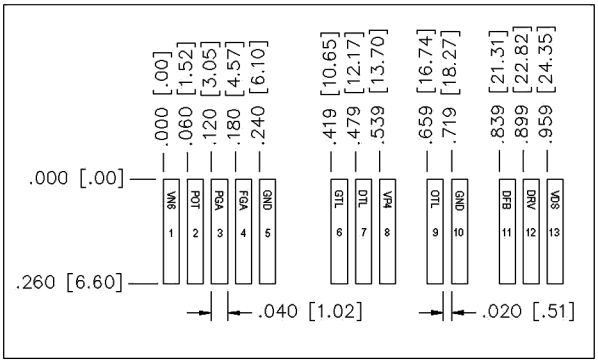
100X, 100T, 200X, 200T



TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED



100L, 200L



TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

Controller I/O Pin Descriptions

WARNING
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

NTP has –4.3V output from a voltage inverter. Tap with >10KΩ trim-pot to establish (-) input to POT pin of the 100 Series only. Otherwise, leave open.

VN6 input is connected to an optional negative supply of > –6V if gate current boost of 100mA is needed for saturated GaN. Internally, there's 30mA. Leave open otherwise.

POT input receives negative voltage for 100 Series or positive voltage for 200 Series. This unity gain buffer provides negative bias to the transistor gate. Temperature-compensation voltage is added here as well.

PGA output produces a square-wave triggered by TTL to pin GTL. It provides gate bias to GaN at a level set from POT pin and down to V_pinchoff established from either the voltage inverter (-4.3V) or from pin VN6.

FGA output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

PTP has +5.0V output from a voltage regulator. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 200 Series only. Otherwise, leave open.

GTL input takes active-low, TTL signal (<4.7V) to control gate switching of the device. It is tied to DTL pin to sequence the gate and drain voltage. This is not used for sub-models. Disconnect from DTL for independent control.

DTL input controls the drain switching end of the transistor. When tied with GTL, the active-low TTL enable switches drain voltage ON and would remain there until gate voltage undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during ramping Vdd up & down.

VP4 input is connected to an optional supply of ≤ +5V. Leave open unless required by sub-models.

OTL output is an active-low TTL drive signal reserved for 300 Series Power CMOS switches. Leave pin open otherwise.

DFB input monitors the presence of drain voltage when the MOS switch is ON. Use if gate switching is desired; otherwise, leave open for sub-models.

DRV output connects to the gate input of MOSFET switch module. Connect to multiple switches with up to 300mA total loads.

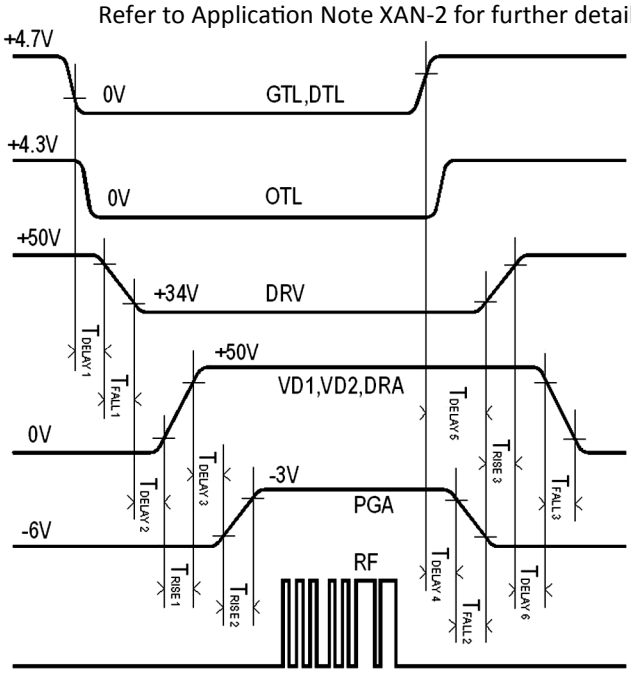
VDS input receives up to +80V from the same supply that powers the GaN.

REG is an auxiliary port of +5.7V from a voltage regulator.

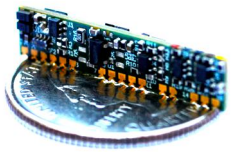
SHD is an auxiliary port for adjusting the gate voltage shutdown threshold. From this node, connect 100KΩ-1MΩ resistor to REG (or PTP) ports for increasing the threshold level, or to GND for decreasing said level.

Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.



200X, 200L, 200T
GaN Controller Module
Power Sequencer, Inverting Analog Input



XSYSTOR

PRODUCT FLYER
July 2017

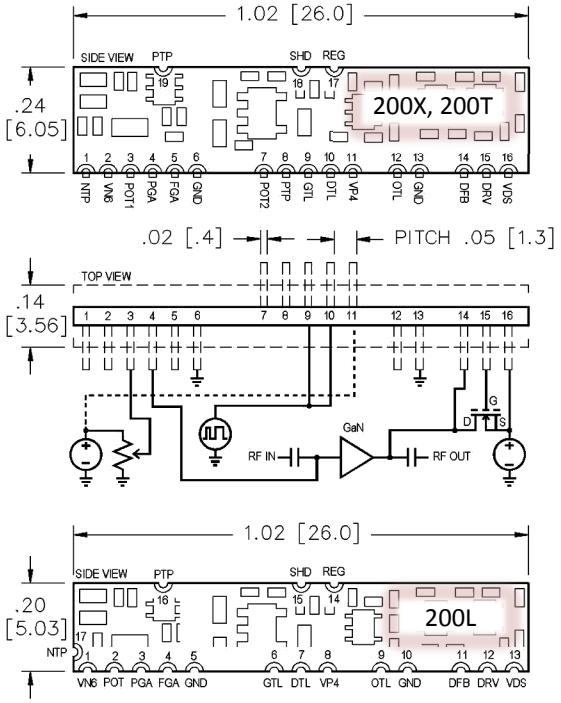
General Description

The 200 Series GaN Controller is capable of operating and protecting all depletion-mode transistors. The inverting analog input accepts positive voltage to produce buffered negative gate bias. It allows 360° board placement with little or no line crossovers in the main board. A single power supply is enough for the 200 to provide dynamic control. Little or no filtering is needed in heavy RF environments. The 200 works seamlessly with 300 and 400 Series MOS switches that have compact footprints for locating near the transistor drain choke. It comes in evaluation boards that are ideal for fast prototyping.

Features

- Protects GaN devices from any power sequence of voltage supplies.
- Internal Negative voltage with 30mA OR external supply for 100mA boost.
- Bias Voltage has Fixed Gate OR Pulsed Gate configuration.
- Simultaneous Gate-Drain sequencing OR Independent Gate/Drain control.
- TTL OR Open Drain (<300mA) output drive for MOSFET switches.
- Temp compensation from local OR remote temp sensor feedback.
- >25dB EMI/RFI Rejection at all I/O ports except from auxiliary taps.
- <500 nsec total delay from V_Logic to V_Drain with applicable switch.
- RoHS* Compliant

Typical Connection Diagram



LABEL	PIN 100X 200X	PIN 100L 200L	DESCRIPTION
NTP	1	17	Aux Negative Voltage Tap
VN6	2	1	Optional Neg (-) Supply
POT	3	2	Gate Voltage Input Adjust
PGA	4	3	Pulsed Gate Voltage Out
FGA	5	4	Fixed Gate Voltage Out
GND	6	5	Ground
POT	7		Connected to Pin 3
PTP	8		Aux Positive Voltage Tap
GTL	9	6	Gate Pulse Logic Enable
DTL	10	7	Drain Pulse Logic Enable
VP4	11	8	Optional Logic (+) Supply
OTL	12	9	Active-Low TTL Driver
GND	13	10	Ground
DFB	14	11	MOS Drain Feedback
DRV	15	12	Open Drain MOS Driver
VDS	16	13	High Voltage Supply
REG	17	14	Aux Regulator Output
SHD	18	15	Aux Gate Threshold Adj
PTP	19	16	Aux Positive Voltage Tap

200T, Optional Pins | 200X, Standard | 200L, Low Profile

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+20 V	+65 V
Supply (-) Voltage, Optional	-6 V	0 V
TTL Voltage Logic High	+3.6 V	+5.0 V
TTL Voltage Logic Low	0 V	+1.4 V
Internal (-) Supply V, Gate Pinchoff	-4.3 V	
Internal (-) Supply I	-30 mA	
Gate Bias Voltage Range	-4.3V	-0.5 V
Out Switch Drive, Open Drain (V)	0 V	+60 V
Out Switch Drive, Open Drain (I)		300 mA
Output ON Prop Delay (T_Delay 1)		120 ns
Output ON Fall Time (T_Fall 1)		120 ns
Output OFF Prop Delay (T_Delay 5)		80 ns
Output OFF Rise Time (T_Rise 3)		80 ns
Gate ON Prop Delay (T_Delay 3)		160 ns
Gate ON Rise Time (T_Rise 2)		60 ns
Gate OFF Prop Delay (T_Delay 4)		160 ns
Gate OFF Fall Time (T_Fall 2)		60 ns
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Open Drain Output with pull-up resistor. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Ordering Information

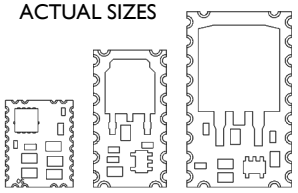
Model ^	
200_02R6 200_02R0 200_01R4 200_00R8	UNIVERSAL GaN CONTROLLER: POSITIVE ANALOG INPUT, SINGLE DC SUPPLY, VGS SHUTDOWN AT -2.6V THRU -0.8V**. INDEPENDENT OR SEQUENTIAL SWITCHING OF DRAIN AND GATE
220_02R6 220_02R0 220_01R4 220_00R8	DRAIN CONTROLLER: 200_ WITH NO GATE SWITCHING CAPABILITY
224_02R6 224_02R0 224_01R4 224_00R8	BASIC SEQUENCER: 200_ WITH NO GATE SWITCHING, NO INTERNAL NEGATIVE AND LOGIC (+5V) SUPPLIES

^ Select type X, L, or T
** All models have provisions for adjusting Vgs shutdown threshold to desired level. See XAN-2 app note.

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

300PNC Series
CMOS Power Switch
For Ultra-High Speed Pulsed GaN Systems

ACTUAL SIZES



XSYSTOR

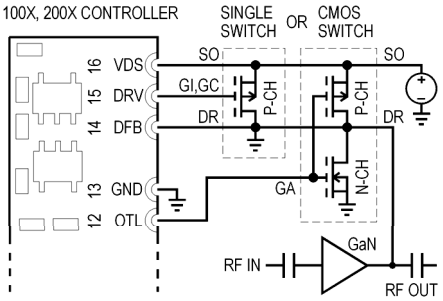
PRODUCT FLYER
July 2017

General Description

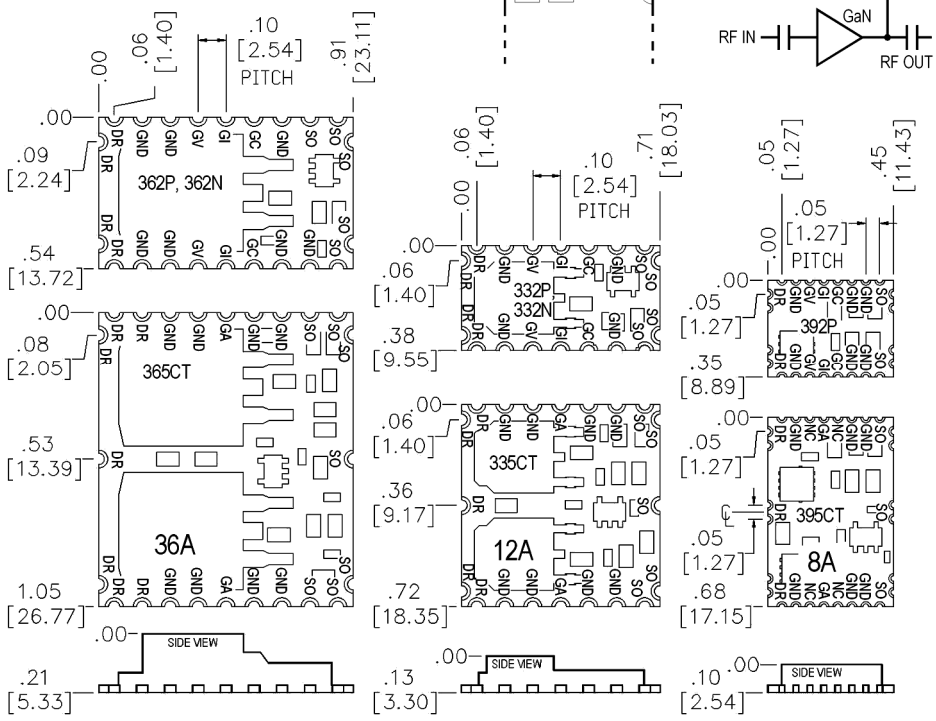
The Complementary MOSFET Switches of the 300PNC Series offers high-performance with ease of integration. Designed for Pulsed-mode, they have clocked speeds of <<200nsec for Rise and Fall Times. Its compact footprint allows direct placement near the RF Choke of the GaN drain. The MOSFETs on board are rated up to 36A Peak, and are safe from 3X the momentary current surges. With modular design introducing higher thermal resistance, the average current ceiling should be specified at half the rating. These switches are ideally driven by the 100 or 200 Series Controllers.

Features

- Rated for 100V
- Ultra-low Rds ON
- Operation up to 125°C, with derated voltage and current.
- Total switching times of <500 nsec when used together with 100 or 200 Series Controllers.
- Complementary P & N-channel MOS achieve Rise & Fall Times of <<200ns.
- Identical I/O Ports at opposite sides.
- RoHS* Compliant



Typical Connection Diagram



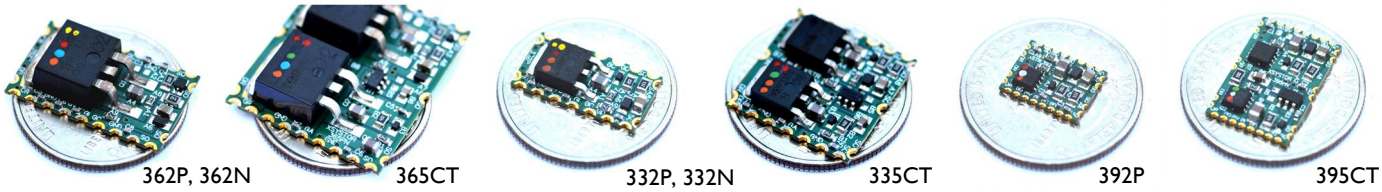
Specification Snapshot

Parameter	Min	Max
Source Voltage (SO)	+20 V	+65 V
Drain Voltage (DR)	+20 V	+65 V
Gate Voltage (GI) Open Drain	0 V	+20 V
Gate Voltage (GA) TTL High	+2.0 V	+5.0 V
Gate Voltage (GA) TTL Low	0 V	+0.8 V
Rds ON (12A Peak Switch)		0.22 Ω
Rds ON (36A Peak Switch)		0.07 Ω
Turn-ON Prop Delay (T_Delay 2)		100 ns
Turn-ON Rise Time (T_Rise 1)		70 ns
Turn-OFF Prop Delay (T_Delay 6) Complementary Pair Only		150 ns
Turn-OFF Fall Time (T_Fall 3)		100 ns
Period for Pulsed Signals		5 ms
Duty Cycle for Pulsed Signals		20 %
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of Drive Signal from Controller to 10% of Drain Voltage Output with load of 1KΩ. Faster speeds occur with decreased load resistance. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Ordering Information

332P0000	12A PEAK, 6A AVG MAX, PULSED
332N0000	COMPLEMENTS 332P ONLY
335CT000	12A PEAK, 6A AVG MAX, PULSED
362P0000	36A PEAK, 16A AVG MAX, PULSED
362N0000	COMPLEMENTS 362P ONLY
365CT000	36A PEAK, 16A AVG MAX, PULSED
392P0000	8A PEAK, 4A AVG MAX, PULSED
395CT000	8A PEAK, 4A AVG MAX, PULSED SWITCH POWER CMOS, TTL DRIVE

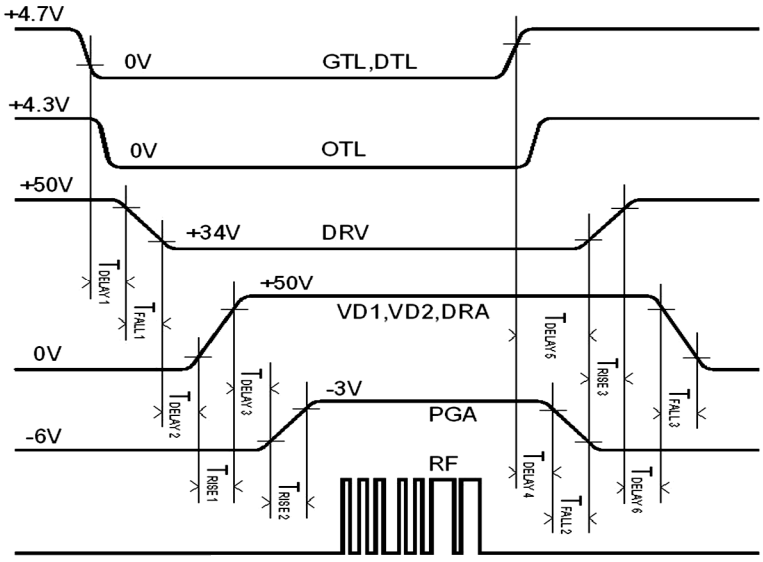


11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

Switch I/O Pin Descriptions

GA is a gate input that receive TTL signals only from OTL output of Controller. Extra caution should be taken when handling TTL signals to prevent damage.
GI is a gate input connected to DRV of Controller. These ports are interconnected for P & N-Chan Pairs. For a Single Switch module GI is tied to GC.
GC is interconnected to like ports for P & N-Chan Pairs. It is only tied to GI for a Single Switch configuration.
GV is interconnected to like ports for P & N-Chan Pairs. Otherwise, leave port open for a Single Switch configuration.
DR are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
SO are source inputs that take up to +65V supply. Larger storage capacitance are attached here.
NC is no connection.

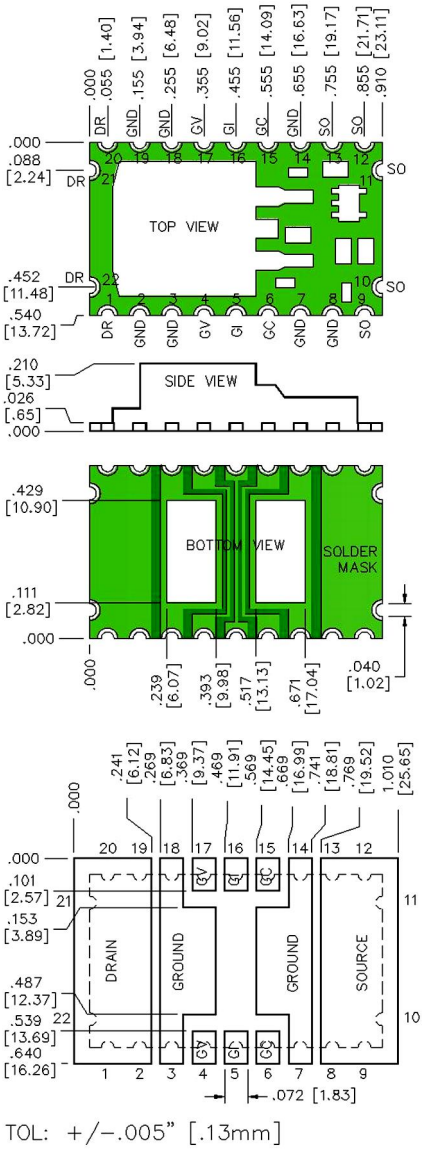
Typical Timing Diagrams



Refer to Application Note XAN-2 for further details.

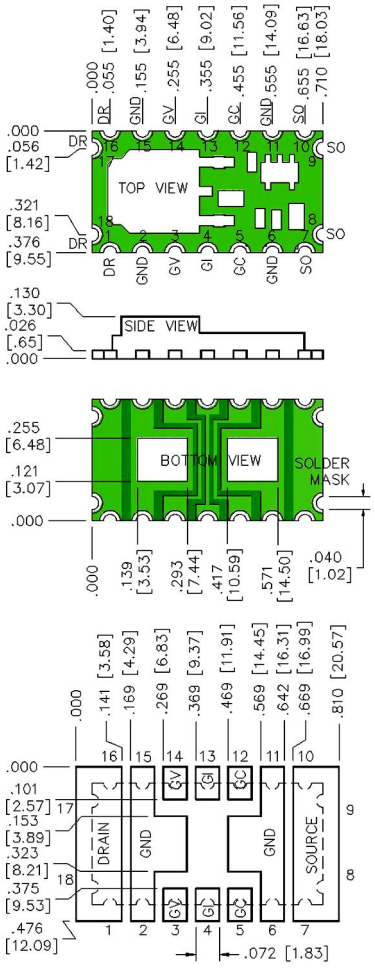
Outline & Land Pattern

362P, 362N



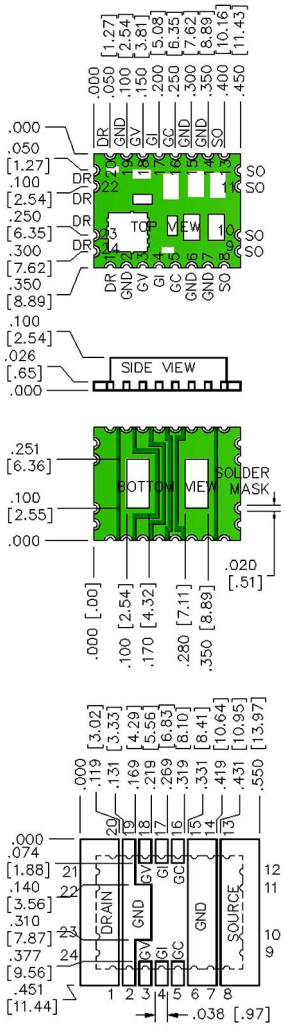
TOL: +/−.005" [.13mm]

332P, 332N



TOL: +/−.005" [.13mm]

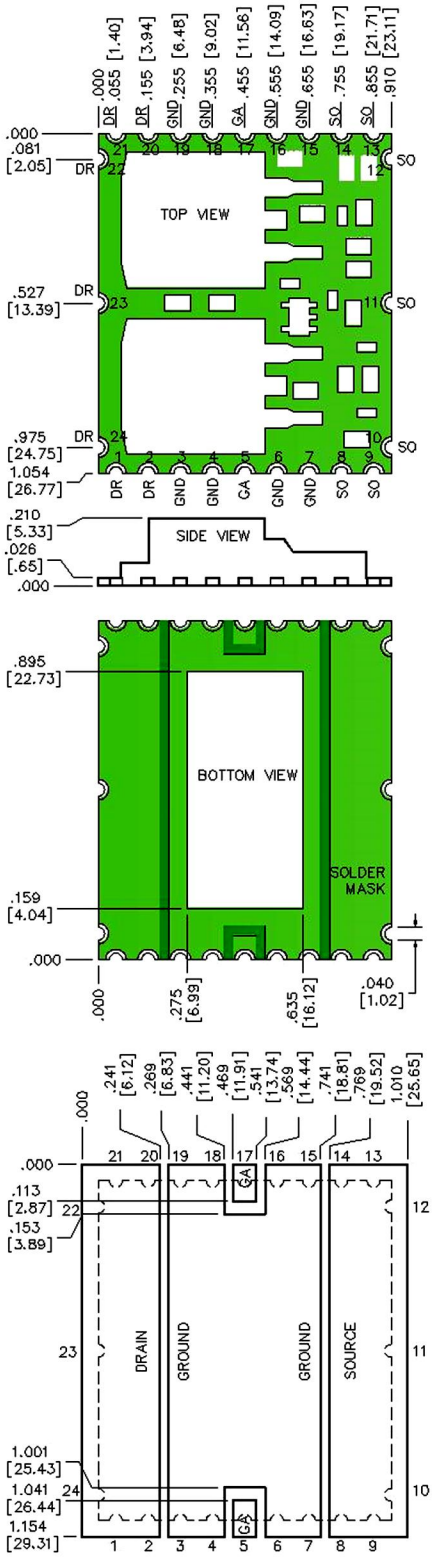
392P



TOL: +/−.005" [.13mm]

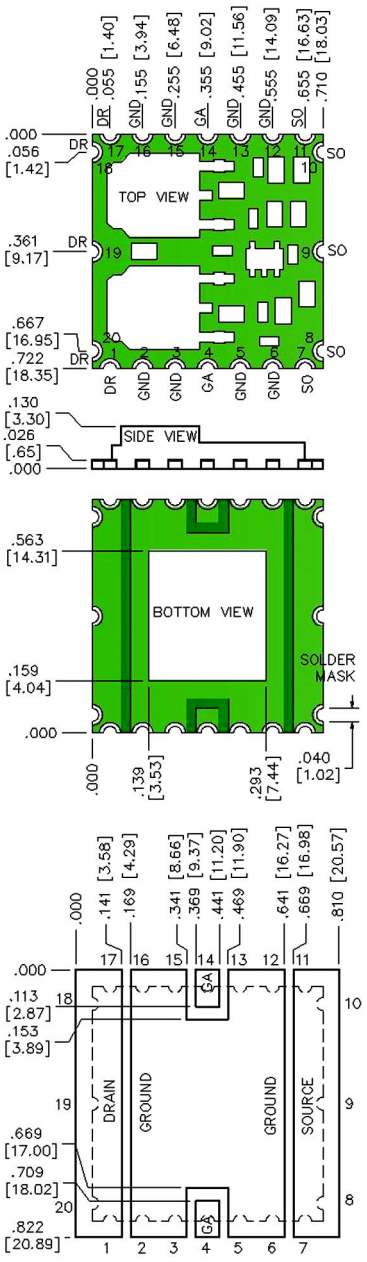
Outline & Land Pattern (continued)

365C



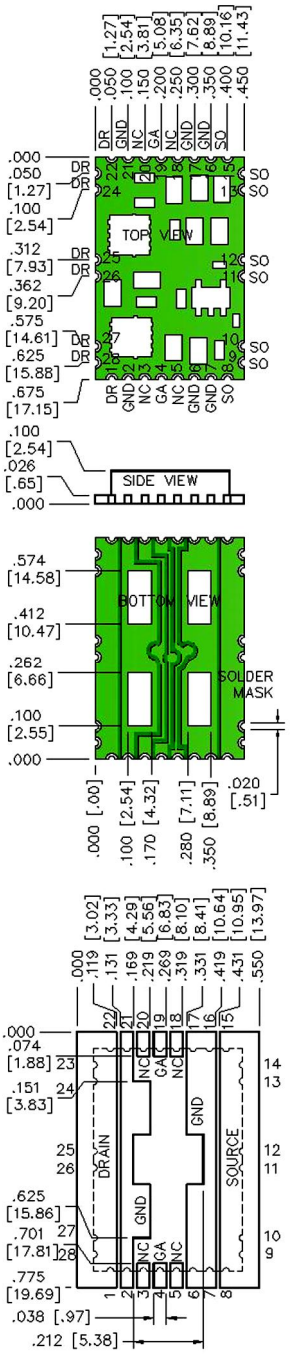
TOL: +/−.005" [.13mm]

335C



TOL: +/−.005" [.13mm]

395C

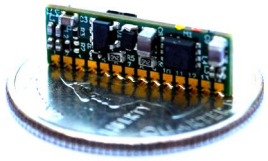


TOL: +/−.005" [.13mm]

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

400X, 400L, 400T
Dual MOSFET Switch Mini Module
From CW to Ultra-High Speed Pulsed Systems



XSYSTOR

PRODUCT FLYER
July 2017

General Description

The 400 Series Dual MOSFET Mini Switch offers high-performance with ease of integration. Like the 100/200 Series, the tiny footprint allows direct placement near the RF chokes of two or more GaN device. While each MOS switch has continuous 8A rating, the higher thermal resistance of the module limits the average current to 4A. These Switches are driven by the 100 or 200 Series Controllers. They come in Dual MOS for CW operation, or Complementary MOS for Pulsed-mode requiring <<200nsec Rise and Fall Times.

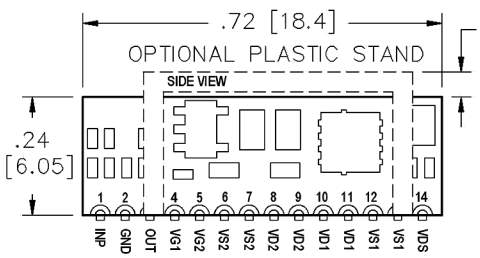
Features

- Rated for 100V
- Ultra-low Rds ON
- Operation up to 125°C, with derated voltage and current.
- Ideal for 2-Stage Amps, Balanced Amps, and for Single GaN with critical rise and fall time requirements.
- Total switching times of <500 nsec when used together with 100 or 200 Series GaN Controllers.
- RoHS* Compliant

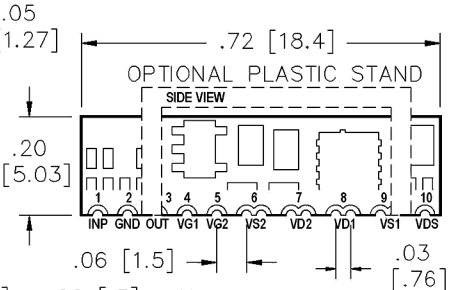
INP	INPUT FROM CONTROLLER DRIVER
GND	GROUND
OUT	OUTPUT TO MOSFET GATES
VG1,VD1,VS1	GATE, DRAIN, SOURCE OF MOS #1
VG2,VD2,VS2	GATE, DRAIN, SOURCE OF MOS #2
VDS	POSITIVE VOLTAGE SUPPLY

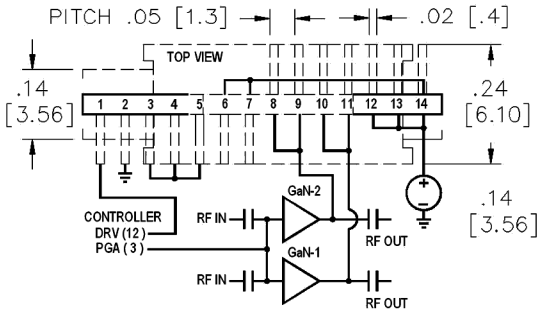
Typical Connection Diagrams

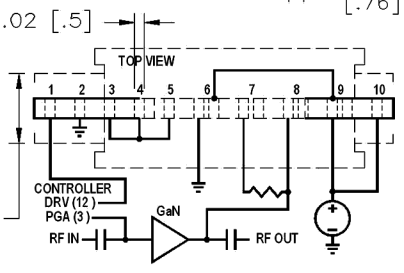
400X, 400T



400L



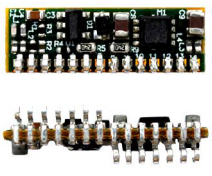




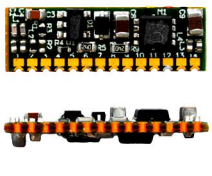
Dual Switch

Complementary MOS

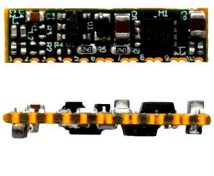
400T



400X



400L



Specification Snapshot

Parameter	Min	Max
Source Voltage, MOS	+20 V	+65 V
Gate Voltage, MOS	0 V	+20 V
Drain Voltage, MOS	+20 V	+65 V
Drain Current, Peak		8 A
Drain Current, Average, CW		4 A
Rds ON		0.18 Ω
Turn-ON Prop Delay (T_Delay 2)		100 ns
Turn-ON Rise Time (T_Rise 1)		70 ns
Turn-OFF Prop Delay (T_Delay 6) Complementary Pair Only		150 ns
Turn-OFF Fall Time (T_Fall 3)		100 ns
Period for Pulsed Signals		5 ms
Duty Cycle for Pulsed Signals		20 %
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of Drive Signal from Controller to 10% of Drain Voltage Output with load of 1KΩ. Faster speeds occur with decreased load resistance. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Ordering Information

410X0000 410L0000 410T0000	8A PEAK, 4A AVG MAX, DUAL P-CHAN MOSFET SWITCH, CW
420X0000 420L0000 420T0000	8A PEAK, 4A AVG MAX, DUAL P-CHAN MOSFET SWITCH, PULSED MODE
430XT000 430LT000 430TT000	8A PEAK, 4A AVG MAX, COMPLEMENTARY MOS SWITCH PAIR, PULSED, TTL ENABLE

X = STANDARD

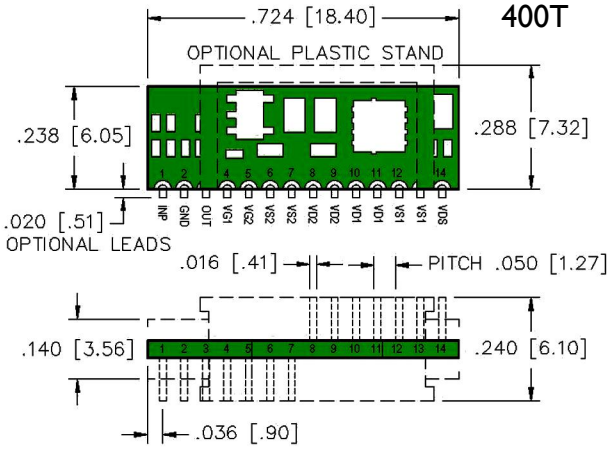
L = LOW PROFILE

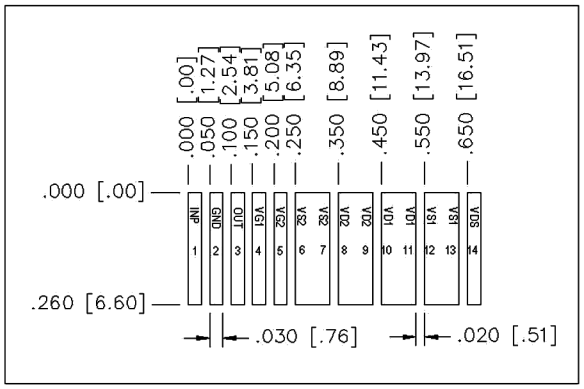
T = OPT PINS AT 0.05" [1.3mm] PITCH

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

Outline & Land Pattern

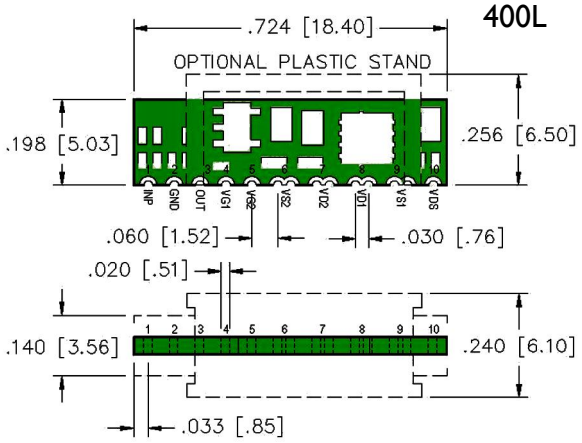
400X
400T

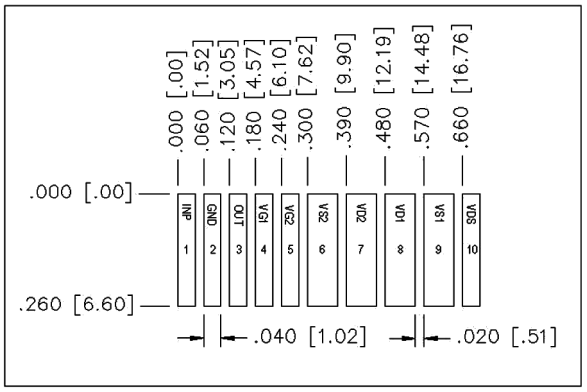




TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

400L

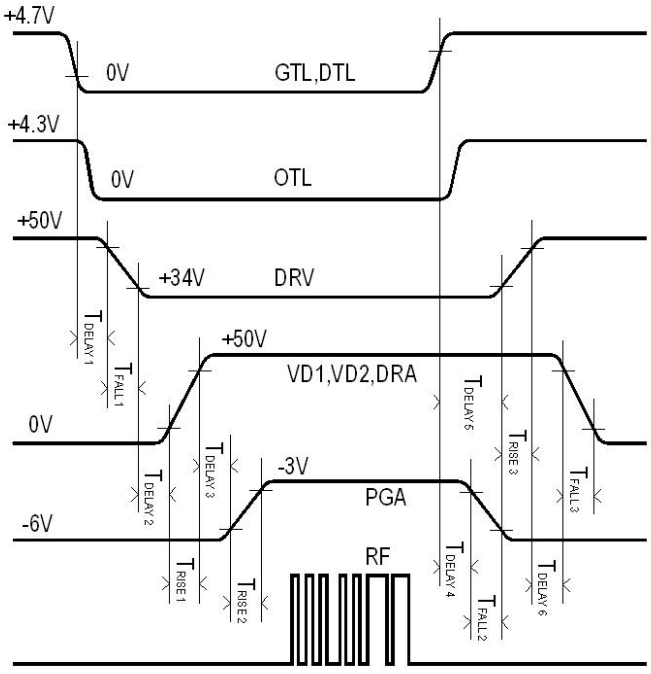




TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.



Switch I/O Pin Descriptions

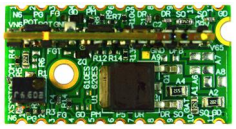
INP input connects directly to the Controller DRV output for dual-switch configuration. For complementary MOS (push-pull), it connects to OTL.
OUT is a low-side driver output which connects to MOSFET gates VG1 and VG2.
VG1, VG2 are gate inputs that receive signals from DRV output of Controller. For a general purpose switch like the 410, the DRV pin can be tied to VG1 & VG2, while bypassing INP & OUT pins.
VD1, VD2, DRA are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
VS1, VS2, SOU are source inputs that take up to +65V supply. Larger storage capacitance are attached here.

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

600E Series
Drop-In Evaluation Board
Controller Plus Switch for Fast Prototyping

ACTUAL SIZE



ALL-IN-ONE MODULE

XSYSTOR

PRODUCT FLYER
July 2017

General Description

The 600E Series Eval Boards are general purpose and complete solutions to operate most GaN devices. The on-board Controller and Switch provide bias adjustment, power sequence, and protection. Demonstrating device performance is as easy as dropping them in on GaN eval boards, sub-assemblies, and test apparatus. The tiny modules can be mounted on either metal surfaces or on printed circuit boards. Identical connections at opposite sides of the module simplifies placement for fast-prototyping. Drop it, set it, and forget it.

Features

Controller:

- Choice of 100L or 200L. Single power supply. Independent or Sequential Drain and Gate Switching.
- Default TTL control signal is Active-Low. Active-High control is available upon request.
- On-board potentiometer for fine gate bias adjustment.

Switch:

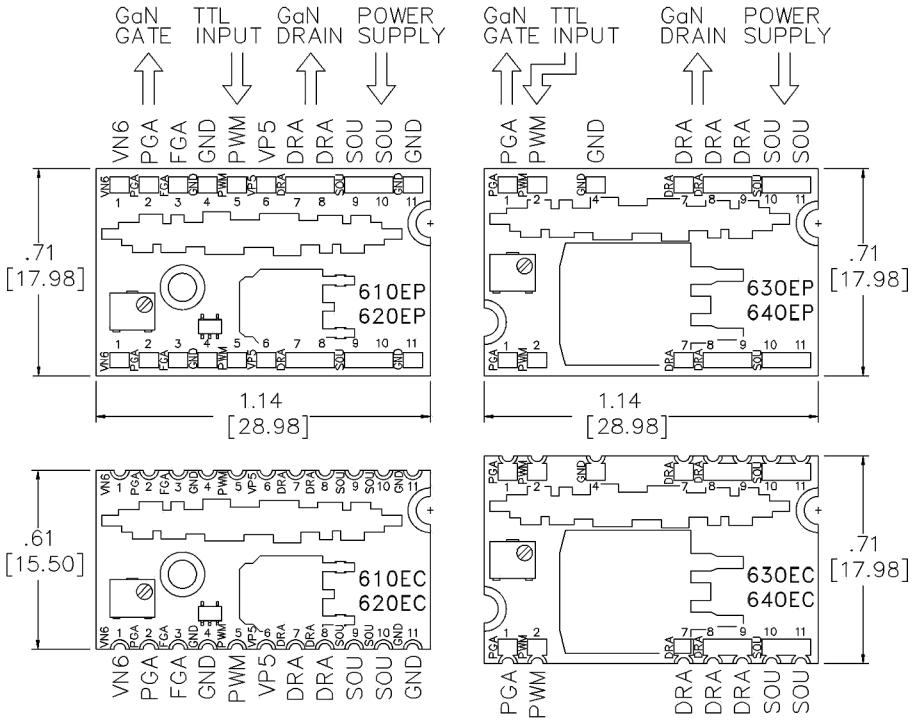
- Rated for 100V, Ultra-low Rds ON, Operation up to 150°C, with derated voltage and current.
- Utilize units at less than half the peak current for best results.

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+20 V	+65 V
Supply (-) Voltage, Optional	-6 V	0 V
Internal (-) Supply V, Gate Pinchoff	-4.3 V	
Internal (-) Supply I	-30 mA	
Gate Bias Voltage Range	-4.3V	-0.5 V
Gate Threshold Shutdown Range	-3.0 V	-0.5 V
TTL Voltage Logic High	+3.6 V	+5.0 V
TTL Voltage Logic Low	0 V	+1.4 V
Avg Current from MOS peak rating		50%
MOS Rds ON (36A to 12A)	0.07 Ω	0.22 Ω
Drain ON Prop Delay, loaded		300 ns
Drain ON Rise Time, loaded		200 ns
Drain OFF Prop Delay, loaded		5 us
Drain OFF Fall Time, loaded		4 us
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Drain Voltage with device load . Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Eval Board Configurations



TYPE-EP typically mounts on metal surfaces, while TYPE-EC on printed circuit boards.

610EP, 620EP | 610EC, 620EC | 630EP, 640EP | 630EC, 640EC

Ordering Information

Content Type	Mount Type	Shut-down Preset	TTL Enable	Misc Type
610	EP	2R6	AL	20
620	EC	2R0	AH	50
630		1R4		PW
640		0R8		

Example: 610EP2R6AL20

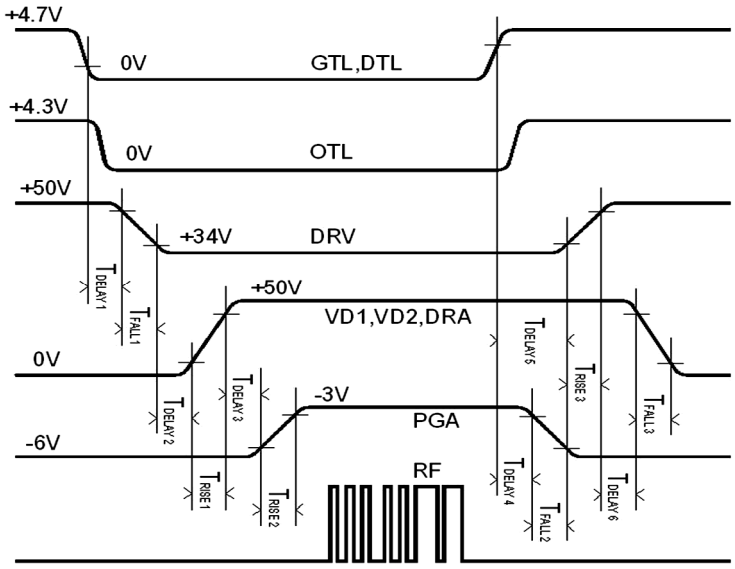
***610**_100L Controller & 6A Avg (12A Peak) Switch*
***620**_200L Controller & 6A Avg (12A Peak) Switch*
***630**_100L Controller & 16A Avg (36A Peak) Switch*
***640**_200L Controller & 16A Avg (36A Peak) Switch*
***EP**_Mounts on Metal. Pads on top, Ground at bottom*
***EC**_Mounts on PCB. Castellated ports for solder reflow*
***2R6...0R8**_Gate Threshold Shutdown Presets at –2.6V, -2.0V,-1.4V,-0.8V. Has provisions for fine adjustment using one resistor. Refer to XAN-2 application note*
***AL**_Active-Low (0V) TTL. Default for all Controllers*
***AH**_Active-High (<5V) TTL for Gate/Drain Voltage ON*
***20**_Supply range of +20V to +36V. General purpose*
***50**_Supply range of +36V to +65V. General purpose*
***PW**_Operates at PW < 500usec, Duty < 20%. Supply: +20V to +65V*

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

I/O Pin Descriptions

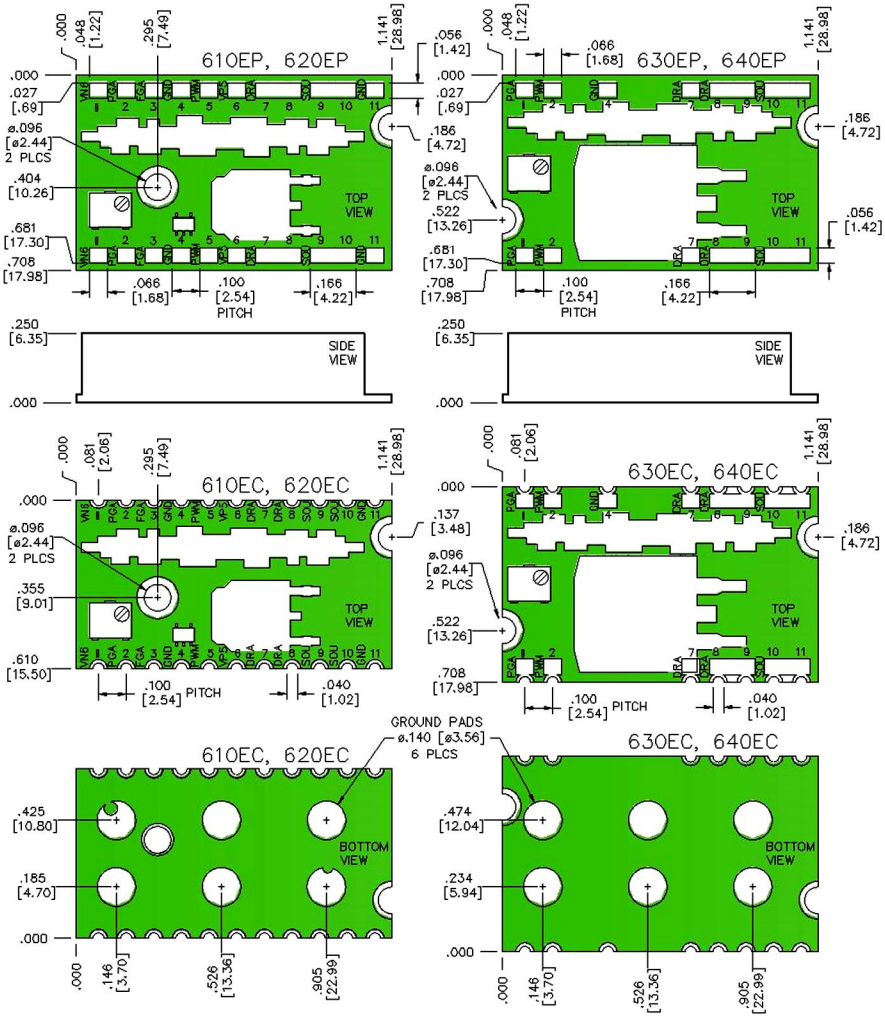
610 620 PIN	630 640 PIN	LABEL	DESCRIPTION
1		VN6	Optional Neg Voltage Input (-6V min) for Gate Current Boost. Leave Open.
2	1	PGA	Neg Pulsed Voltage Output to Transistor Gate
3		FGA	Neg Fixed Voltage Output to Transistor Gate
4	4	GND	Ground
5	2	PWM	TTL/PWM Signal Input to Switch Transistor.
6		VP5	Optional Positive Voltage Input (+5V max). Leave Open.
7,8	7,8,9	DRA	High Voltage Output to Transistor Drain. Avoid excess wires or lines to minimize inductive parasitic. Max capacitive load is 500pF for optimum switching speed
9,10	10,11	SOU	High Voltage Power Supply Input. Connect high value storage capacitors here.
11		GND	Ground

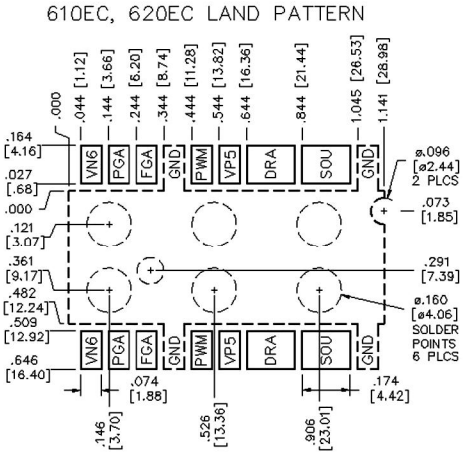
Typical Timing Diagrams

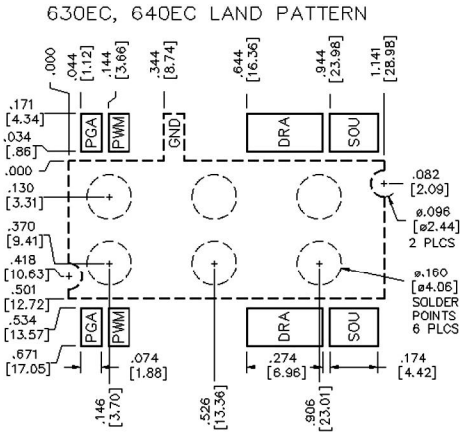


- Refer to Application Note XAN-2 for further details.

Outline & Land Pattern







TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED

Model Number Color Code

0	1	2	3	4	5	6	7	8	9

700E Series
Evaluation Board, Controller & Power CMOS Switch
Ultra-High Speed, High Power, Removable Modules

XSYSTOR

PRODUCT FLYER
July 2017

General Description

The 700 Series Evaluation Board is a complete solution with a Controller and Power CMOS Switch. They are used for demonstrating GaN in Pulsed applications that require both Rise and Fall Times to clock faster than <<200 nsec and Propagation Times of <<200 nsec. The modules are removable for real-world applications when the evaluation phase is complete. Bias adjustment, power sequence, and protection are provided when interfaced to GaN Eval/Test board with minimal inductive & capacitive loads.

Features

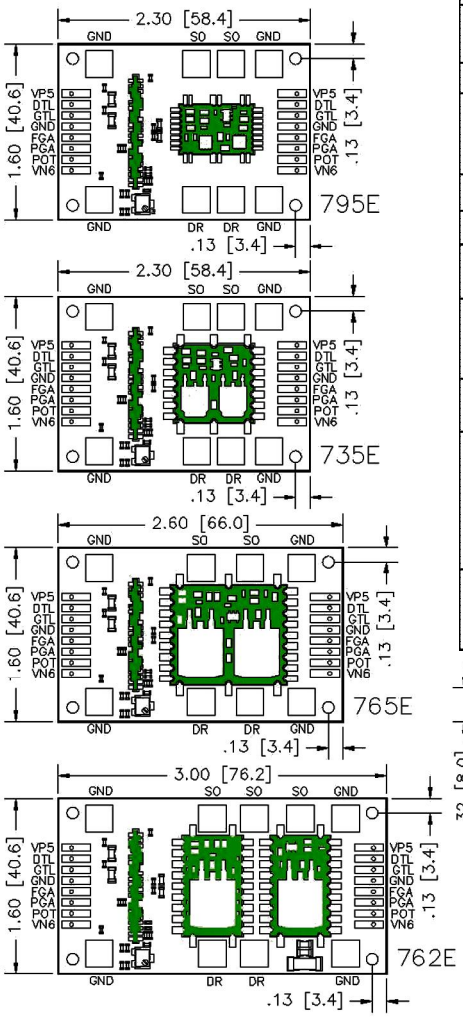
- Large mounting pads and pitched holes are ideal for banana plug receptacles, headers, & wire jumpers.
- Switch is rated for 100V, Ultra-low Rds ON, Operation up to 150°C, with derated voltage and current.
- Utilize units at half the rated current for best results.
- Controller: Choice of 100L or 200L. Single power supply. Independent or Sequential Drain and Gate Switching.
- On-board potentiometer for fine gate bias adjustment.

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+20 V	+65 V
Supply (-) Voltage, Optional	-6 V	0 V
Internal (-) Supply V, Gate Pinchoff	-4.3 V	
Internal (-) Supply I	-30 mA	
Gate Bias Voltage Range	-4.3V	-0.5 V
Gate Threshold Shutdown Range	-3.0 V	-1.0V
TTL Voltage Logic High	+3.6 V	+5.0 V
TTL Voltage Logic Low	0 V	+1.4 V
Avg Current from MOS peak rating		50%
MOS Rds ON (40A to 14A)	0.07 Ω	0.22 Ω
Drain ON Propagation Delay, cmos		150ns
Drain ON Rise Time, cmos		200ns
Drain OFF Propagation Delay, cmos		250ns
Drain OFF Fall Time, cmos		200ns
Soldering Temp (10 sec)		+195°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Drain Voltage with device load . Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Eval Board Configurations



I/O Pin Descriptions

LABEL	DESCRIPTION
VP5	Optional +5V max Supply Voltage. Leave open
DTL	Drain Switch Enable TTL Input
GTL	Gate Switch Enable TTL Input. Usually tied to DTL. Disconnect for independent switching
GND	Ground
FGA	Fixed Bias Voltage to Transistor Gate
PGA	Pulsed Bias Voltage to Transistor Gate, as enabled by GTL
POT	Analog Bias Voltage Input. Leave open when trim-pot is utilized. Temp-comp input voltage
VN6	Optional -6V max Supply Voltage for Gate bias current boost. Leave open
DR	High Voltage Output to Transistor Drain. Avoid excess wires or lines to minimize inductive parasitic. Max capacitive load is 500pF for optimum switching speed.
SO	High Voltage Input Source up to +65VDC. Connect high value storage capacitors here

Ordering Information

MODEL * ^	MODULE CONTENT ~ °
732E_2R6	(1) 100X + 332P & 332N
732E_2R0	(2) 200X + 332P & 332N
732E_1R4	12A peak, 6A avg max
735E_2R6	(1) 100X + 335CT
735E_2R0	(2) 200X + 335CT
735E_1R4	12A peak, 6A avg max
762E_2R6	(1) 100X + 362P & 362N
762E_2R0	(2) 200X + 362P & 362N
762E_1R4	36A peak, 16A avg max
763E_2R6	(1) 100X + 2 x 362P
763E_2R0	(2) 200X + 2 x 362P
763E_1R4	36A peak, 16A avg max
765E_2R6	(1) 100X + 365CT
765E_2R0	(2) 200X + 365CT
765E_1R4	36A peak, 16A avg max
792E_2R6	(1) 100X + 392P
792E_2R0	(2) 200X + 392P
792E_1R4	8A peak, 4A avg max
795E_2R6	(1) 100X + 395CT
795E_2R0	(2) 200X + 395CT
795E_1R4	8A peak, 4A avg max

* Select (1) 100X or (2) 200X Controller
^ All models have provisions for fine adjusting Vgs shutdown threshold to desired level. Refer to 100 or 200 Controller Spec Sheets for more information
~ Select preset shutdown at Vgs = -2.6V, -2.0V, or -1.4V
° Remove modules at solder melting point of <195°C

11331 E. 183rd STREET # 209, CERRITOS CA 90703, PHONE/FAX: 888-968-7755, EMAIL: SALES@XSYSTOR.COM, WWW.XSYSTOR.COM

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

1. Background

Designers of RF circuits face diminishing returns when choosing GaN HEMTs for their next generation power products. The superior attributes of GaN over the established realm of LDMOS and Bipolar loses some of its luster when the biasing difficulty is factored in for depletion mode devices. Putting smart circuitry to ensure that GaN HEMTs are safe and unconditionally stable becomes a daunting task to begin with, let alone dealing with the high cost of accommodating several IC components to share space fraught with EMI and RFI. The situation demands a multilayered PCB solution.

But the sensible solution is to let the PCB remain as a 2-layer RF laminate and dropping-in tiny controller and switch modules that take advantage of tight spaces and simple printed line interconnects. A significant reduction of cost and complexity will be apparent in "black box" documentation, parts procurement, assembly, and test.

2. Controller I/O Table

Before we start interconnecting, lets become familiar with the module inputs and outputs. From the table below, reference each label, pin, and description to the schematic and outline drawings in coming pages . Refer to the Product Flyers for more details.

LABEL	PIN 100X 200X	PIN 100L 200L	DESCRIPTION
NTP	1	17	Aux Negative Voltage Tap
VN6	2	1	Optional Neg (-) Supply
POT	3	2	Gate Voltage Input Adjust
PGA	4	3	Pulsed Gate Voltage Out
FGA	5	4	Fixed Gate Voltage Out
GND	6	5	Ground
POT	7		Connected to Pin 3
PTP	8		Aux Positive Voltage Tap
GTL	9	6	Gate Pulse Logic Enable
DTL	10	7	Drain Pulse Logic Enable
VP4	11	8	Optional Logic (+) Supply
OTL	12	9	Active-Low TTL Driver
GND	13	10	Ground
DFB	14	11	MOS Drain Feedback
DRV	15	12	Open Drain MOS Driver
VDS	16	13	High Voltage Supply
REG	17	14	Aux Regulator Output
SHD	18	15	Aux Gate Threshold Adj
PTP	19	16	Aux Positive Voltage Tap

3. Controller I/O Pin Descriptions

WARNING
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

NTP has –4.3V output from a voltage inverter. Tap with >10KΩ trim-pot to establish (-) input to POT pin of the 100 Series only. Otherwise, leave open.

VN6 input is connected to an optional negative supply of > –6V if gate current boost of 100mA is needed for saturated GaN. Internally, there's 30mA. Leave open otherwise.

POT input receives negative voltage for 100 Series or positive voltage for 200 Series. This unity gain buffer provides negative bias to the transistor gate. Temperature-compensation voltage is added here as well.

PGA output produces a square-wave triggered by TTL to pin GTL. It provides gate bias to GaN at a level set from POT pin and down to V_pinchoff established from either the voltage inverter (-4.3V) or from pin VN6.

FGA output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

PTP has +5.0V output from a voltage regulator. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 200 Series only. Otherwise, leave open.

GTL input takes active-low, TTL signal (<4.7V) to control gate switching of the device. It is tied to DTL pin to sequence the gate and drain voltage. This is not used for sub-models. Disconnect from DTL for independent control.

DTL input controls the drain switching end of the transistor. When tied with GTL, the active-low TTL enable switches drain voltage ON and would remain there until gate voltage undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during ramping Vdd up & down.

VP4 input is connected to an optional supply of ≤ +5V. Leave open unless required by sub-models.

OTL output is an active-low TTL drive signal reserved for 300 Series Power CMOS switches. Leave pin open otherwise.

DFB input monitors the presence of drain voltage when the MOS switch is ON. Use if gate switching is desired; otherwise, leave open for sub-models.

DRV output connects to the gate input of MOSFET switch module. Connect to multiple switches with up to 300mA total loads.

VDS input receives from the same supply that powers the GaN.

REG is an auxiliary port of +5.7V from a voltage regulator.

SHD is an auxiliary port for adjusting the gate voltage shutdown threshold. From this node, connect 100KΩ-1MΩ resistor to REG (or PTP) ports for increasing the threshold level, or to GND for decreasing said level.

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

3. Switch I/O Pin Descriptions

I/O TABLE: 400 SERIES	
INP	INPUT FROM CONTROLLER DRIVER
GND	GROUND
OUT	OUTPUT TO MOSFET GATES
VG1,VD1,VS1	GATE, DRAIN, SOURCE OF MOS #1
VG2,VD2,VS2	GATE, DRAIN, SOURCE OF MOS #2
VDS	POSITIVE VOLTAGE SUPPLY

I/O TABLE: 300 PNC SERIES	
DRA	DRAIN
GND	GROUND
G A	GATE IN, CMOS
G I	GATE IN
G C	GATE CAP
G V	GATE 15V
SOU	SOURCE

INP input connects directly to the Controller DRV output.
OUT is a low-side driver output which connects to MOSFET gates VG1 and VG2.
VG1, VG2, GA are gate inputs that receive signals from DRV or OTL outputs of the Controller. For a general purpose switch like the 410, the DRV pin can be tied to VG1 & VG2, while bypassing INP & OUT pins.
GI, GC, GV are interdependent gate inputs that connect matching pins of complementary switch pairs. Only when using a single switch that GI and GC are tied together.
VD1, VD2, DRA are drain outputs that connect to the GaN device drain. Switching speeds may be compromised when bypass capacitance exceeds 500pF.
VS1, VS2, SOU are source inputs that take up to +65V supply. Larger storage capacitance are attached here.

4. Functional Diagrams

The following circuit diagrams are just a sampling of the numerous configurations the Controller and Switch can work for your application. The base model Controller like the 100 & 200 are the most universal, meaning they have the most features that can be utilized or ignored. Sub-categories of these are budget models that have certain features removed for a simpler, more specific application.

The primary function of the Controller is a bias sequencer. Gate voltage is delivered to device before drain voltage and remains there until the drain side has no more potential. The Switch stands ready for shutdown when GaN safety is compromised. The secondary function is to control the Switch with PWM/TTL signals and deliver high-voltage/high-current/high-speed square pulses to power-up or modulate the RF device. Drain switching can also be left in the ON-state indefinitely by grounding the pulse enable pin. The tertiary function is the ability to control gate voltage switching independently or slave to drain switching. In addition to added stability mentioned previously, pulse-shaping can be introduced with gate control.

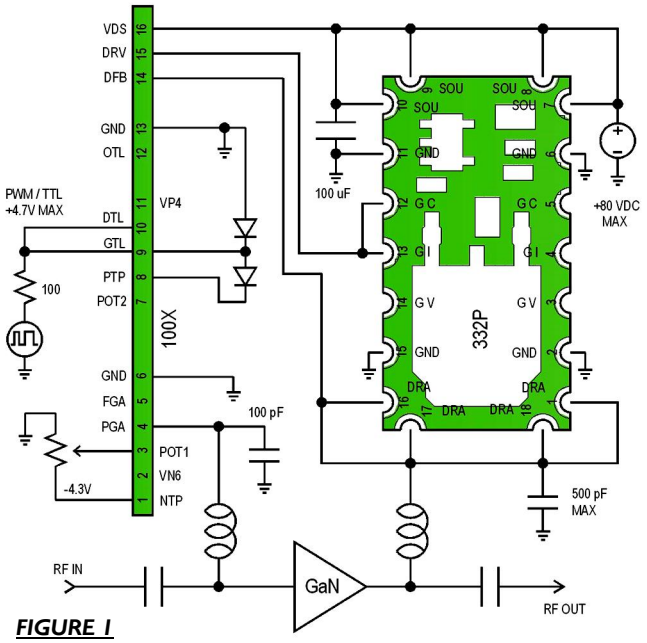


FIGURE 1

The circuit in Figure 1 uses a non-inverting controller, 100X and paired with a pulsed switch 332P. A single power source is used; therefore, gate current from internal inverter is limited to 30mA available to GaN. In cases where negative supply is accessible, the potentiometer should give relief to the negative tap, NTP. There are general purpose switching diodes that protect the TTL inputs from transients, signal level changes, and negative sources.

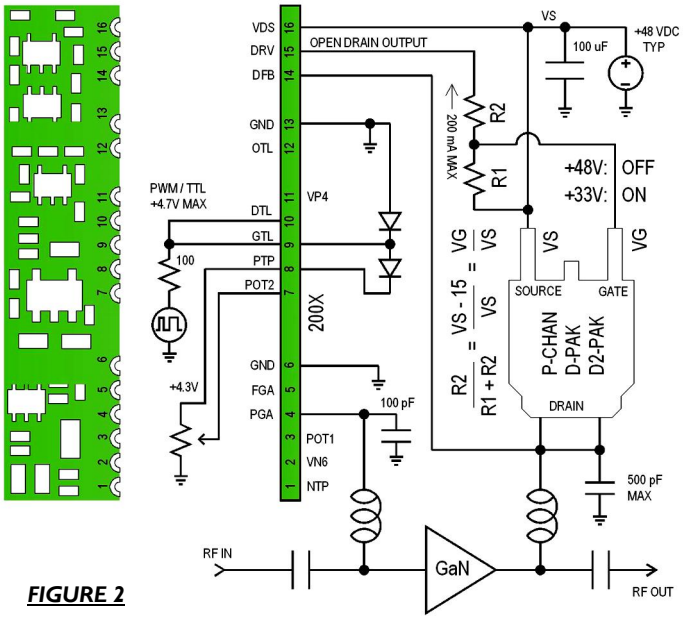


FIGURE 2

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

The circuit in Figure 2 has a 200X inverting controller driving a general purpose PMOS transistor. The switch operating in CW is typically used for pulse periods beyond 5msec. The value and rating of the pair of resistors R1 & R2 depend on how much current to draw for increased switching speed. The DRV output of the controller should not exceed 100mA of sink current. A potentiometer taps into the positive auxiliary port to generate an operating gate voltage. This combination also relies on a single power source.

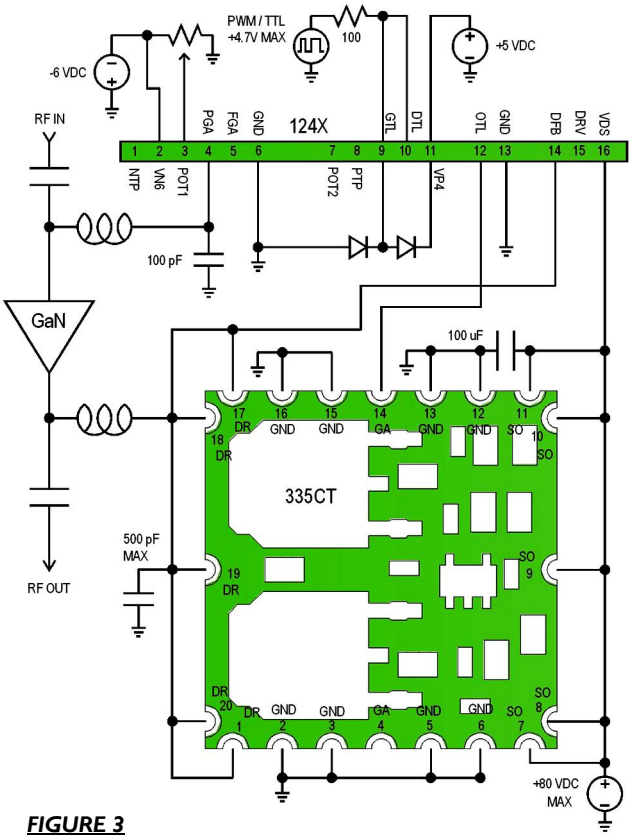


FIGURE 3

A Complementary MOS (push-pull) switch is illustrated in Figure 3 with a power CMOS 335CT controlled by a basic sequencer 124X. The advantage of a P & N-Chan pair is mainly to "pull-down" the drain voltage from say 50V down to 0V as quickly as possible with no significant decay normally seen with single MOSFET switches. Structured rise and fall times (<<200nsec) make for a well controlled spectral characteristic. The negative supply also provides boost current to the gate of a GaN transistor in saturation.

A 220X controller with no gate switching feature drives a 410X dual switch in CW, as shown in Figure 4. The objective is that one switch controls the high-power, final amp stage, while the other switch handle two driver amp stages. While it's possible to tie the gates of three transistors from one controller, their gate impedances may adversely affect their individual bias points and cause current imbalances. It's better practice to buffer each device gate with voltage follower or adjustable gain op-amps.

Even though the controller's fixed or pulsed gate output is able to handle a few device loads, remember that the inverter of the 200X is limited to 30mA unless an external negative source is connected to provide a boost of up to 100mA. Also, having op-amp buffers will further extend the current limit for up to 100mA per buffer, which is a welcome source for applications with saturated GaN transistors.

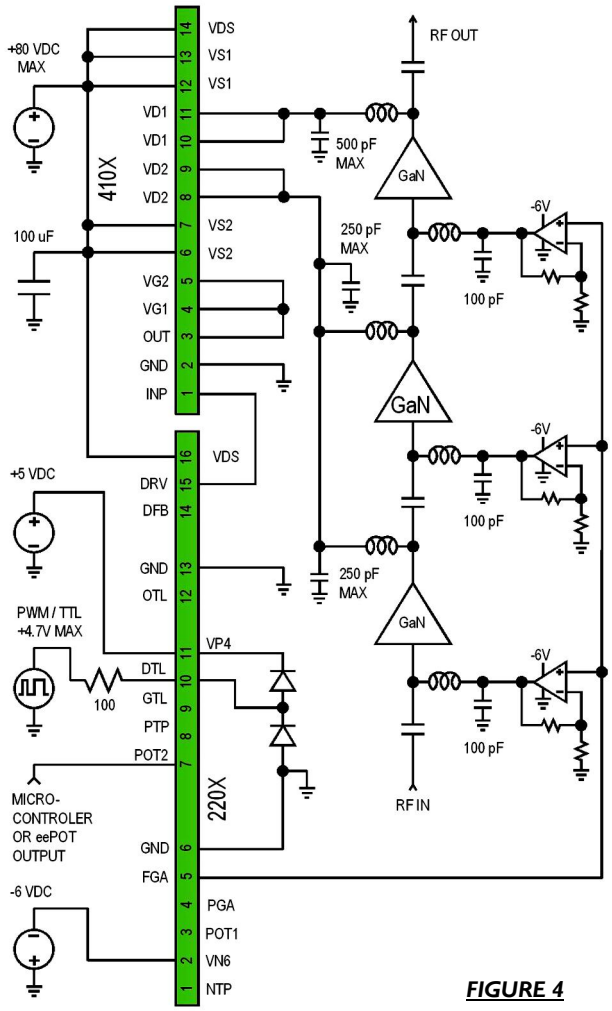


FIGURE 4

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

5. More Application Diagrams

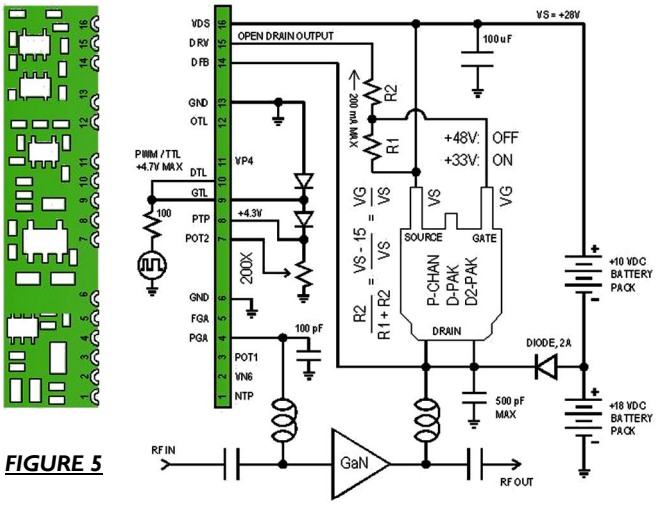


FIGURE 5

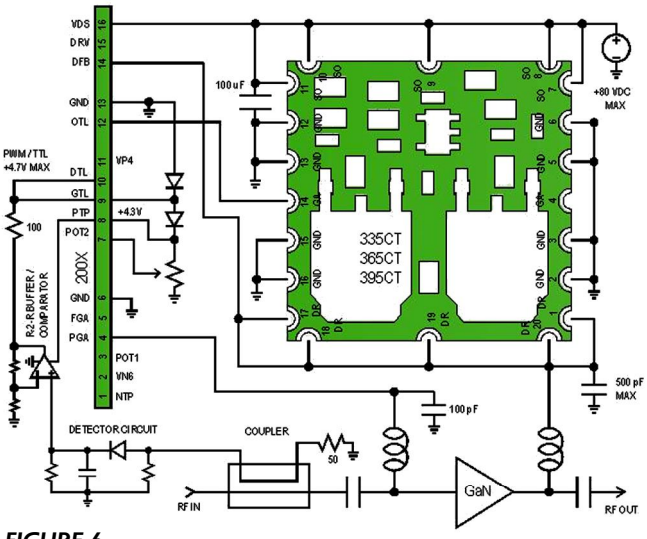


FIGURE 6

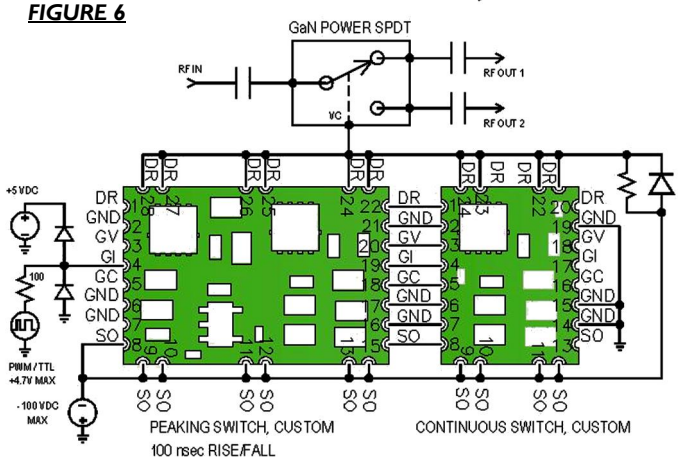


FIGURE 7

The diagrams on the left are customer applications utilizing the Controller and Switch for specific tasks. Figure 5 is a high-efficiency, dynamic drain voltage that provides two power settings for transmitters of emergency radio packs. This concept can also be applied to RF signals with high peak-to-average ratios (PAR). Figure 6 is a kW-level amplifier with short, high-speed pulses. It does not rely on a TTL trigger, but instead, RF is automatically detected and enables the power sequence of the device. Figure 7 is an ultra-high speed driver for a GaN-based SPDT Switch. It uses a peaking-switch with ON & OFF speeds of <100nsec. Then a continuous-switch maintains its state. This customized pair can also be configured for PIN diodes of Silicon or GaN variety.

6. Drop It, Set It , & Forget It

When making a printed circuit board becomes too much of a commitment and fast prototyping is needed to prove a concept, then a drop-in Evaluation Board would make more sense. They provide the quickest and complete solution for proper GaN operation. Figure 8 shows a variety of devices controlled with a tiny 600E Series drop-in, eval board mounted next to it. These also come with castellation for surface-mounting on production units. The CW modules shown below are equivalent to the schematic diagram in Figure 2, page 2. The MOS switches have 12A and 36A peak, with 6A and 16A average capacity respectively.

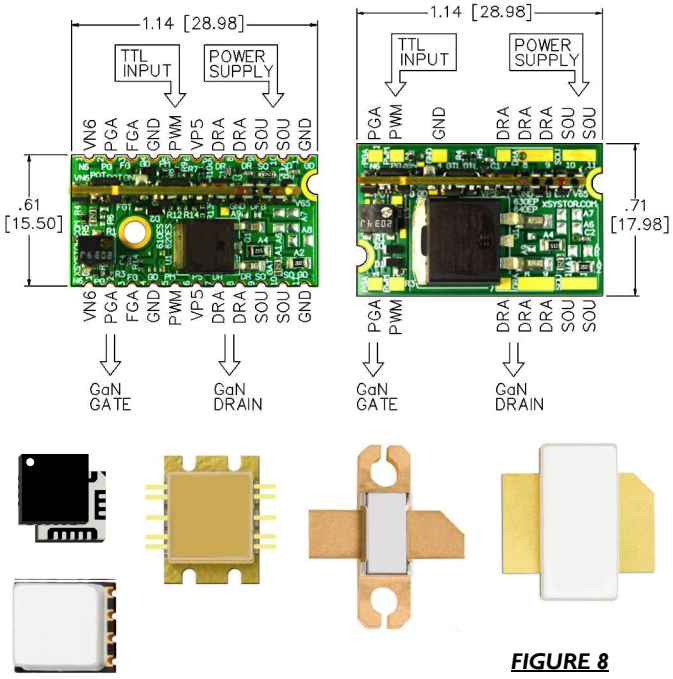


FIGURE 8

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

5. Start-up and Operation

Prior to any power start-up, the following must be taken into account and double-checked.

- *Perform continuity tests of all connections leading to the gate and drain sides of the transistor.*
- *Disconnect all DC supplies and signal inputs. Then measure proper output levels. Prevent recall commands from instruments which could be inadvertently summoned with destructive results, like excessive drain & gate voltages as well as non-TTL signals.*
- *Refer to the I/O pin descriptions on the first page. As a default, leave unused pins open.*
- *Practice safe handling and prevent ESD damage.*

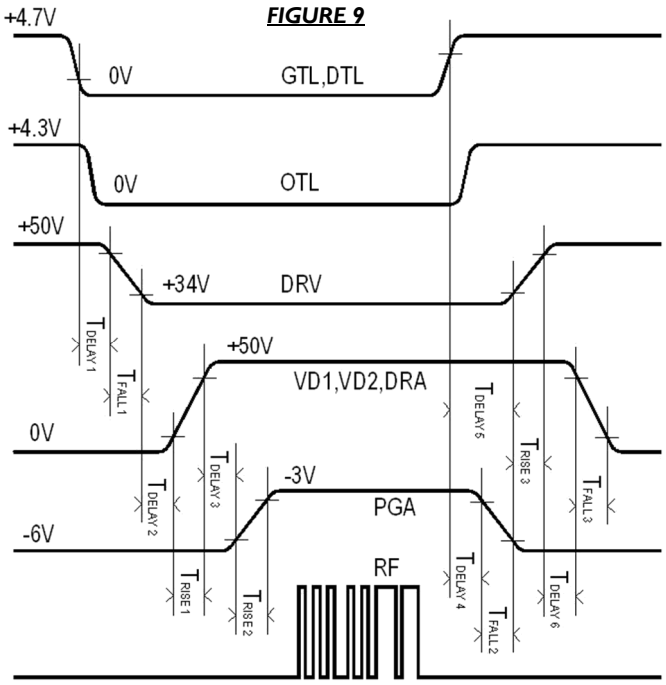
The controller will protect the GaN device from any sequence of power-up and power-down activity, provided the connection to device gate is solid. The negative supply is turned ON first. In cases where negative voltage is generated by the controller, the main power supply can be turned ON, but ONLY if power is disconnected firsthand from reaching the GaN drain physically. When the proper gate level is established with the potentiometer and measured at the device port, only then should drain voltage be turned ON or reconnected. As a matter of habit during operation, negative voltage should be first in and last out, and the controller may only provide back-up protection.

An alternative test method for initial operation of controller & switch is to temporarily take out the GaN device and replace with resistive and capacitive loads. As a starting point, refer to the spec sheets which assumes a gate load of 2.7KΩ + 500pF and drain load of 1.0KΩ + 500pF. Once the proper signals are established, the GaN device may be reinstalled.

6. Timing Diagrams

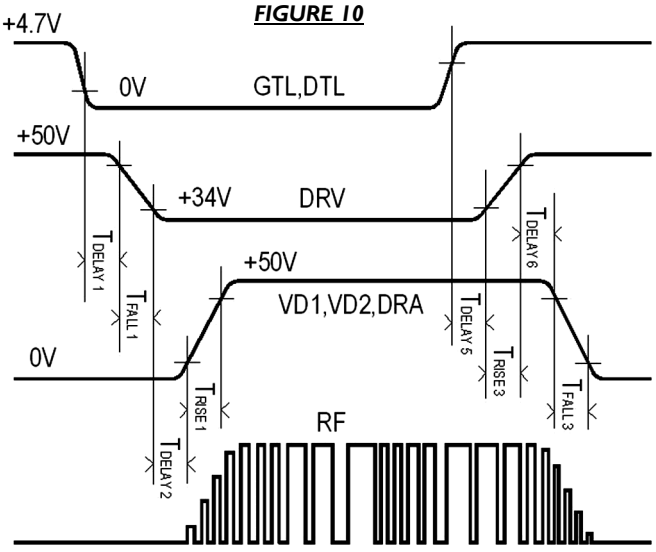
The timing sequence in Figure 9 illustrates a master-slave relationship of drain-gate switching with the 100 or 200 Series Controller connected to the 300 or 400 Series Switch. To do this, the gate switch enable pin (GTL) is tied or synchronized with drain switch enable pin (DTL), and then started up with an active-low TTL signal. The controller produces an optional TTL output (OTL) and an open-drain current drive (DRV). Then the MOSFET switch turns ON and supplies power to the transistor (from VD1, VD2, or DR).

FIGURE 9



Only with the presence of drain voltage would the gate switching feature activate (PGA), and finally turns on the GaN device for RF to transmit. The sequence is finished with the rising end of the TTL signal. The pulsed gate (PGA) goes back to pinch-off voltage and drain voltage (VD1, VD2, DR) shuts down thereafter. Note that the total ON propagation time from TTL to RF is the sum of time delays, rise times, and fall times shown in the diagram. Total propagation times of <500nsec are common.

FIGURE 10



XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

Figure 10 has a timing sequence that's typical of sub-models like the 124/224 with no gate switching capability. Gate bias is left as a fixed value, so drain voltage activity turns the GaN device ON and OFF . This particular diagram shows a CW RF to be pulse modulated. In a different scenario when gate switching is available, we can fix the drain voltage to a steady state and pulse the gate bias instead to get a similar result. Either way, the gate (GTL) and drain (DTL) enable pins are really independent and will cater to various customer preference.

7. Temperature Compensation

This subject is best described in its own application note, but some general functionalities will be noted here. The 100 & 200 Controllers have two provisions to add temperature compensation. The first is adding a specific thermistor to the unit. This is a custom feature not included in the standard fare. Though handy, the sensing component is far removed from the base plate or heat source, and may require over-compensation to work.

The second way is installing a familiar temperature sensor IC or discrete circuit near the device and feed its resultant voltage to the controller input, POT. This same pin is also connected to the potentiometer that established the operating gate bias. Now the two signals are combined by an op-amp adder circuit to produce a composite negative voltage for the GaN device. Series resistors for each voltage inputs are first calculated to regulate the impact of the variable voltage from the sensor.

In general, typical temp sensors have positive voltage outputs; therefore, the 200 Series Controllers are more apt to the task to share the POT pin for positive inputs.

8. Mounting Considerations

The 100X/200X controllers and the 400X switch have very small footprints considering they are mounted upright on the receiving board. The I/O ports are castellated holes with a 50 mil pitch. The "L" models have a lower profile of 0.20" height with castellation at 60 mil pitch. The "T" models have 0.10" long terminal pins at 50 mil pitch that would make them stand on their own. Though reflow soldering is acceptable to mount them, care should be taken that a large temperature gradient at the top of the units may dislodge components or worst burn them. At this time, manual installation is recommended with lead-free solder at <230°C, otherwise the reflow process is appropriate at <195°C.

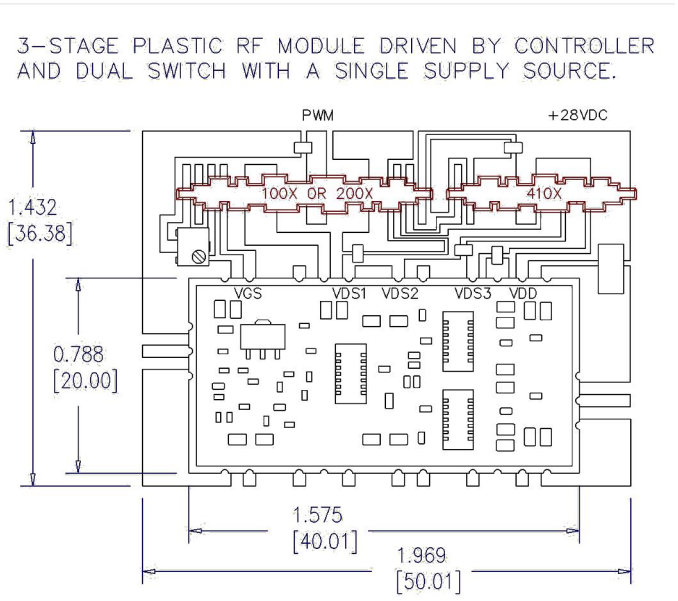


FIGURE 11

Ideal placement for controllers is on the gate side of transistor while MOSFET switches on the drain side, as shown on Figures 11 and 12. The units should be as close to the device to minimize parasitic inductance from supply lines. The drain side is especially susceptible to large voltage spikes if there's significant distance between the RF choke and the switch.

In cases where system requirements have tougher height restrictions from components, the 100X & 200X controllers are better suited to address this. The units can be installed in three ways, which are upright, slanted, and flat & buried. A resultant height of 0.10" [2.54mm] can be realized from the board surface. This is illustrated in the application note XAN-4: Mounting schemes for the Controller.

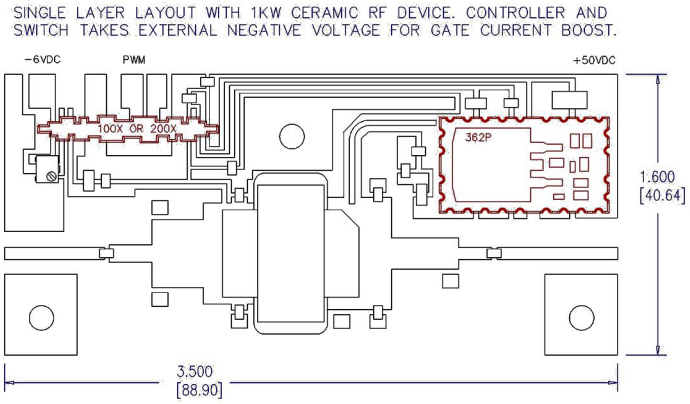


FIGURE 12

XAN-2:
Connecting the Controller and Switch

XSYSTOR

APPLICATION NOTE
July 2017

9. Adjusting Gate Threshold Shutdown

The 100/200 Series Controllers come in presets of –2.6V, -2.0V, -1.4V, or -0.8V thresholds at the device gate, where drain voltage is shutdown when these levels are reached. The device gate operating voltage or quiescent voltage is typically 0.5V lower than these presets. The user has the option to adjust them when necessary to precisely trigger a shutdown event and protect the GaN transistor from excessive current or runaway. Figure 13 illustrates the tap points of resistors R1, R2, or R3 when increasing or decreasing the preset voltages with a single resistor. Refer to Page 1 for the pin descriptions. Always shutdown power to the Controller when soldering new components.

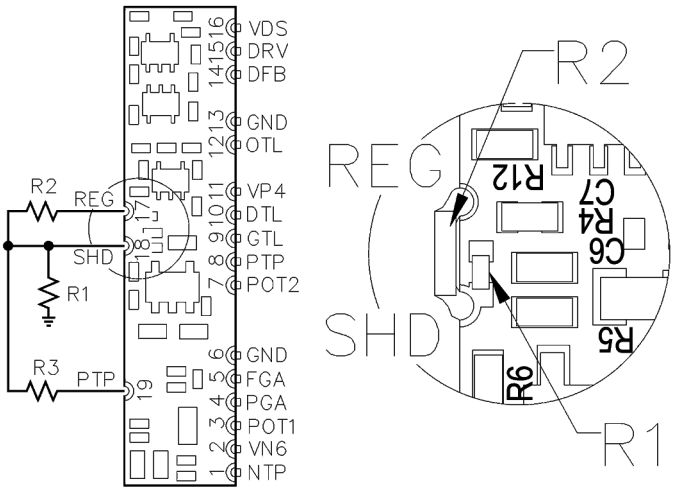


FIGURE 13

If chip resistors are preferred, the placeholder for R1 will fit an 0201 size. R2 will fit 0603 or 0805 size, and soldered on top of the unit between pins REG and SHD. On the other hand, a simpler approach to tapping these points is by using small axial resistors between 100KΩ and 1MΩ. The table below shows resistance values needed to increase or decrease the threshold presets.

	R1 (Ω)			R2 or R3 (Ω)		
ADJUST →	-0.4 V	-0.2 V	-0.1 V	+0.1 V	+0.2 V	+0.4 V
PRESETS↓						
-2.6 V	120K	240K	480K	620K	310K	150K
-2.0 V	140K	280K	580K	600K	300K	150K
-1.4 V	140K	280K	580K	500K	250K	125K
-0.8 V	140K	280K	580K	400K	200K	100K

10. Controller Selection Guide

MODEL	DESCRIPTION
100X, 100T, 100L	100X, 100T, & 100L ARE IDENTICAL FUNCTIONALLY BUT DIFFER STRUCTURALLY. SUFFIX 'T' STANDS FOR TERMINAL PINS AT 50 MIL PITCH, WHILE 'L' FOR LOW PROFILE AT 60 MIL PITCHED CONNECTIONS. 'X' IS STANDARD CONFIGURATION. THE 100X & 100L MOUNT ON PCB FROM CASTELLATED I/O PORTS. THESE UNITS CONTROL THE GaN TRANSISTOR BY SWITCHING THEIR DRAIN AND GATE SUPPLIES SEQUENTIALLY OR INDEPENDENTLY. A SINGLE SUPPLY OF UP TO +65V IS SUFFICIENT TO OPERATE. THE 100 SERIES HAVE NON-INVERTING INPUTS, WHICH MEANS IT TAKES NEGATIVE VOLTAGE TO PRODUCE NEGATIVE GATE BIAS TO THE
120X, 120T, 120L	SAME AS THE 100 SERIES BUT WITHOUT GATE SWITCHING CAPABILITY. A FIXED GATE BIAS VOLTAGE IS UTILIZED INSTEAD.
122X, 122T, 122L	SAME AS THE 100 BUT WITHOUT GATE SWITCHING AND VOLTAGE INVERSION. A NEGATIVE SOURCE IS SUPPLIED BY THE USER.
124X, 124T, 124L	THIS MODEL IS A BASIC GaN SEQUENCER/MODULATOR. THERE ARE NO GATE SWITCHING, VOLTAGE INVERTER, AND LOGIC SUPPLY. THE USER BASICALLY PROVIDES THE NECESSARY DC SOURCES THAT'S ALREADY IN THEIR SYSTEM.
200X, 200T, 200L	200X, 200T, & 200L ARE THE SAME AS THEIR COUNTERPARTS ABOVE EXCEPT THAT THEY HAVE INVERTING INPUTS. IT TAKES POSITIVE VOLTAGE TO PRODUCE NEGATIVE GATE BIAS TO THE
220X, 220T, 220L	SAME AS THE 200 ABOVE BUT WITHOUT GATE SWITCHING CAPABILITY. A FIXED GATE BIAS VOLTAGE IS UTILIZED INSTEAD.
222X, 222T, 222L	SAME AS THE 200 BUT WITHOUT GATE SWITCHING AND VOLTAGE INVERSION. A NEGATIVE SOURCE IS SUPPLIED BY THE USER.
224X, 224T, 224L	THIS BASIC SEQUENCER/MODULATOR HAVE NO GATE SWITCHING, VOLTAGE INVERTER, AND LOGIC SUPPLY. THE USER PROVIDES ALL DC SOURCES ALREADY PRESENT IN THEIR SYSTEM.

11. MOS Switch Selection Guide

MODEL	DESCRIPTION
332P	SINGLE 12A SWITCH MODULE FOR PULSED APPLICATIONS.
332N	ADD-ON TO 332P FOR A COMPLEMENTARY CONFIGURATION.
335CT	12A POWER CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
362P	SINGLE 36A SWITCH MODULE FOR PULSED APPLICATIONS.
362N	ADD-ON TO 362P FOR A COMPLEMENTARY CONFIGURATION.
365CT	36A POWER CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
392P	SINGLE 8A SWITCH, MINI-MODULE FOR PULSED APPLICATIONS.
395CT	8A MINI CMOS MODULE WITH TTL DRIVE. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE/FALL TIME REQUIREMENT.
410X, 410T, 410L	HAS DUAL 8A MOSFET SWITCHES FOR CW OR GENERAL PURPOSE OPERATION. 410X, 410T, 410L ARE IDENTICAL FUNCTIONALLY BUT DIFFER STRUCTURALLY. SUFFIX 'T' STANDS FOR TERMINAL PINS AT 50 MIL PITCH, WHILE 'L' FOR LOW PROFILE AT 60 MIL PITCHED CONNECTIONS. 'X' IS STANDARD CONFIGURATION. THE 410X & 410L MOUNT ON PCB FROM CASTELLATED I/O PORTS.
420X, 420T, 420L	HAS DUAL 8A MOSFET SWITCHES FOR PULSED APPLICATIONS. LIKE THE 410 AND 430, THEY ARE SMALLER THAN THE 100/200 CONTROLLER MODULES AND WORK WELL IN TIGHT SPACES.
430X, 430T, 430L	THE 8A P-CHAN & N-CHAN MOS SWITCHES ARE COMPLEMENTARY AND WORKS LIKE A PUSH-PULL. SPECIFIC TO PULSED OPERATION WITH VERY FAST RISE AND FALL TIME REQUIREMENT.

XAN-4:
Mounting Schemes for the Controller

XSYSTOR

APPLICATION NOTE
July 2017

Background

The 100/200 Series GaN Controller is a versatile device. Not only can it handle a multitude of system variants described in the spec sheets and app notes, but the in-line, castellated ports allow multidirectional mounting, narrow landing patterns, and adaptable height profiles. The positioning and soldering of these modules are done either manually, or with the aid of available erector kits for reflow. Note that the circuit board uses lead-free, high-temp solder. However, care should be taken when exposing them to similar temperatures during reflow and assembly.

Mounting Schemes

UPRIGHT

This is the standard method for installing the Controller module. All components from both sides of the board are visible for easy identification and troubleshooting. The maximum height is 0.24" [6.1mm] from the mounting pads. Erector sets (see next page) may be used to aid installation. They clamp on the module and their four legs are press-fit through a clearance hole on the receiving board, which locks the unit in place during solder reflow.

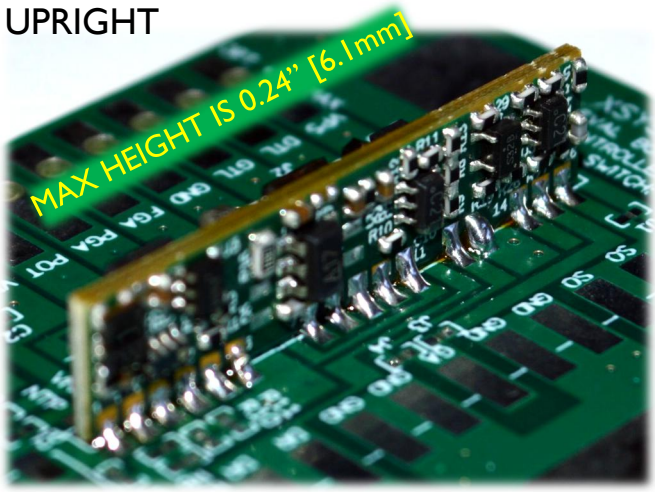
SLANTED

To lower the height profile in a simple step, this is a preferred method. The maximum height is 0.16" [4.1mm] from the mounting pads. Erector sets (see next page) may also be used to aid installation. They clamp on the module and maintain a stable angle during solder reflow. The components on the other side of the board will no longer be visible. With the increased footprint, care should be taken when running active lines underneath the module.

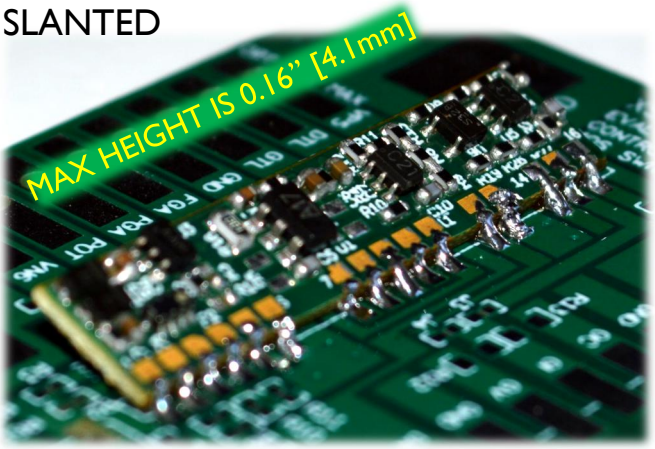
FLAT & BURIED

This method is more involved but a maximum height of 0.10" [2.5mm] from the mounting pads can be realized. The receiving board will have to be routed out to give the buried components a clearance of 0.05" [1.3mm] approximately. This may extend into the heatsink if applicable. An alternate solution is to install the module at the edge of the receiving board. The sixteen (16) solder points are very strong and will be more than enough to suspend the module horizontally. Further, the use of potting epoxy for support and heat dissipation may be supplemental.

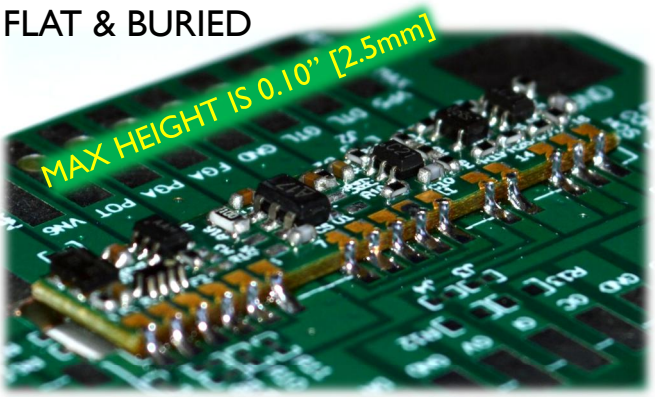
UPRIGHT



SLANTED

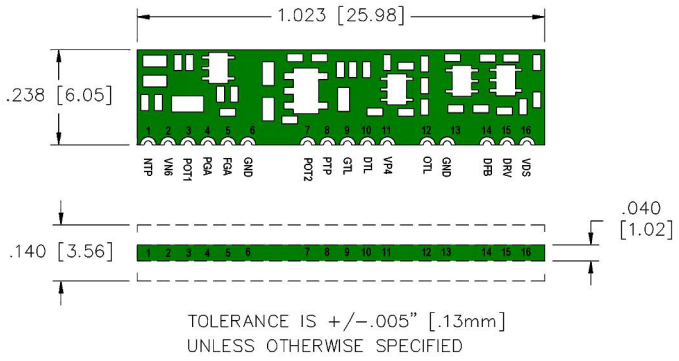


FLAT & BURIED

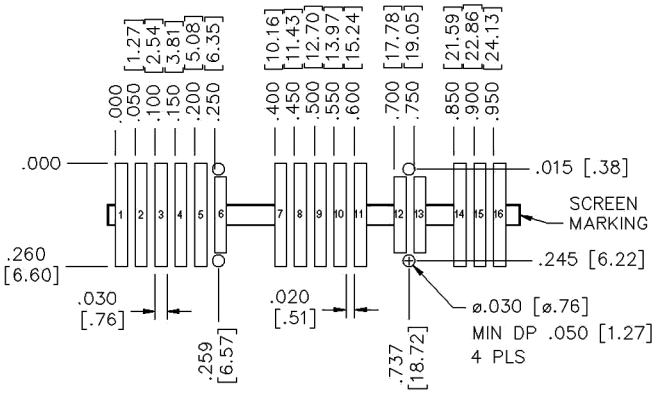


Land Patterns

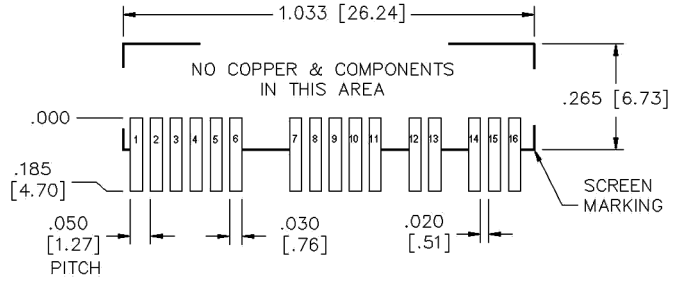
100X, 200X



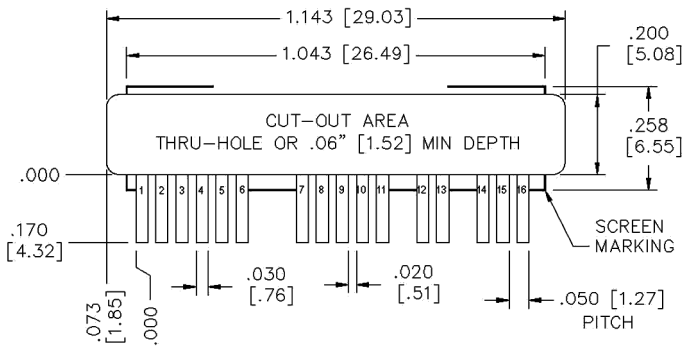
UPRIGHT



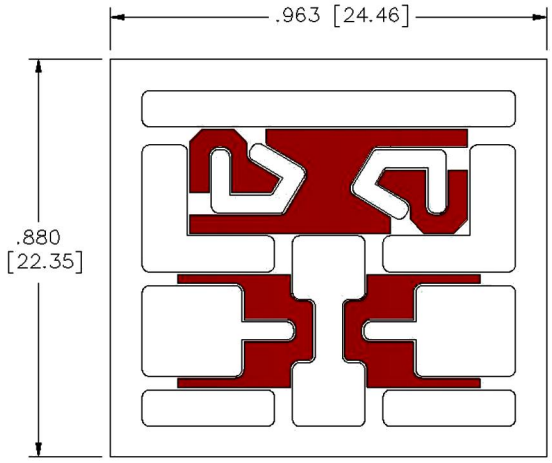
SLANTED

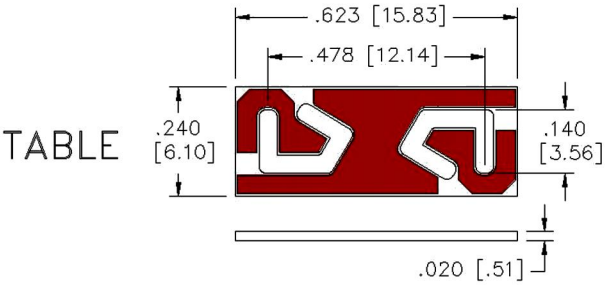


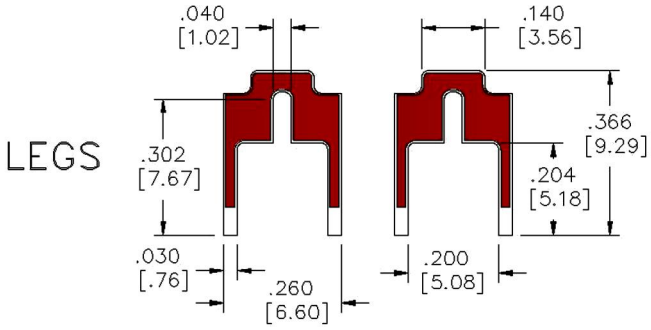
FLAT & BURIED

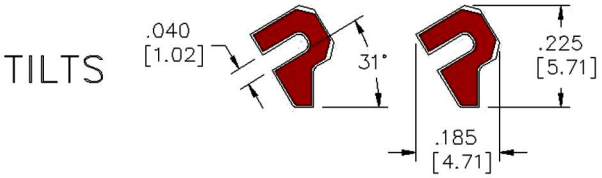


Module Erector Kit









The Erector cutouts shown above are used to facilitate the solder-reflow process for module installation. Use sharp wire cutters to separate and shape the pieces. They may be discarded after use. For UPRIGHT assembly, the TABLE and LEGS are snapped together and clamped onto the empty grooves of the module. The LEGS are either cut to size or press-fit through holes on the receiving board. For SLANTED assembly, TILTS are clamped onto the module instead. Either LEGS or TILTS may be used as spacers for the FLAT & BURIED assembly.

XAN-6:
Converting Switch from Pulsed to CW

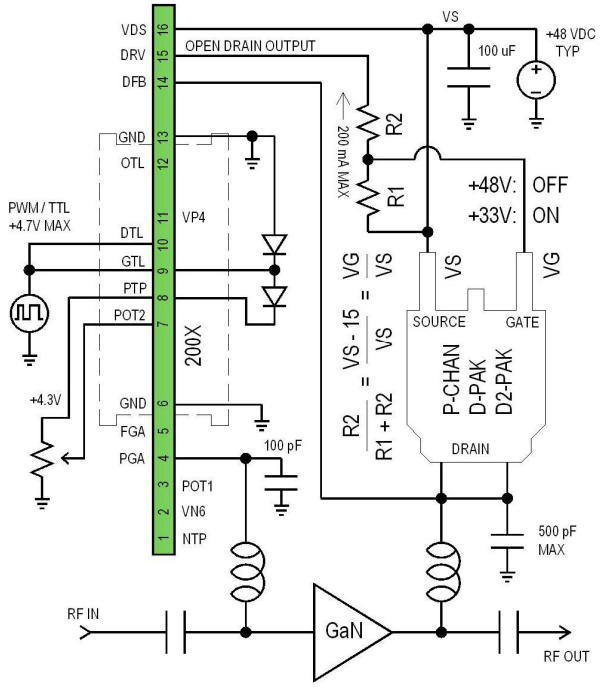
XSYSTOR

APPLICATION NOTE
July 2017

Background

GaN transistors operate in a host of drain voltages from 24V to 65V. While any Pulsed Switch type currently offered can accommodate them easily, it is not so easy with a CW switch to cover all voltage possibilities. The CW switch is very simple, and consists of a P-channel MOSFET with two resistors, which was detailed in previous application notes and diagrams. This app note allows the user to convert all types of single MOS Pulsed Switches into a CW version, in the event that pulse requirements become longer than 500usec width or 5msec period.

CW Switch Schematic

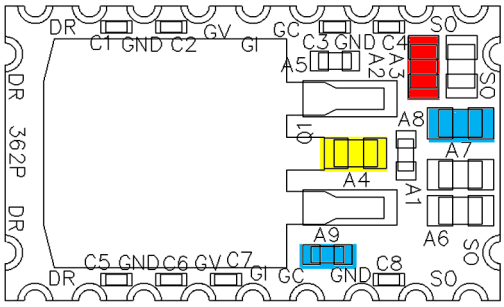


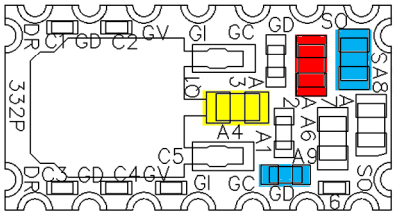
The diagram above shows a controller with an open-drain output driving a CW switch. It can be seen that the gate voltage to the MOS device is always 15V below the source level to turn-ON the switch. Therefore,

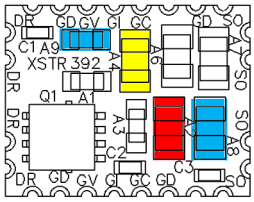
$$\frac{R2}{R1 + R2} = \frac{VS - 15}{VS} = \frac{VG}{VS}$$

Where, drive current Idrv ≈ 5mA << VS / (R1 + R2) << 100mA typically. Increasing current improves speed, but at the cost of added heat to the controller and resistors.

Modifications to the Switch



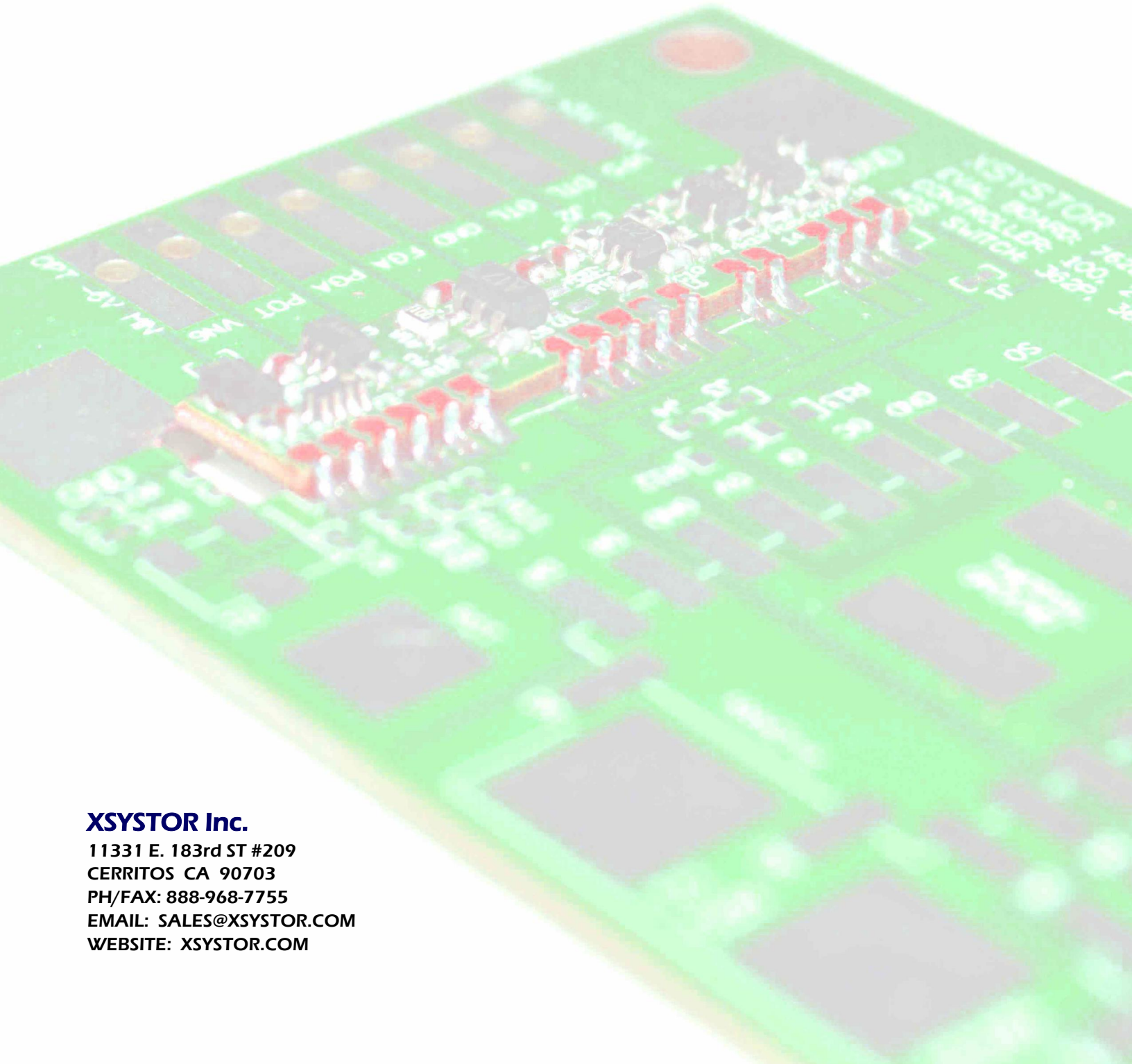




Rework Instructions:

1. Only Switches 332P, 362P, and 392P apply.
2. Place module on a hot plate set at 120°C. Use solder gun or hot-air gun to remove or insert parts. Lead-free solder melts at approximately 220°C.
3. Remove four components A2, A4, A8, and A9. They are indicated by red, yellow, and blue colors.
4. Insert placeholder A2 (shown in red) with R1 resistor as calculated from the schematic.
5. Insert placeholder A4 (shown in yellow) with R2 resistor as calculated. Make sure to use higher wattage resistors for appropriate current drawn.
6. Use lead-free solder as necessary.
7. Below are initial values to consider:
   - VS = 28V, Idrv = 5.2mA, R1 = 3.0K, R2 = 2.4K
   - VS = 36V, Idrv = 5.2mA, R1 = 3.0K, R2 = 3.9K
   - VS = 48V, Idrv = 5.4mA, R1 = 3.0K, R2 = 6.2K

Note: Scale down resistor values to increase current and switching speeds.



XSYSTOR Inc.
11331 E. 183rd ST #209
CERRITOS CA 90703
PH/FAX: 888-968-7755
EMAIL: SALES@XSYSTOR.COM
WEBSITE: XSYSTOR.COM