Design and Comparison of Performance of Different Types of Adders

C Meghana[1], G Sai Kumar[2], N Chandrashekhar[3], S N Chandrashekhar[4] and Dr. S Ramani[5]

[1,2,3] *B. Tech Final Year Students, Department of Electronics and Communication Engineering Sreenidhi Institute of Science and Technology, Hyderabad, Telangana, India.*

[4,5] *Faculty, Department of Electronics and Communication Engineering Sreenidhi Institute of Science and Technology, Hyderabad, Telangana, India.*

***Abstract*—**Adders are the primary blocks of any electronic circuit. An adder is a circuit that sums up two signals. Adders can be of any size and there are sufficient number of adders which performs an N-bit addition. Efficient design of adders enhances the performance of the processors. as there are many types of adders, by studying the performance of adders helps us to understand where a particular adder can be used according to the requirement. Proper utilization of adders according to the requirement is equally important. This motivated us to design and analyse the performance of some adders and conclude a better one among them. The parameters that we used to study these adders are power, area and delay. The adders that we are going to evaluate are Ripple carry adder, carry lookahead adder, carry select adder, carry skip adder and carry save adder. As this is a software-based design project, we use two different tools. They are: Microwind and Mentor graphics. In Microwind, we have another tool integrated called DSCH where we implement the circuit. In Microwind, we obtain the power and in mentor graphics we validate the functionality and obtain the parameters area and delay. In this project we designed different types of adders and evaluated the performance so that one can select the adders require. Finally, we conclude that if we require a power efficient adder which can compromise on delay, we can use ripple carry adder. If we require an adder with extreme timing deadlines, we go for carry select adder. Instead of using Microwind DSCH, we have implemented this project in xilinx vivado to compare the performance of different types of adders with power, area and delay of different adders.

***Keywords*—**Adder, Comparison, Delay, Microwind.

1. INTRODUCTION

Embedded systems and electronic gadgets effect the present day lifestyle of people. Developments in technology have paved a way to improve the characteristics and study the designs in circuit level. Adders on the other hand effects the performance of these systems, as adders are the basic building blocks for any digital circuit. In many computers and other kinds of processors, adders are used in arithmetic logic units. They are also used in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operations and similar operations. Hence the study on performance of adders plays a major role in improving the characteristics of the electronic devices.

An adder is a circuit that sums up the amplitudes of two signals. Adder circuits can be constructed in many number representations, such as decimal, binary, hexadecimal, octal etc., In general, we implement in binary numbers. Even in the binary, n-bit adders can be constructed. A Half adder (HA), is an adder which simply adds two bits and generates a sum and carry, but is incapable to adding two numbers. A Full adder (FA), also add two input signals but in addition has a carry in signal. The circuit of a half adder and full adder are fixed but when it comes to an n-bit adder using these adders, it gives us many ways in implementing or designing the adders. One of the basic n-bit adder is a ripple carry adder(RCA), some other adders are: Carry lookahead adder (CLA), Carry skip adder (CSA), Carry increment adder(CIA), Carry select adder(CSeA), Carry save adder(CSaA), so on…

Power, Area and Delay

In order to estimate the performance of an adder, power, area and delay play a significant role. As per the design concerns, the best adder requires low power consumption, compact design (small area) and High speed (less delay). If we can understand the factors that effects these parameters it helps in designing the better adder.

A. POWER:

Power consumption is a primary factor considered in designing an embedded system. For any electronic system, low power consumption along with long battery life is desirable. ASIC design comparatively consume less power when compared to same application implemented on an FPGA. The major source of power consumption in a circuit the clock tree and registers, control and data path logic and memory. The Active power is a combination of Dynamic power and Leakage power.

Dynamic power: It is the logic power. Dynamic power is due to clock transitions, switching capacitances and short circuit power. The dynamic power depends on square of the Vdd. The main focus on the circuit is to reduce the Vdd.

Leakage power: It is the current leakage when the device is in standby mode. There is no logic power in during stand

by mode. During active mode, the leakage power accounts for 10% to 30% of total power. Choosing the optimal Vdd value can even reduce the leakage power.

B. AREA:

In order to build a compact design, we need to study the y factors effecting the increase in area. To obtain the area of an ASIC design, we need to find out the area occupied by each individual logic block. The gap or interconnections between these logic block also accounts for the increase in area. Based on the gaps present between the logic blocks, the area of the ASIC is estimated. All these computations are performed in micro level hence we take the help of the EDA tools to compute the area.

C. DELAY:

The high performance (high speed) of an electronic circuit is know by estimating the delay of the circuit. Delay in simple terms is the time between the output displayed and the input triggered. There are several types of delays in ASIC design: Gate delay, Net delay, Transition delay, Propagation delay and Contamination delay.

Gate delay: The finite time taken to change the output of the gate when the input is changed.

Net delay: The time taken by the signal to reach the input of the cell from its previous output.

Transition delay: It is the time taken by the signal to change its stage ie., from 0 to 1 or vice versa is called transition delay.

Propagation delay: the time required for the input to propagate to the output.

Contamination delay: The minimal amount of time required from when an input changes until any output starts to change.

The longest path in the circuit is called as critical path, if the critical path is lengthy, the delay also will increase. If a greater number of gates are used, the delay also increases.

While modeling delays, we try to avoid certain structures due to the effect they show in the integrated circuit. The delays occurred in the logic gates is of two components, parasitic delay (T), and is given by the expression T=P+F

2. LITERATURE SURVEY

R.Uma [1][2012] stated in his paper that addition is a basic operation in signal processing, ALU's and many other devices. Therefore performance of adders will greatly influence the performance of the device that used adders. Improving the performance of adders will enhance the performance of digital systems. Adders are the basic components in most of the digital systems because of the widespread usage of adders in all the digital operation. Therefore many different adder architectures are designed and implemented in order to achieve fast execution to improve the performance.

Ripple carry adder is the simplest and the slowest adders with O(n) delay and O(n) area where n is the number of operand size in bits. Ripple carry adder is implemented by using the one bit full adders placed side by side to perform the operation. The addition is performed by adding the two input bits along with the carry bit to generate sum and carry bits. The generated carry bit is propagated to the next bit and the process repeats till the MSB. The most serious drawback of the ripple carry adder is that delay increases linearly with the bit length. The worst case delay is when the carry signal travels through all the stages of the adder chain from least significant bit to most significant bit.

Carry Look ahead adder which has an irregular layout and more number of gates have O(log(n)) delay and O(n.log(n)) area. Carry is calculated for every single bit eliminating the need for carry propagation. Carry for every bit is calculated in two gate steps which results in the same delay for generation of carry for all bits. The disadvantage of carry look ahead is as the number of input bits increases the circuitry for carry also increases resulting in increase in the power. Carry look ahead adders are implemented in two gate levels but has fan in and fan out limitations.

Carry Skip adder has low power and less delay with O(n) area and O(nl+2/l+1) delay. It uses propagate and generate logic which skips the delay thereby reducing the delay in carry propagation. Based on generate and propagate bits it is decided whether to skip the carry or not. This adder is used to speed up the large bit addition namely 32 and 64 bit.

Carry Select adder has O(n) area and O(nl+2/l+1) delay with gate depth of O(n1/2). Except for the least significant bit, carry select adder is divided into two sections, each section consisting of full adder with inputs and carry as 1 and 0. Based on the carry received from the previous bit the sum and carry of the present bit is selected through the mux. Carry select adder uses more gates thereby area and power dissipation is more. Carry select adder is 40-90% faster than ripple carry adder.

Carry Save adder performs the addition by considering the carry obtained as one of the addend. It has O(n) area and O(log n) delay. The addition is performed between the two given numbers and the obtained carry is again added to the obtained sum in the next step thus avoiding the delay due to carry propagation. The delay involved is 3 gate delay irrespective of the length of input. This avoids the delay due to carry propagation resulting in less delay compared to other adders.

In this paper, the adders are implemented at an operating frequency of 500MHz and 0.12µm technology in microwind and are compared based on the AT, AT2 and PD values. The adders are compared on the basis of AT, AT2 and PD values and efficient adder is the adder with the least value. Based on the results obtained it is visible that Carry Look ahead adder has the best tradeoff between area, power and delay making it the efficient adder to be used in the devices. Carry Select and Carry Save adders are the fastest adders to perform the addition with high area requirement than other adders.

Jasbir Kaur [2] [2015] mentions that there is a need to develop the adders with either high speed or less area or combination of both. The journal further speaks about the

comparison of adders based on power, area, delay and gate count with an operating frequency of 500MHz.

Carry Increment adder consists of ripple carry and incremental circuitry. The incremental circuitry consists of series of half adders in sequential order. It has O(n) area and O(nl+2/l+1) delay. The addition is done by dividing the input into sets of 4 bits. The first set is added using the ripple carry adder with carry as given and the remaining sets are added with carry as zero. The obtained carry from the first set along with the sum obtained in the second set is given to incremental circuitry and the sum is incremented and goes on until the last set. The performance of carry increment adder can be increased further more by using carry lookahead adder in place of ripple carry adder. By this we can overcome the delay effects due to ripple carry adder.

From the results it is clear that the least power dissipation occurs for the ripple carry adder followed by carry increment adder. Carry save and carry select adder have the maximum power dissipation. In comparison with area, ripple carry occupies the least area followed by carry look ahead adder whereas carry select adder occupies more area and then comes the carry save adder.

With respect to delay, Carry increment adder and carry select adder have the least delay and ripple carry along with carry skip adder have the highest delay. Carry select and carry save adder have more number of gates whereas carry look ahead and ripple carry have less gates.

New and fast algorithms to perform addition operation are implemented at the cost of one or the other factors [3]. These factors may be power, area, delay or gate count. Ripple carry adder which is the basic adder with the least power requirement and less hardware have the disadvantage of delay incurred due to carry propagation. Carry Select adder which is designed to overcome the delay due to carry propagation achieved the least delay at the cost of doubling the components thereby increasing the number of gates and area.

3. METHODOLOGY

A. TYPES OF ADDERS

There are large number of adders that are designed to match the need of the industry. Some are designed to perform operation in less time whereas some are designed to satisfy the power and area constraints. Therefore basic adders are modified accordingly to meet the necessary constraints. Some of the basic adders are

1.Ripple Carry adder.
2.Carry Look ahead adder.
3.Carry Select adder.
4.Carry Skip adder.
5.Carry Save adder.

These adders differ in the method they choose to generate the carry. This results in variations in speed, power and area characteristics of the adder and this decides whether the adder is efficient or not.

B. RIPPLE CARRY ADDER:

Ripple carry adder is an important structure essential in designing digital circuits. It is a combinational logic circuit that is used for the purpose of adding two n-bit binary numbers. It requires n full adders in its circuit to add two n bit binary numbers. Multiple full adders are cascaded in parallel to perform addition between two numbers.

The approach of ripple carry adder to add two numbers is considered to be heuristic approach. A Heuristic approach is the one which is built by closing observing the process that is happening. Ripple carry adder is developed by observing the process of manual addition of two binary numbers. A ripple carry adder is logical circuit in which the carry out of each full adder is the carry in of next full adder. The carry gets propagated from one full adder to the next full adder i.e. from the LSB full adder to MSB full adder. Because of the rippling nature of the carry it is called as ripple carry adder.

C. CARRY LOOK AHEAD ADDER:

The main disadvantage of ripple carry adder is the delay in producing the output. This delay is mainly due to the carry propagation. One method of speeding up the process is by eliminating the carry propagation delay and this is implemented in Carry look ahead adder. Carry look ahead adder is a fast parallel adder which reduces the delay by using extra circuitry. It is an improvised form of ripple carry adder. This adder utilizes logic gates to look at the lower order bits of augend and addend to see if any higher order carry is to be generated. The time complexity of carry look ahead adder is O(logn).

D. CARRY SELECT ADDER:

Carry Select adder is one of the fastest adders where the addition of numbers does not depend on the carry form the previous carry. Here the addition of bits is carried for both carry as 1 and 0. Carry select adder consists of two ripple carry adders and a multiplexers. Adding two n-bit numbers with a carry select adder is done with two ripple carry adders in order to perform the calculation twice, once with carry as 0 and other with carry as 1. Carry select adder is considered to be one of the fastest adders because the addition operation is performed without depending in the previous full adder carry. Due to this the time required to produce the output reduces.

E. CARRY SKIP ADDER:

Carry Skip adder is a ripple carry adder that is partitioned into several blocks of full adders, attaching a carry skip circuit to each block. The design of carry skip adder is based on the definition of generate and propagate signals. Carry skip circuit consists of mux and propagate block.. Carry skip circuit checks whether the propagation condition is satisfied and skips the carry that comes from the previous block to next block. Carry skip circuits are not implemented throughout the circuit. They are implemented only at the required positions where there is the possibility of skipping the carry. At the least significant positions carry

skip logic is not implemented. The amount of hardware required for the carry skip adder is proportional to n where n is the number of bits.

F. CARRY SAVE ADDER:

Carry save adder is type of adder which is used for adding three or more numbers. Carry save adder is just a set of full adders, one per bit position which is similar to ripple carry adder. The difference is that in carry save adder the carry out of each adder is not connected to the carry-in of the next more significant adder. Instead, the carry-in is treated as another input, so that three numbers are added at once instead of two. The output carries are not propagated and added in at the next position, instead they are treated as the outputs from the circuit. The carry save adder thus produces a set of sum bits and a set of carry bits. The separate sets of sum and carry bits must eventually be recombined with the carry bits added in one place to the left of where they are generated to obtain the final result. The adder using this technique achieves high speed when many numbers are to be added.

4. RESULTS

The performance analysis of these five adders are studied based on the power, area and delay values obtained from the steps discussed in the methodology. All the adders implemented are 8-bit adders. The results are compared by taking their reference as Ripple carry adder as it is the basic adder. The obtained results in each step are shown following figures:

Ripple Carry Adder:

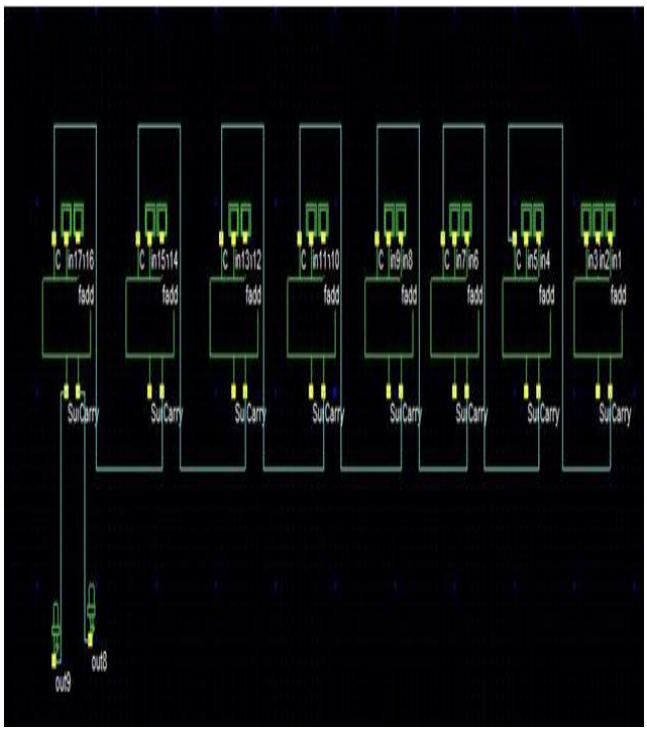

Figure 1: RCA Circuit diagram

Carry Look Ahead Adder:

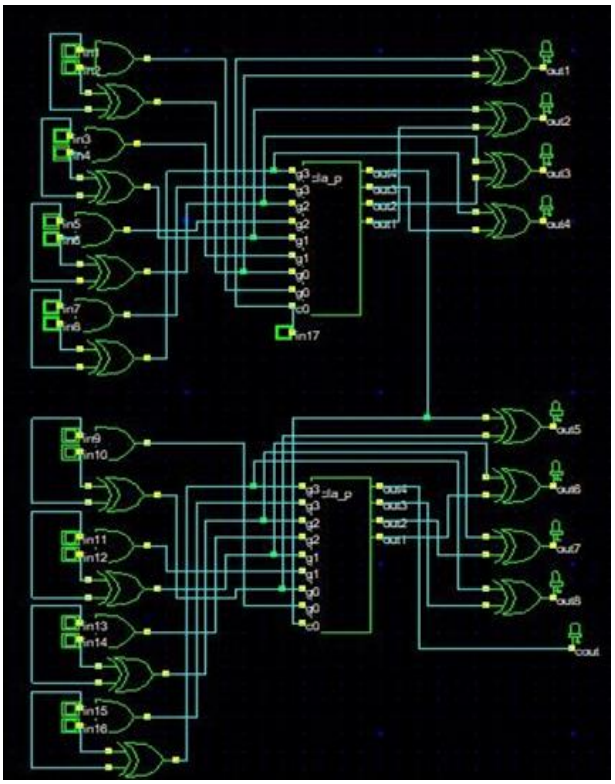

Figure 2: Circuit of Carry lookahead Adder.

Carry Select Adder:

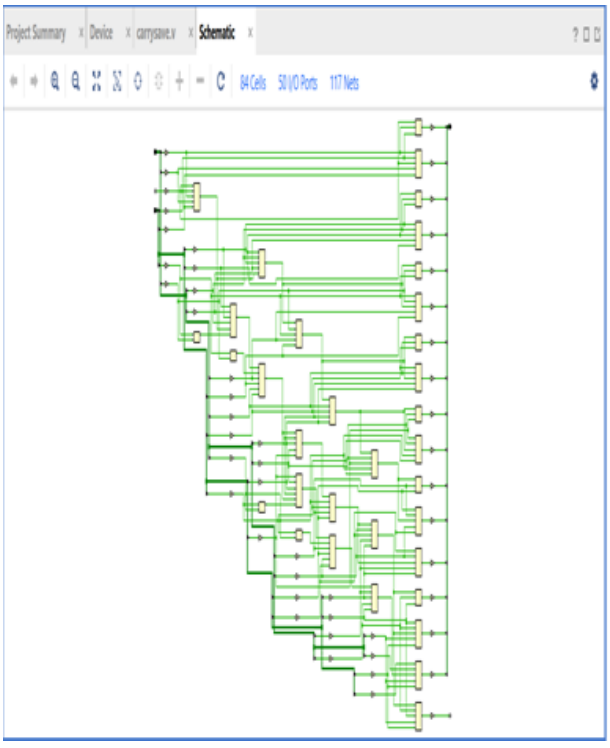

Figure 3: Carry select adder logic circuit.

Carry Save Adder:

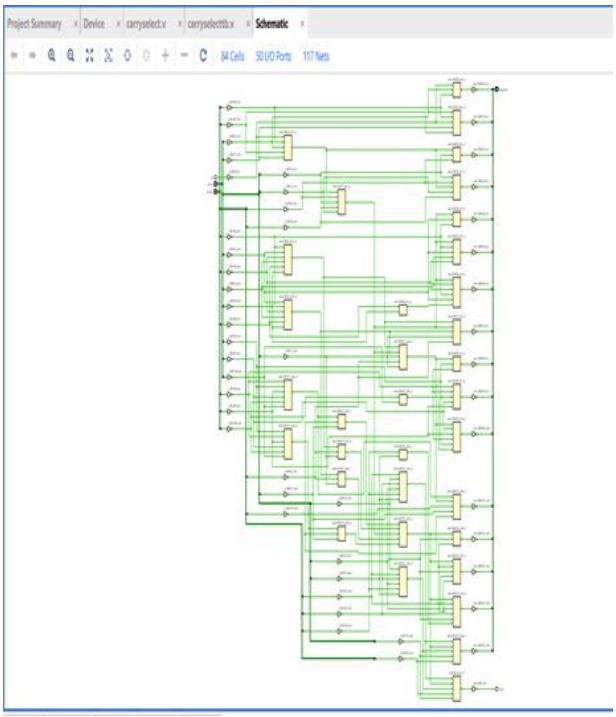

Figure 4: Carry save adder circuit.

.Carry Skip Adder:

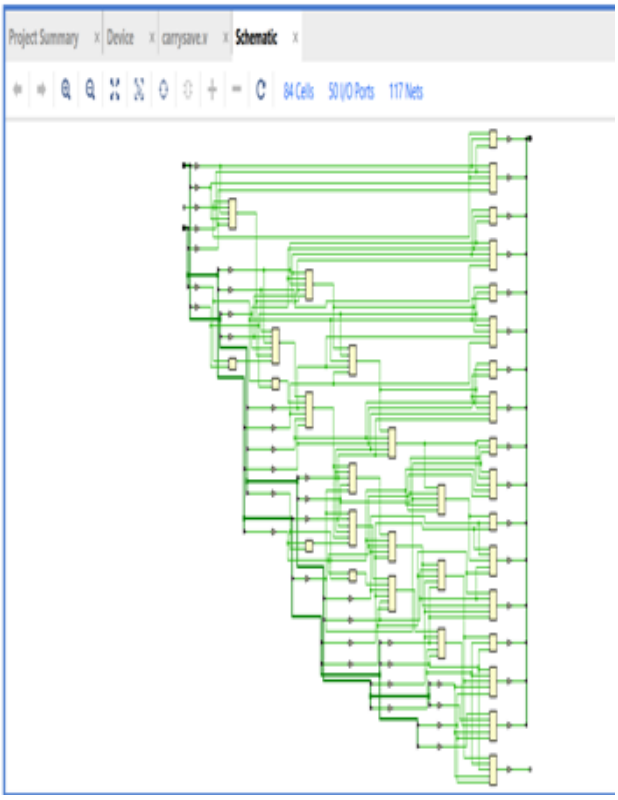

Figure 5: Circuit of Carry skip adder.

GRAPHS:

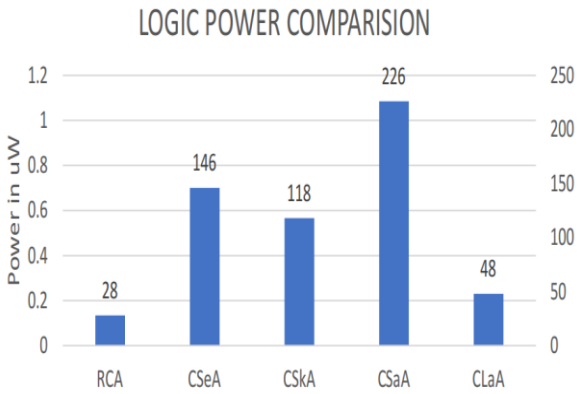

Figure 6: Graph showing logic Power Comparison.

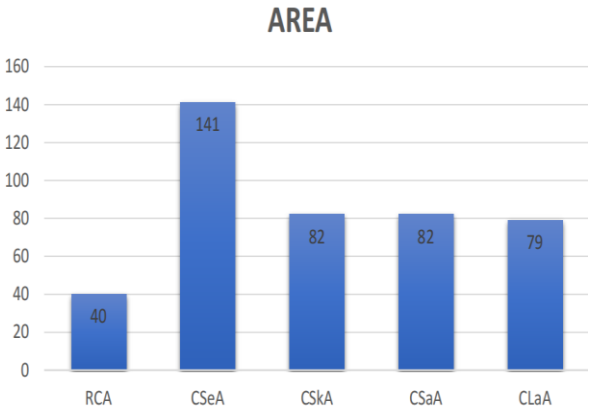

Figure 7: Graph showing Area Comparison.

Figure 8: Graph showing Delay Comparison.

5. CONCLUSION

In this project, different types of adders are designed and simulated and their performance is compared in terms of power, delay and area. To sum it up, initially we have implemented the designs of different types of adders like Ripple carry adder, Carry Select adder, Carry save adder,

Carry skip adder and Carry look ahead adder and obtained it's respective Verilog code. We have simulated and synthesised the code to obtain the power, area and delay. The main idea of the project is to compare and propose a better adder among them. By observing the results, we can conclude that, we need to compromise on any one of the parameters i.e. if you want a power efficient adder then you need to compromise in delay and vice versa. We can use these adders in the areas where we can compromise on any of its parameters. If we want to implement an adder in extremely timing deadlines then we can use carry select adder, but its power consumption is more. If there is a requirement of compromisable delays but a compact design with power efficient adders then we can go for Ripple carry adder.

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