Low Power based Dynamic TSPC D flip flop for High Performance Application based on GNRFET

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Abstract: The rapid advancement in semiconductor technology made it practicable to integrate whole electronic system on a single chip. CMOS technology is the most feasible semiconductor technology but it fails to perform as per expectations beyond and at 32nm technology node due to the short channel effects. Nano ribbon technology like GNRFET is most viable successor of MOSFETs at 22nm and beyond. In this thesis, Dynamic TSPC based D Flip-Flop are designed using GNRFET technology to improve their power consumption. Also a comparative study for various performance parameters like Average power, delay, PDP and EDP is also presented in this thesis. It can be concluded that the GNRFET technology can effectively reduce power and delay of logic gates and sequential circuits also. Hence it can be used in number of portable electronics devices applications which requires limited amount of power and by the use of this technology components the size of the device is reduced. In this thesis, we have used HSPICE software and implemented two circuits of dynamic nature namely TSPC DFF and Modified TSPC DFF.

Keywords: D FLIP-FLOP, GNRFET, 32nm, MOSFET D FLIP-FLOP, TSPC, Positive edge

I. INTRODUCTION

Many researchers have developed circuits which reduce power consumption so as to increase the portability time of the electronic gadgets in silicon industry. [1] The number of transistors increasing in a single chip is extremely rapid and so is the demand of high speed devices. [2] The necessary steps are to reduce power and increase speed in the back end devices and smaller circuits which shows incredible changes in the final product. [3][4] D Flip Flop is an important category of the sequential circuit logic family. It is used in almost all microprocessor and microcontroller chips and is an essential part of the storage and delay providing gadgets and in Very Large Scale Integration ICs. In [1], a circuit is proposed which gives better performance in 180nm technology and is based on the concept of TSPC which is popularly known as preset-able True Single Phase Clock based D flip flop. This type of D flip flop comes under the category of dynamic flip flops and is often seen that its performance is much better than that of the static D flip flop. Also the conventional D flip flop based on TSPC have certain glitches involved which are also overcome by the use of modified TSPC based D flip flop. In the modified TSPC based D flip flop, an extra transistor is added to the path in such a way that it suppresses the toggling nodes and hence reduces the glitches involved in the circuit. [1] Figure 1 shows the D flip flop symbol and truth table.

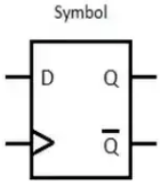

Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Figure 1: D Flip Flop Symbol and Truth Table

This paper is organized as follows, in section 1 brief introduction is given about the motivation and need of working on the topic of D flip flop and also current advancements in the dynamic flip flop are mentioned. In section to need to switch from MOSFET to GNRFET technology is mentioned and also a brief introduction about the structure of GNRFET is shown. In section 3 necessary details about the implementation of two configurations namely TSPC D flip flop based on GNRFET and a modified MTSPC D flip flop based on GNRFET is presented. In section 4, simulation results are shown which proves the benefit of GNRFET over MOSFET in 32nm technology. In section 5, conclusion of this research work is presented and hence followed by the references involved in the research work.

II. GNRFET TECHNOLOGY

The GNRFET technology having many advantages which attempts to overcome the worst types of short-channel effect encountered by deep submicron transistors, such as drain-induced barrier lowering (DIBL). [5] These effects make it harder for the voltage on a gate electrode to deplete the

channel underneath and stop the flow of carriers through the channel – in other words, to turn the transistor Off. The great challenge in the nanometer regime is due to Short Channel Effects that cause an exponential increase in the leakage current. [8][9] With the advancement in technology, Conventional CMOS has Short Channel Effects. In order to reduce the Short Channel Effects, GNRFET is used. [10] [11] GNRFETs are the new emerging transistors that can work in the nanometer range to overcome these Short Channel Effects. Due to the recent technology trends all the electronic markets are based on reliable and speed performance devices. [12] By developing semiconductor industry, all the passive and active components are assembled on a single chip named as an Integrated chip (IC). [6][7] Developing this type of technology made all the electronic devices becomes smarter and reliable in performance. It shows improvement in Average Power, Leakage and PDP. The figure 2 below shows the diagram of GNRFET.

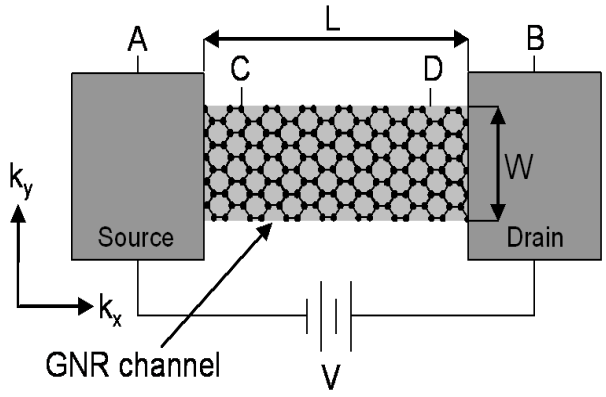

Figure 2: GNRFET Structure

The above structure shows that the channel area consists of thin ribbon like structure which is made of graphene to improve the characteristics and performances of the conventionally used MOSFET.

III. IMPLEMENTATION OF TSPC AND MTSPC BASED DFLIPFLOP USING GNRFET

The implementation is performed on simulations on software name Synopsys HSPICE, it gives the opportunity to use different kinds of transistor technologies. The technology used here is MOSFET like GNRFET, the fabrication of which resembles the MOSFET fabrication, which in turn makes it easier to replace the technology after successful results in the simulation software tool. The model files used in HSPICE are based on Verilog-a language. The netlist prepared and based on spice language and in spice format for MOSFET 32nm PTM model is used. The width of MOSFET is taken as 90nm for PMOS and 64nm for NMOS. In GNRFET configuration, all parameters are taken as default values except the number of ribbons are 3 and the number of dimmer lines in the lattice are 6. The diagrams of GNRFET based TSPC D flip flop and Modified D flip flop MTSPC GNRFET are shown in figure 3 and figure 4.

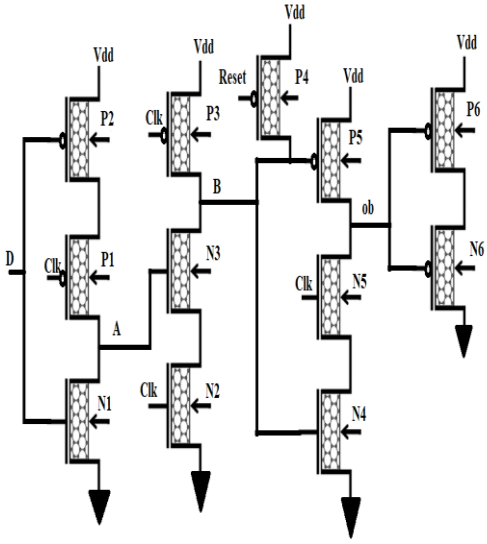

Figure 3: TSPC D flip flop using GNRFET

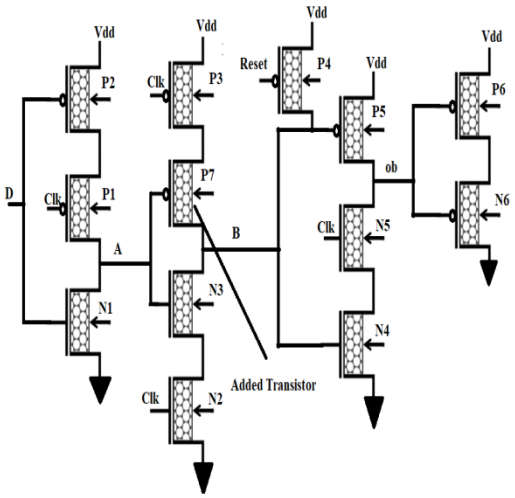

Figure 4: MTSPC D flip flop using GNRFET(Modified)

IV. SIMULATION RESULTS

This sections shows the simulations results obtained in Synopsys HSPICE software in 32nm MOSFET and GNRFET model files. The table 1 below shows the tabulated results of different parameters such Consumption of power, Delay in the circuit, Dissipation of power, PDP or energy efficiency and EDP (Energy Delay Product).

Table 1: Parameter Comparison

	MOS-32nm TSPC DFF	MOS-32nm MTSPC DFF	GNRFET-32nm TSPC DFF	GNRFET-32nm MTSPC DFF
Consumption (w)	3.63E-06	4.33E-06	7.61E-07	7.70E-07
Delay(s)	9.20E-10	9.06E-10	9.15E-10	9.14E-10
Dissipation(w)	1.16E-05	1.16E-05	6.84E-11	7.73E-11
PDP(J)	3.34E-15	3.92E-15	6.96E-16	7.03E-16
EDP(J-S)	3.08E-24	3.55E-24	6.36E-25	6.43E-25

The table above shows the numerical values of the results obtained and shows the better performance of the GNRFET based circuits.

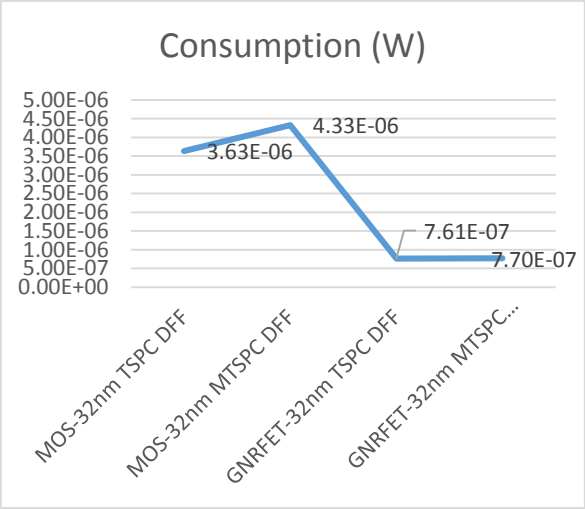

Figure 5: Consumption Comparison Chart

In figure 5, it seen that the consumption is reduced in the GNRFET based circuits.

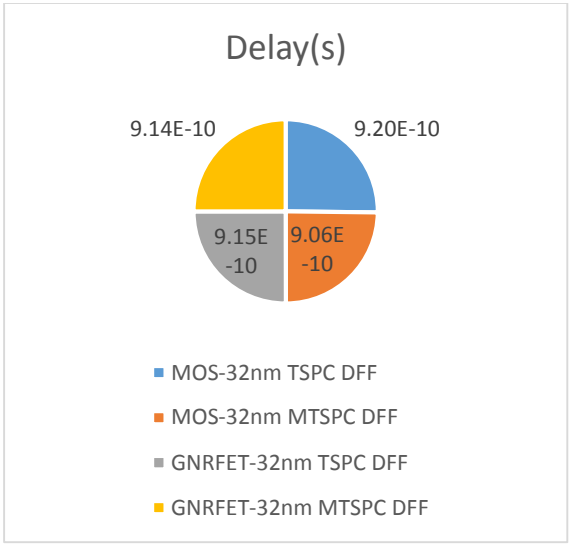

Figure 6: Delay Comparison Chart

In figure 6, it is seen that the delay is nearly same in all case and MOSFET based MTSPC is showing least delay and GNRFET based TSPC and MTSPC are showing comparably low delay when compared to the MOSFET based TSPC D Flip Flop.

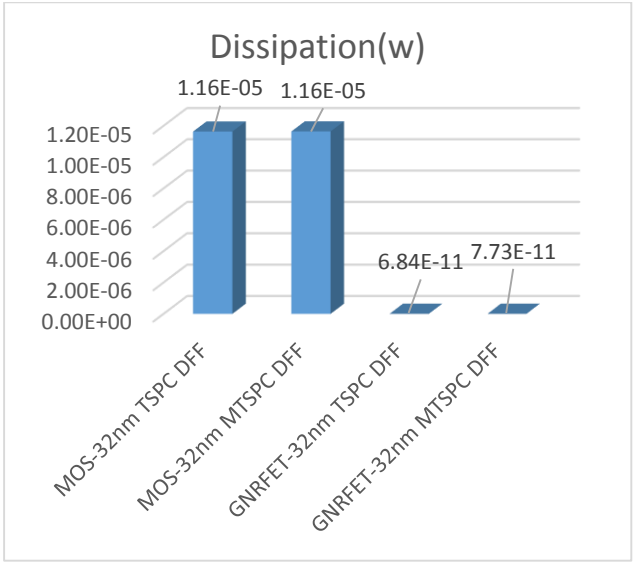

Figure 7: Dissipation Comparison Chart

In the figure 7, the dissipation of all circuits signify that the very low dissipation is seen in the circuits of GNRFET based TSPC and MTSPC D flip flop.

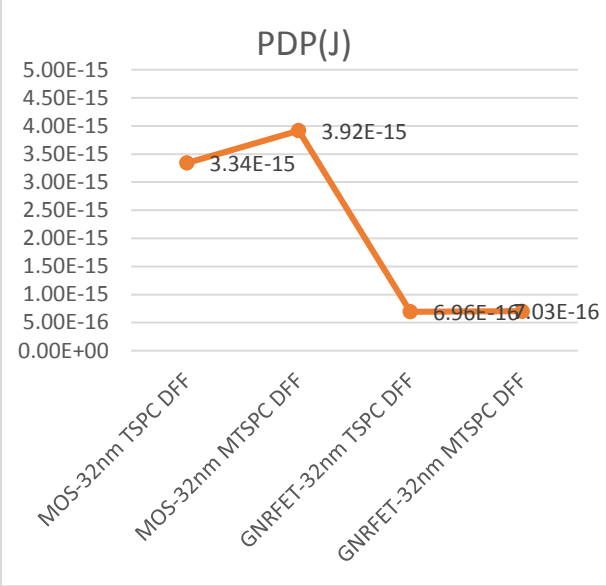

Figure 8: PDP Comparison Chart

In figure 8, the PDP values or the power delay product is seen very low for GNRFET based circuits.

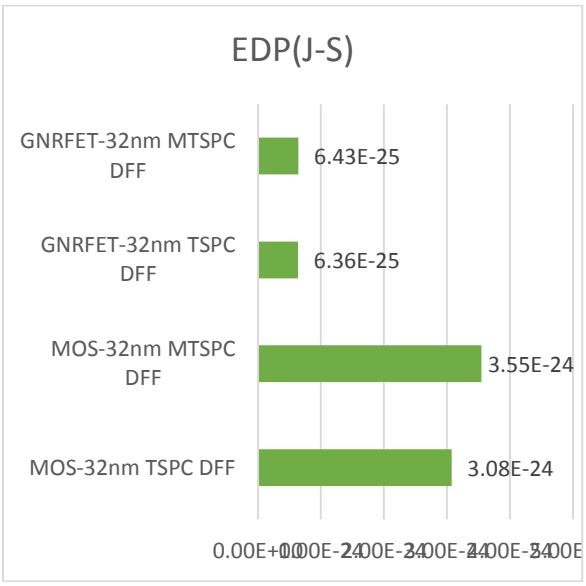

Figure 9: EDP Comparison Chart

In figure 9, EDP efficiency is seen and signifies the energy to delay product is best in GNRFET based circuits.

V. CONCLUSION

- The use of GNRFET over MOSFET in the proposed technique reduces Average Power consumption; it indicated that GNRFET is a promising substitute for MOSFET beyond in VLSI technology.
- The reduced short channel effects in GNRFET and better control over the gate of the GNRFET improves the Power dissipation in designed techniques.
- Power consumption is reduced by 99% and delay is comparably low in GNRFET when compared to MOSFET based TSPC D flip flop.

VI. REFERENCES

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