**ADF4350, ADF4351**

This document answers common questions relating to the usage of the ADF4350, ADF4351, and their evaluation boards.

### Evaluation Board
If only using one of the RFout SMA connectors, terminate the other with 50 Ω. This can be either a SMA termination or a 50 Ω resistor between the trace and GND.

To use USB power:

To use external power (5.5 V on banana connectors):

### Initialization Sequence
After powering up, write registers in this order:

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5, R4, R3, R2, R1, R0</td>
<td>Write registers in this order: [R4], [R1], R0 (R4 only required if MOD changed).</td>
</tr>
</tbody>
</table>

### Change in frequency applications

- **R3**, **R4**, **R0**
- **[R4]**, **[R1]**, **R0**

After initialization, to change output frequency, write registers in this order:

- After initialization, to change output frequency, write registers in this order:
  - [R4], [R1], R0
  - R4 only required if MOD changed.

### Prescaler
**ADF4350:** If the input to the prescaler is >3 MHz, use 8/9 prescaler.

**ADF4351:** If the input to the prescaler is >3.6 MHz, use 8/9 prescaler.

**Fundamental/Divided feedback** (R4, DB23) will change the prescaler input frequency. For example, when the output frequency is 2195 MHz, the VCO fundamental output is actually 4390 MHz. If Fundamental feedback is used, 8/9 prescaler must be used. Alternatively, Divided feedback must be used so the prescaler input will be 2195 MHz.

When using 4/5 prescaler, the minimum N value is 23. When using 8/9 prescaler, the minimum N value is 75.

### Phase Noise and Loop Filter

**Phase noise from the reference source.** Reduce by using a lower phase noise reference source.

**Phase noise from the phase detector, charge pump, and the loop filter.** Reduce phase noise from phase detector and charge pump by maximizing PFD frequency.

**Loop Filter Bandwidth:** Changing the loop filter bandwidth will change the dynamic response of the loop. Optimize profile using ADIsimPLL for application’s phase noise/ jitter requirement.

Lower in-band phase noise

Faster set-up time

### RFout Relationship
**RFoutA** is a differential signal; that is, **RFoutA~** is 180° relative to **RFoutA+**.

**RFoutB** is the same as **RFoutA**, except delayed 80 ps, regardless of frequency.

### Output Frequency Error
Any offset in the reference source will be multiplied by N, and appear as an offset at the output. Register settings may be incorrect. Use evaluation board control software to generate register values.

### Powerdown
**Hardware powerdown (CE pin)** or software powerdown (R2, DB5) will retain register contents.

Powerdowning the **AVDD** and **DVDD** pins will lose register contents.

**Low Spur Mode**

- **When using Low Spur Mode, MOD must be 50 or greater.**

### Support
For further support, follow the EngineerZone® link below.

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### Links

- **ADIsimPLL**: http://www.analog.com/adisimpll
- **ADF4350 product page**: http://www.analog.com/ADF4350
- **ADF4351 product page**: http://www.analog.com/ADF4351
- **EngineerZone® support forum**: http://ez.analog.com/community/RF
- **ADF4350 and ADF4351 evaluation board files (including gerber files)**: http://ez.analog.com/message/155240
- **ADF435x evaluation board control software and source code**: http://ez.analog.com/message/38857

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**PFD Frequency and Channel Spacing**

The minimum channel spacing is set by:

\[ f_{PFD} / MOD \]

where \( f_{PFD} \) = PFD frequency (maximum: 32 MHz in fractional-N modes);

\( MOD = R1, DB[14:3] = 2 \) to 4095.

Example: \( f_{PFD} = 32 \) MHz; \( MOD = 4095 \); channel spacing = 7.8 kHz.

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**Charge Pump Current**

Increasing the charge pump current will increase the loop bandwidth. Decreasing it will decrease the loop bandwidth. ADIsimPLL™ shows the effect of changing the charge pump current.

It is recommended to design the loop filter at the middle charge pump current (2.5 mA), and then, after soldering the loop filter components, tweak the charge pump current to get the desired loop filter dynamic.

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**Phase Resync**

When using phase resync, use Divided feedback (R4, DB23 = 0).

Set Clock Divider Value (R3, DB[14:3]) so that:

\[ CLK \text{ Div} = MOD \times \text{PFD settling time} \]

**Phase Adjust (ADF4351 only)**

When Phase Adjust (R1, DB28) is enabled, writing to R0 will increment the output phase by:

\[ \text{Phase Value (R1, DB[26:15])} \times 360 \degree / \text{MOD (R1, DB[14:3])} \]

relative to the current phase.

If FRAC = 0, RS DB[18:15] must be set to 0b0100.

Do not use Phase Adjust and Phase Resync together.

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**FRAC/MOD Reduction**

When the FRAC/MOD fraction can be reduced, it is recommended to do so. Doing so will reduce fractional spurs by reducing the MOD value.

\[ \frac{FRAC (R6, DB[14:3])}{MOD (R1, DB[14:3])} \]

can be reduced to \( \frac{25}{100} \).

Use caution when using Phase Adjust or Low Spur Mode, as both use the MOD value.

This reduction is enabled by default in the evaluation board control software, but can be disabled in the Tools menu.

**Evaluation Board**

- Do not use N counter to Muxout setting during band select process (writing to R0). Enable N counter to Muxout after output has locked to new band.

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**Muxout**

- **Do not use N counter to Muxout setting during band select process (writing to R0). Enable N counter to Muxout after output has locked to new band.**

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**Support**

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