Design Development of Low Offset High Speed CMOS Voltage Comparator

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ABSTRACT

In today's world, where demand for portable battery-operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high-speed applications. In this high-speed low power, low voltage era there is an increasing demand of a High-Speed Comparator for ADC, DAC and various applications in analog and digital domain. Various types of dynamic latch comparators such as resister dividing comparator, current sensing comparator and charge sharing latch comparator are used for high speed application. The fully dynamic latch comparator Lewis-Gray structure is simulated in different technologies with different characteristics like propagation delay, ICMR and offset voltage for low offset high speed. A Rail-to Rail high speed comparator is simulated for power offset, propagation delay and input common mode range in different CMOS technologies. Generally, NAND latch are used in most of the comparator in literature; in proposed comparator NOR base latch is used and two separate Clk1 and Clk2 are used which results in low offset voltage and low propagation delay at the cost of small increase in power dissipation as compare to the conventional Lewis Gray comparator. Simulation are done in 180 nm and 90 nm CMOS technology which shows that proposed comparator gives low propagation delay and low offset voltage compare to the conventional Lewis Gray comparator at the cost of small increase in power dissipation.

Keywords:
Comparator, Open Loop Comparator, Rail-to-Rail Comparator, Lewis Gray comparator, Low Power Low Offset Dynamic Comparator

I. INTRODUCTION

The schematic symbol and basic operation of a voltage comparator as shown in Figure 1, this comparator can be thought of as a decision-making circuit.

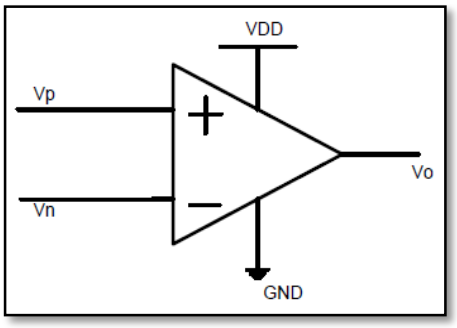


Figure 1. Circuit Symbol for a Comparator

The comparator is the circuit which compares an analog signal with another signal or reference signal and gives outputs a binary signal based on the comparison. VP is the positive input voltage applied to the positive terminal of comparator and VN is the negative input or reference voltage applied to the negative terminal of comparator. If positive input voltage of the comparator VP, is greater value than the VN, which is negative input voltage then comparator output is at logic '1' where as if negative input voltage of the comparator VN, is greater value than the VP, which is positive input voltage at potential less than VN then comparator output is at logic '0' [21, 22].

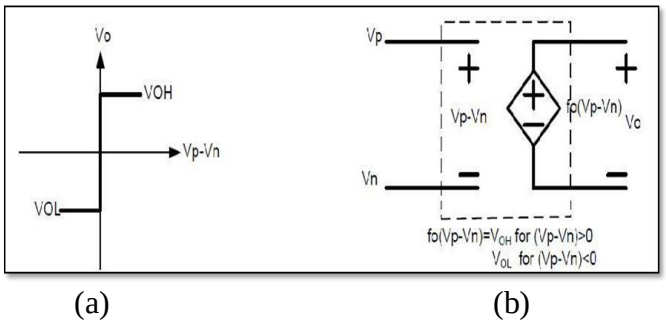
$$\text{If } V_P \geq V_N, \text{ then } V_o = \text{logic'1'} \text{ -------(1)}$$

$$\text{If } V_P \leq V_N, \text{ then } V_o = \text{logic'0'} \text{-------(2)}$$

Here an analog signal is mean one of that signals which can have any one of a continuous time of amplitude values at a given point in time. In the strictest sense a binary signal can have only one of two given values logic 1 or logic 0 at any point in time, but this concept of a binary signal is too ideal for real world situations, where there is a transition region between the two binary states. It is essential for the comparator to pass quickly through the transition region. The comparators can be divided into this type of structure, open-loop and regenerative comparators. The open- loop comparators basically op-amps without compensation. Regenerative comparators use positive feedback, like sense amplifiers or flip-flops, to accomplish the comparison of magnitude between two signals. A third type of comparator emerges that is an arrangement of the open-loop and regenerative comparators. This arrangement results in comparators that are extremely fast [22].

1.1 Static Characteristics

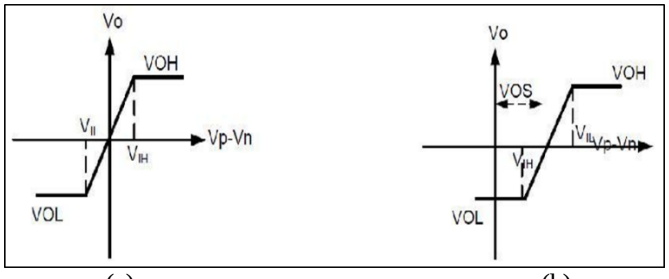
A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is shown in Figure 1. The output of comparator is high (VOH) when the difference between the non-inverting and inverting inputs is positive, and low (VOL) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Figure 2 comprise a Voltage Controlled Voltage Source (VCVS) whose characteristics are described the mathematical formulation given on the Figure 2.



(a) (b)

Figure 2. (a) Ideal Transfer curve of a Comparator (b) Model for an Ideal Comparator

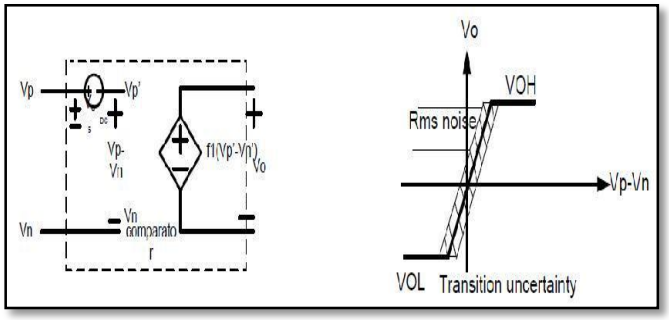
Gain: The gain of the comparator is the derivative of the dc transfer curve at VI ~ VR. The transfer curve of an ideal comparator with infinite gain is as shown in Figure 2. The second non-ideal effect seen in comparator circuit is input offset voltage, VOS. In Figure 2 the output changes the input difference crosses zero. If the output did not change until reached a value +VOS then this difference would be defined as the offset voltage. This would be a problem if the offset could be predicted, but it varies randomly from circuit to circuit for a given design. Figure 3 (a) illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Figure 3 (b). The sign of the offset voltage accounts for the fact that VOS unknown in polarity.



(a) (b)

Figure 3. (a) Transfer curve of Comparator with Infinite Gain (b) Transfer curve of a Comparator including Input-Offset Voltages

In addition to above characteristics, the comparator can have a differential input resistance and capacitance and the output resistance. All these aspects can be modeled in the same manner as was done for the Op-amp. Because of the comparator is usually differential, the input common mode range is also important. The ICMR for a comparator would be that range of input common mode voltage over which the comparator functions normally. This input common mode range is generally the range where all transistor of the comparator remains in saturation. Even through the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modeled as if the comparator were biased in the transition region of the voltage transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Figure 4. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.



(a) (b)

Figure 4 (a) Model for a Comparator including Input-Offset Voltage. (b) Influence of Noise on a Comparator

1.2 Dynamic Characteristics

The dynamic characteristics of the comparator include both small signal and large signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristics delay between input excitation and output transition is the time response of the comparator. Figure 5 illustrates the response of a comparator to an input as a function of time. Note that there is a delay between the input excitation and the output response. This time difference is called the propagation delay time of the comparator. It is a very important parameter since it is often the speed limitation in the conversion rate of an A/D converter. The propagation delay time in comparators generally varies as the function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which further increase in input voltage will no longer affect the delay. This mode of operation is called slewing or slew rate. The small-signal dynamics are characterized by the frequency response of the

comparator. A simple model of this behavior assumes that the differential voltage gain, AV, is given as,

$$Av(s) = \frac{Av(0)}{\frac{S}{Wc}+1} = \frac{Av(0)}{S\tau c+1} \text{ ---------(3)}$$

Where AV (0) is dc gain of the comparator, and Wc = 1/τc is the -3 db frequency of the single (dominant) pole approximation to the comparator frequency response.

Normally, the AV (0) and Wc of the comparator are smaller and larger, respectively, than for an op-amp.

Let us assume that the minimum change of voltage at the input of the comparator the resolution of the comparator. We will define this minimum input voltage to the comparator as

$$V_{in(min)} = \frac{V_{OH} - V_{OL}}{Av(0)} - - - -(4)$$

For a step input voltage, the output of the comparator modeled by equation 3 rises (or falls) with a First-order exponential time response from VOL to VOH (or VOH to VOL). If Vin is larger than Vin (min), the output rise or fall time is faster. When Vin (min) is applied to the comparator, we can write the following equation:

$$\frac{V_{OH} - V_{OL}}{2} = Av(0)\left[1 - e^{\frac{T_p}{T_c}}\right] Vin$$

$$= Av(0)\left[1 - e^{\frac{T_p}{T_c}}\right](V_{OH} - V_{OL})/Av(0))\text{----- (5)}$$

Therefore, the propagation delay time fosssr an input step of Vin(min) can be expressed as,

$$t_p(max) = \tau_c \ln 2 = 0.693\ \tau_c \text{ ------ (6)}$$

This propagation delay time will be valid for either positive – going or negative-going comparator outputs. The propagation delay time is given as

$$t_{p=}\ \tau_c \ln\frac{2k}{2k-1} \text{ --------(7)}$$

Where $k = (\frac{V_{in}}{V_{in(min)}})V_{in}$

Obviously, the more overdrive applied to the input of this comparator, the smaller the propagation delay time. As the overdrive increases to the comparator eventually the comparator enters a large signal mode of operation. Under large-signal operation, a slew-rate limit will occur due to limited current to charge or discharge capacitors.

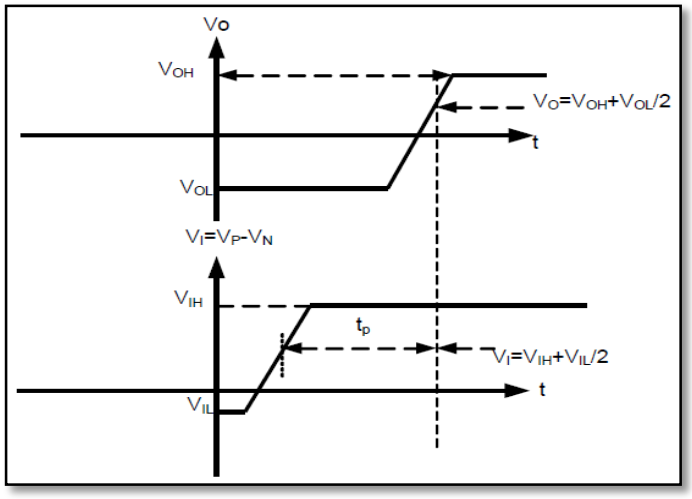


Figure 5. Propagation Delay Time of a Non-Inverting Comparator

The offset can be minimized or ignored by proper layout. If the input step is sufficiently small the output should not slew the transient response will be a linear response. The settling time is the time needed for the output to reach a final value within a predetermined tolerance, when excited by a small signal. Small-signal settling time is determined by the gain bandwidth product of the amplifier; this will be shown in the op-amp circuit section later. If the input step magnitude is sufficiently large, the comparator will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitance. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. Slew rate is limited by the current sourcing/sinking capability in charging the output capacitor. Settling time is important in analog signal processing. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.

II. EXISTING ARCHITECTURES OF COMPARATOR AND ITS ANALYSIS

A widely used ADC architecture for dynamic comparator is called 'Lewis Gray' dynamic comparator. The main advantages of this comparator are its low power consumption or no DC power consumption. This comparator is same as all the single-phase comparators which comprising a preamplifier stages and cross coupled latch. In this both stage which is operate as asynchronously and simultaneously when this dynamic comparator in evaluation phase [11].

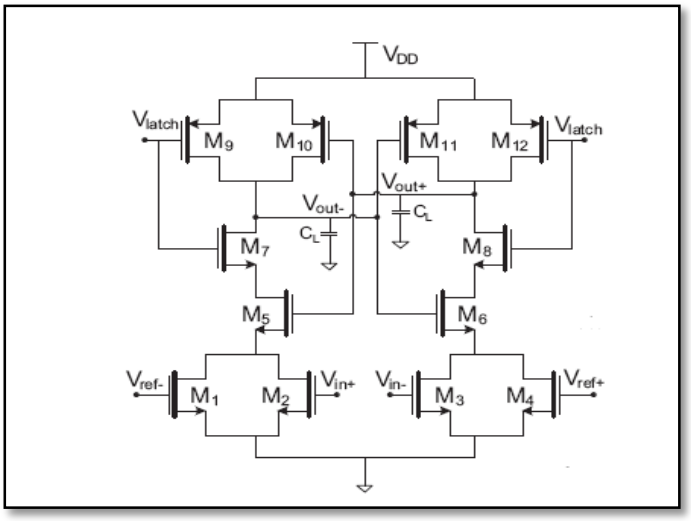


Figure 6. 'Lewis Gray' Comparator

The circuit operation is like this where in this circuit the input transistors Vin+, Vin-, Vref+, Vref-, operate in the triode region and act like a voltage-controlled resistor, so that this comparator is also called 'Resistor Divider Comparator'. Now in this circuit where in reset phase when the (Vlatch=0V), so M9 to M12 PMOS transistors are reset and charge up and the Out node is going up to VDD. At that time the NMOS transistors M5 and M6 on and the node voltage at the VD5,6 discharge to ground. Same as when transistor M1 and M2 discharge to ground while NMOS transistor M7 and M8 are off [23].

Now during the evaluation phase where control signal goes up (Vlatch=VDD), where the operation regions of the entire transistor are well defined. Input transistor M1 to M4 connecting to the input and reference voltages are in the triode region and act like a voltage-controlled resistor. If no mismatch is present the comparator changes its output when the conductance of the left and right input branches is equal gL = gR.

$$V_{in}\,(threshold) = \frac{W_B}{W_A} V_{ref} - - - (8)$$

Where $W_A=W_2=W_3$ $W_B=W_1=W_4$

$V_{in}=V_{in+} - V_{in-}$ $V_{ref}=V_{ref+} -V_{ref-}$

Where M10 and M11 both PMOS transistors have equal drain and gate voltage, which make them both work at saturation region. Transistors M7 and M8 work as switches in cross-coupled transistor pairs including M5M10 and M6M11, this all are turned on during comparison stage and also working in the triode region because of its high gate voltage Vg7,8 = VDD. The drain voltage of M5 and M6 is pulled up closed to Vout+ or Vout- and works in saturation because switches M7 and M8 are in the triode region. Transistors M9 and M10 are both turned off because control signal Vlatch is VDD, which indicates that mismatch effects in M9 and M12 is negligible [11]. The offset of the comparator depends on the mismatch of the transistor M1-M4. This is true only when all other transistors M5-M12 are assumed to match perfectly. Since during the evaluation phase the input transistors M1 to M4 are operate in linear region, so the transconductance of this both transistors is approximately written as by this equation:

$$g_{m1.2.3.4} = \mu_n C_{ox} \left(\frac{W_{1,2,3,4}}{L}\right) V_{ds1,2,3,4} - - - (9)$$

Also, during evaluation phase transistors M5 and M6 are operated in the saturation region, for those transistors the transconductance can be written as:

$$g_{m5,6} = \mu_n C_{ox} \left(\frac{W_{5,6}}{L}\right) (V_{ds5,6} - V_t) - - - (10)$$

The transconductance of the this transistor M5 and M6 is very larger than the M1 to M4 input transistor pairs, hence the differential voltage gain built from the input transistor pair is not big enough to overcome an offset voltage caused from such a mismatch between transistor pair M5 and M6. For that the result of these transistors are the most critical mismatch pair in this dynamic comparator also needed to the big enough size to minimize the offset voltage at the cost of the increased power consumption. So, it can be concluded that the zero-static power consumption and threshold voltage adjustable as advantages, so in, Lewis Gray comparator for mismatch sensitivity this can be avoided by adding an extra latch or inverters as a buffering stage after the comparator core outputs.

III. LOW OFFSET HIGH SPEED COMPARATOR

The circuit operation is like this where reset phase when the Clk1 and Clk2 both are low, so PMOS transistors M11, M12, M13 and M14 on and NMOS transistor M5 and M8 are off, and both output nodes are precharges to VDD.

Now during the comparison phase where Clk1 goes to high and Clk2 still at low, where the operation region of the all transistor are well defined. PMOS transistors M11 and M12 are off and NMOS transistor M5 and M8 are on. PMOS transistor M13 and M14 on because of Clk2 is low. During the phase when the comparator is not making decision when Clk1 and Clk2 is low. This will ensure that all the internal nodes are reset before the comparator goes into the decision mode.

Drain voltage of M1, M2, M3 and M4 are high at VDD supply and the difference between the amounts of current produce in input branches is related to the voltage difference between the input and reference. The latch circuit is operating and induced differential voltage is compare and gives the output.

Generally NAND latch are used in most of the comparator in literature; in proposed comparator NOR base latch is used and two separate Clk1 and Clk2 are used which results in low offset voltage and low propagation delay at the cost of small increase in power dissipation as compare to the conventional Lewis Gray comparator.

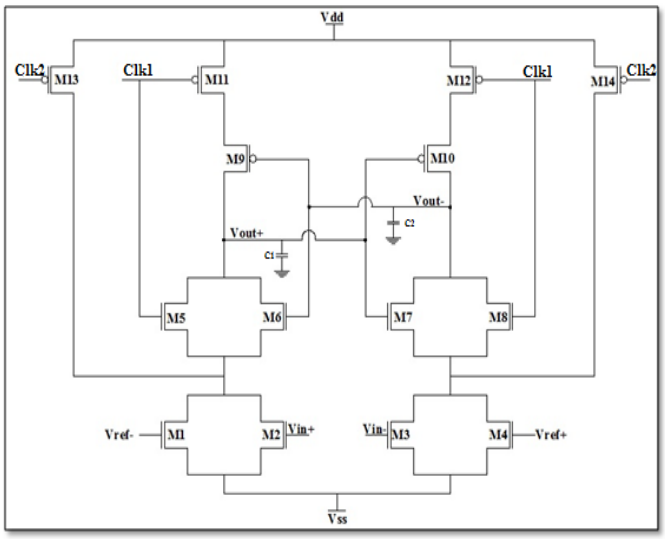


Figure 7. Low Offset High Speed Comparator

a. Designing of Low Offset High Speed Comparator

In Table 1, different voltage values are given for supply voltage VDD and Vss, Clk1 and Clk2 signal, input voltages Vin+ and Vin- and reference voltages Vref+ and Vref-.

Table 1. Different Voltage Values for Different Technology

Voltage Terminals	Technology	
	180 nm	90 nm
V_{DD}	1.8V	0.9V
Vss	-1.8V	-0.9V
Clk_1	1.8V	0.9V
Clk_2	-1.8V	-0.9V
V_{in+}	1.8V	0.9V
V_{in-}	-1.8V	-0.9V
V_{ref+}	0.9V	0.45V
V_{ref-}	-0.9V	-0.45V

IV. SIMULATION RESULT

To verify its operation and the consistency with the analytical derivations including delay, offset ICMR, frequency response and input –output noise spectral density. The circuit operates from a ± 0.9V power supply. The simulation results shown in Fig. -8 to 15.

a. Simulation Results of Simulation Result for 180nm Technology

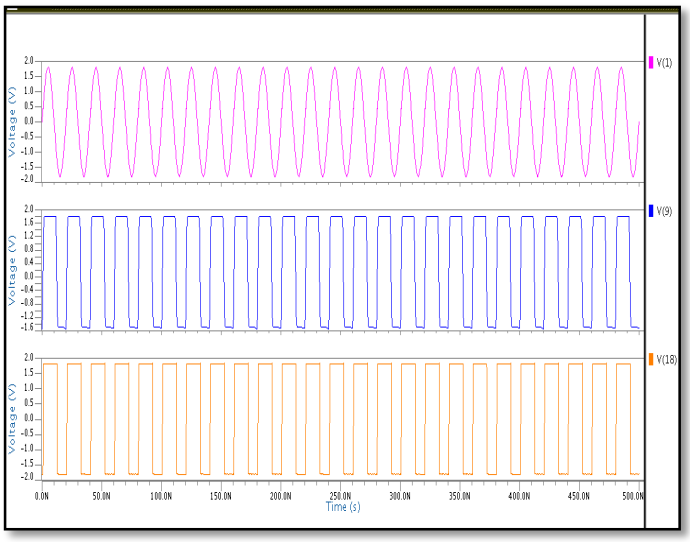


Figure 8. Input as Sin wave

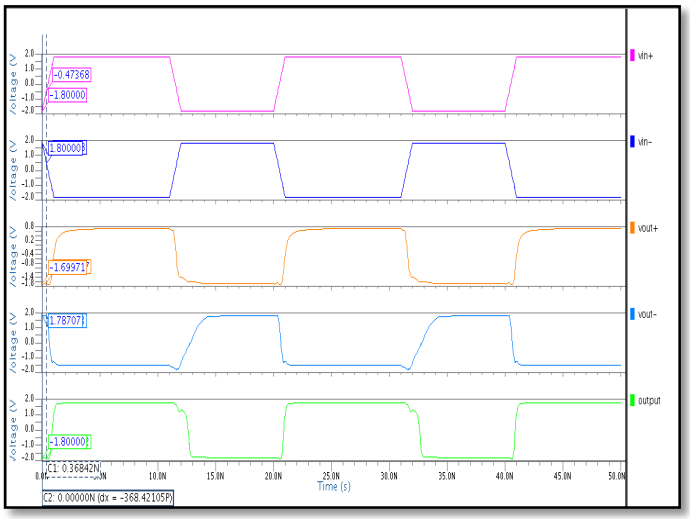


Figure 9. Transient Response

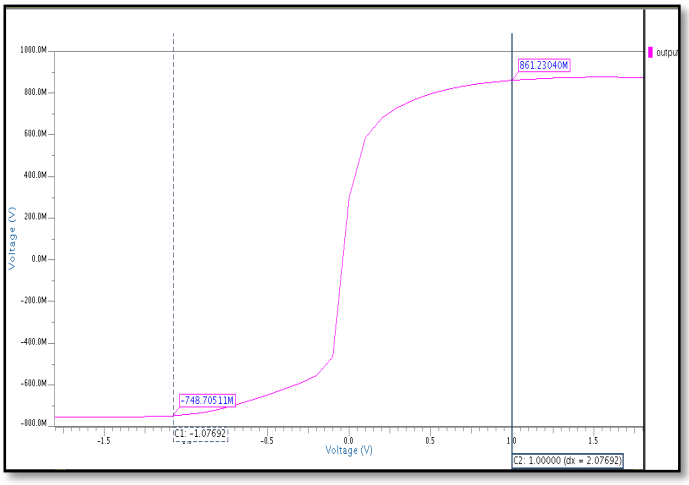


Figure 10. Input Common Mode Range

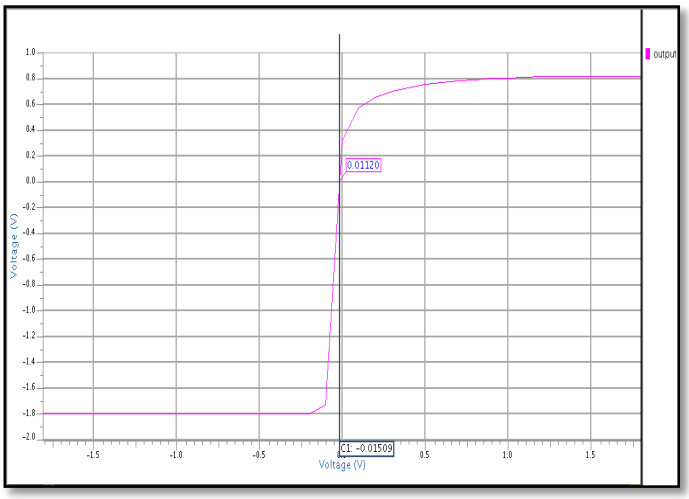


Figure 11. Offset Voltage

b. Simulation Results of 90 nm Technology

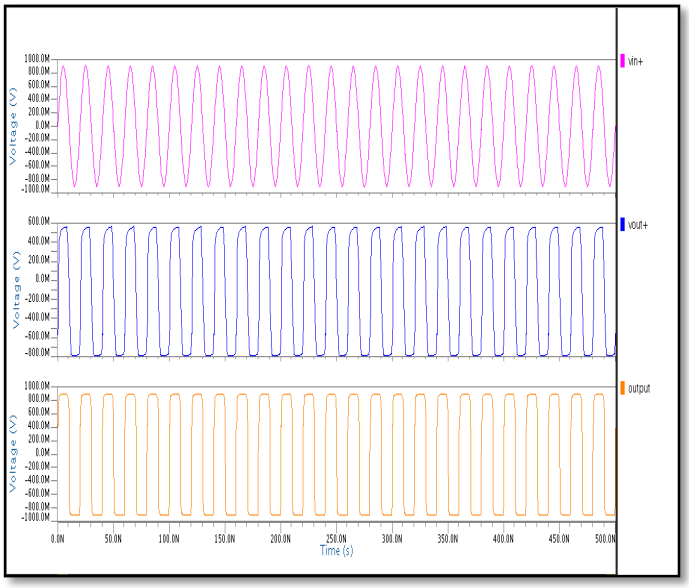


Figure 12. Input as Sin wave

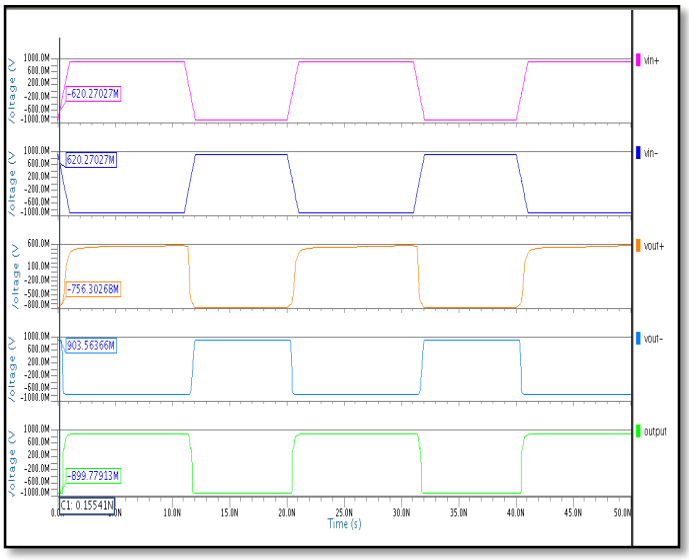


Figure 13. Transient Response

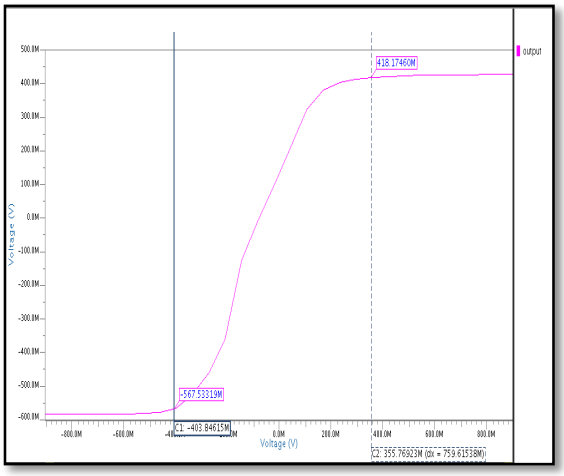


Figure 14. Input Common Mode Range

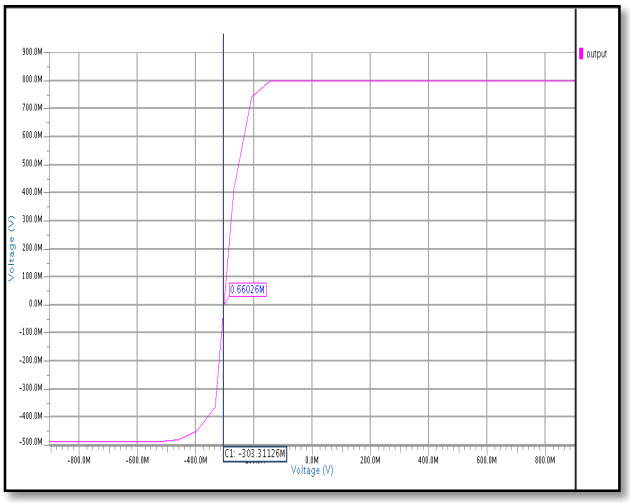


Figure 15. Offset Voltage

Table 2. Comparative Analysis of Different Architectures of Voltage Comparator in 180 nm Technology

Parameter	Lewis Gray Comparator	Rail to Rail High Speed Comparator	Low Offset High Speed Comparator
Propagation Delay (ns)	0.473	0.684	**0.368**
ICMR (V)	-1.3 to 0.56	-0.68 to 0.21	-1.07 to 1
Offset Voltage	21.30 mV	105 mV	11.20 mV
Power Dissipation	0.238 mW	26.43 nW	1.27 mW

Table 3. Comparative Analysis of Different Architectures of Voltage Comparator in 90 nm Technology

Parameter	Lewis Gray Comparator	Rail to Rail High Speed Comparator	Low Offset High Speed Comparator
Propagation Delay (ns)	0.270	0.486	0.155
ICMR (V)	-0.4 to 1.03	-0.79 to 0.74	-0.4 to 0.35
Offset Voltage	9.20 mV	4.48 mV	0.66 mV
Power Dissipation	3.508 µW	8.05 µW	2.69 mW

V. CONCLUSION

The comparator architectures are characterized in terms of Propagation Delay, ICMR, Offset and Power Dissipation. The simulation result allows the circuit designer to fully explore the tradeoffs in comparator design; such as offset voltage, speed, power for A/D converters. Different types of comparator architectures in which pre-amplifier is used before the comparator to reduce the input offset voltage, but it also increases the power consumption. Therefore, the latched comparator is good alternative for lower power consumption and high-speed operation. A Rail-to Rail high speed comparator for low power low offset dynamic comparator simulated for different characteristics of comparator in terms of propagation delay, offset voltage, and input common mode range. Generally, NAND latch are used in most of the comparator in literature; in present comparator NOR base latch is implemented and two separate Clk1 and Clk2 are used which results in low offset voltage and low propagation delay. Simulation are done in 180 nm and 90 nm CMOS technology which shows that present comparator gives low propagation delay and low offset voltage compare to the conventional Lewis Gray comparator at the cost of small increase in power dissipation

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