Design And Analysis of Low Power High Speed and AreaEfficient Dynamic Comparators for Future ADC'S

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Abstract: In this system presents a low power dynamic comparator for ultra-low power applications. The prototype is designed in an 18nm CMOS process with a supply voltage of 5V and is compared against the widely used double tail latch comparator in terms of power consumption and input referred RMS noise. The addition of cross-coupled devices to the input differential pair prevents the comparator internal nodes from fully discharging to ground in contrast to the conventional architecture. This reduces the power consumption while achieving similar noise levels. Dynamic comparators are the essential building block in many mixed signal conditioning circuits. The widespread use of battery powered applications demands low power signal processing circuits, resulting in the widespread use of dynamic comparators. Strong-arm latch type dynamic comparators and its variants are widely used owing to their negligible static power consumption.

Index Terms—Analog-to-digital converter (ADC), comparator, double-tail latch-type comparator, latch, low-noise, low-power, SAR, Strong Arm.

I. INTRODUCTION

The latch-based dynamic comparator is a crucial module in analog-to-digital converters (ADC), high-speed digital I/O circuits, memory sensing amplifiers and analog built-in-self-testing (BIST) circuits. Compared with static comparators, dynamic comparators utilize positive feedback and dynamic bias; therefore, have higher speed and lower static power consumption .The conventional single-stage dynamic comparators directly stack the input transistors with the cross-coupled latch circuit; hence, they require large voltage head room. Moreover, they suffer from severe kickback noise introduced by the capacitive paths from the output nodes to the input nodes, and there is a challenging trade-off between speed and power consumption. Several design techniques for low- voltage, low-power dynamic comparators have been reported, including the charge-steeringtechnique, techniques using body-driven transistors, and supply boosting methods. As an alternative, the two-stage dynamic comparator topology employs a fully dynamic preamplifier as the input stage, which is separated from the latching stage. This structure has less stacking, so it is more suitable for low-voltage operation. In addition, it reduces the kickback noise by providing additional shielding between the input and the output and enables independent optimization of theinput stage (which mainly affects the off-set) and latching stage (which mainly affects the speed).

II. RELATED WORK

Several modified two-stage comparators have been reported to achieve faster speed and lower power consumption. In, positive feedback is introduced in the preamplifier of the two-stage comparator to strengthen the regeneration, which reduces the delay. However, it suffers from higher kickback noise than the conventional two-stage comparator. The latch is activated with anintentional delay to reduce power consumption. However, it suffers from a larger required area and higher kickback noise. The two-stage comparator in employs a dynamic bias preamplifier, which only partially discharges the internal nodes and reduces the energy consumption. However,its delay is larger than that of the conventional structure. An additional positive feedback and a special clocking pattern are used in the preamplifier to improve the preamplifier gain.

In SAR ADCs targeted for ultra-low power applications the comparators play a crucial role. Typically 40-50% of the total SAR ADC energy consumption is by the comparator alone. A widely used double tail latch type comparator is shown in Fig. 1. The timing diagram associated with this comparator is shown in Fig. 2. For each comparison, the pre-amplifier output (intP and intN) node capacitors (Cp) discharge completely to ground and afterwards they have to be re-charged to the supply, VDD. The time to discharge the capacitors, Cp from VDD to the voltage, Vlatch determines the integration time, Tint. Vlatch is the voltage at which the regenerative latch triggers i.e. low enough to turn the transistors M11 and M12 on to provide the conduction path

for the regenerative latch. Once the latch triggers, further reduction of the node voltages intN and intP is not going to improve the noise or conversion time but it will cost more energy to reset these nodes to VDD. In order to save the power, ideally we would stop the discharge of these nodes immediately after the latch triggers. Conventional architectures fail to do this and allow Cp to discharge completely to ground as shown in Fig. 2. This means a fixed charge of Cp*VDD is required at each of the nodes, intP and intN. Thereby consuming the energy 2*Cp*VDD 2 for every comparison. As a result of this, the preamplifier consumes almost 70-80% of the total comparator energy. Ideally this pre-amplifier energy consumption would reduce to VDD*Cp*2*(VDD-Vlatch). However, this implementation requires extra headroom and a degenerative capacitor increases the comparison time. The floating inverter pre-amplifier based comparator architecture uses a reservoir capacitor to reduce the energy consumption the cost of this is larger circuit area and the need for a higher supply voltage.

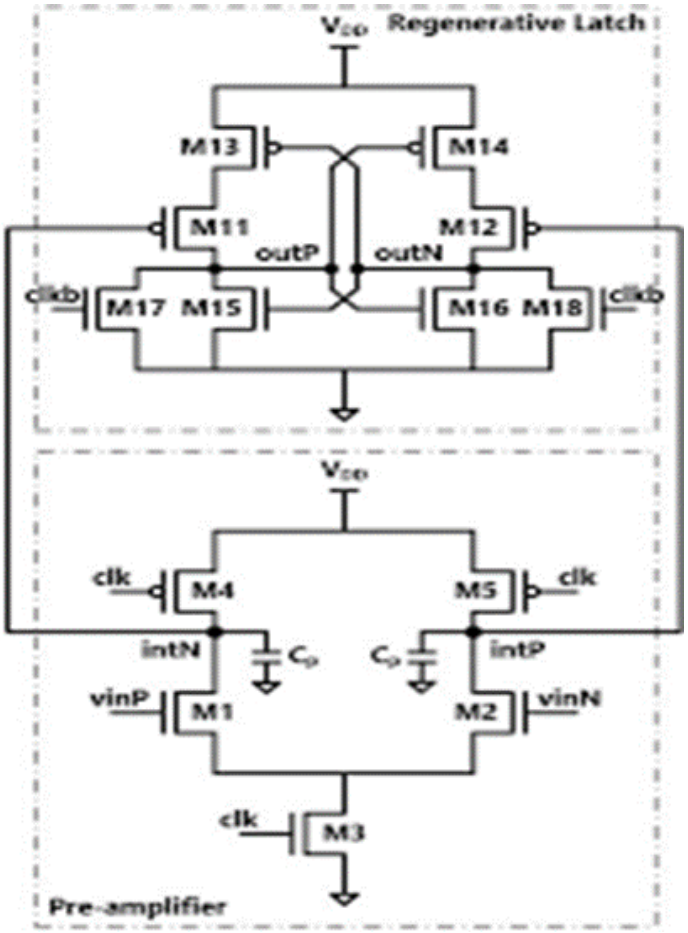

Fig. 1. Conventional double tail latch type comparator schematic.

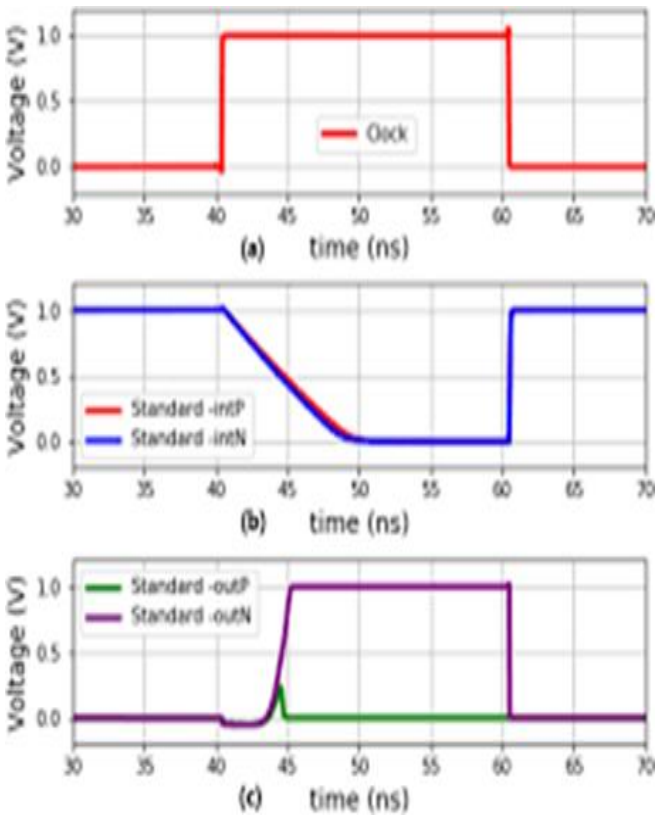

Fig. 2. Simulated timing diagram of a conventional comparator

Drawbacks:

- Need more capacitors.
- More power consumption.
- High cost

III. PROPOSED SYSTEM

This paper presents a comparator architecture to reduce the power consumption without the use of any extra capacitors or complex logic but with a simple cross coupled mechanism around the input differential pair. This technique prevents the comparator internal nodes from discharging fully for small differential inputs and thus reducing the energy consumption per each comparison.

The proposed comparator architecture is shown in the Fig. 3. It consists of a new modified pre- amplifier with the addition of the cross coupled devices (M21 and M22) and a regenerative latch. The operational behavior

of the proposed comparator circuit is explained as follows. During the reset phase, when the applied clock is low, the transistors M4, M5, M6 and M7 pre-charge the nodes intN, intP, N1 and P1 to VDD and the transistors M17 and M18 reset the regenerative latch output nodes (outP and outN). As the transistor M3 is turned off, there is no direct flow of current from the supply to ground. During the amplification phase, when the clock is high, the nodes intP, intN, P1 and N1 are disconnected from VDD and M3 provides a discharge path to ground. The amplification phase can be divided into two sub-phases.

At the instant that amplification starts, as the gates of M3 and M21 are tied to VDD, the node N1 quickly gets discharged to a low voltage which is the IR drop across the switches (M3 and M21). The node P1 behaves in a similar manner. Once the transistors M1 and M2 start conducting and M21 and M22 operate in the linear region (i.e as resistors). As the voltage at nodes intP and intN decrease, at a rate controlled by the applied input voltages, the internal node N1 and P1 voltages will increase slowly. This behavior changes the effective Vgs of the input differential pair lowering the trans-conductance (gm). For small input differential voltages, this behavior can increase the conversion time of the comparator. Based on the applied input differential voltage (vinP>vinN), the rate of decrease of the node intN is faster than the node intP. As the node intN reaches to the threshold voltage of M22, the rate of decrease of the node intP reduces and eventually intP will become static as transistor M22 turns off completely. With the node intP static, the operational behavior of the circuit changes.

IV. RESULTS & DISSCUSSION

Both the existing and proposed works are designed in s-edit and the waveforms are generated by T-spice in Tanner EDA tool.

Existing System:

A widely used double tail latch type comparator is designed. For each comparison, the pre- amplifier output (intP and intN) node capacitors (Cp) discharge completely to ground and afterwards they have to be re-charged to the supply, VDD.

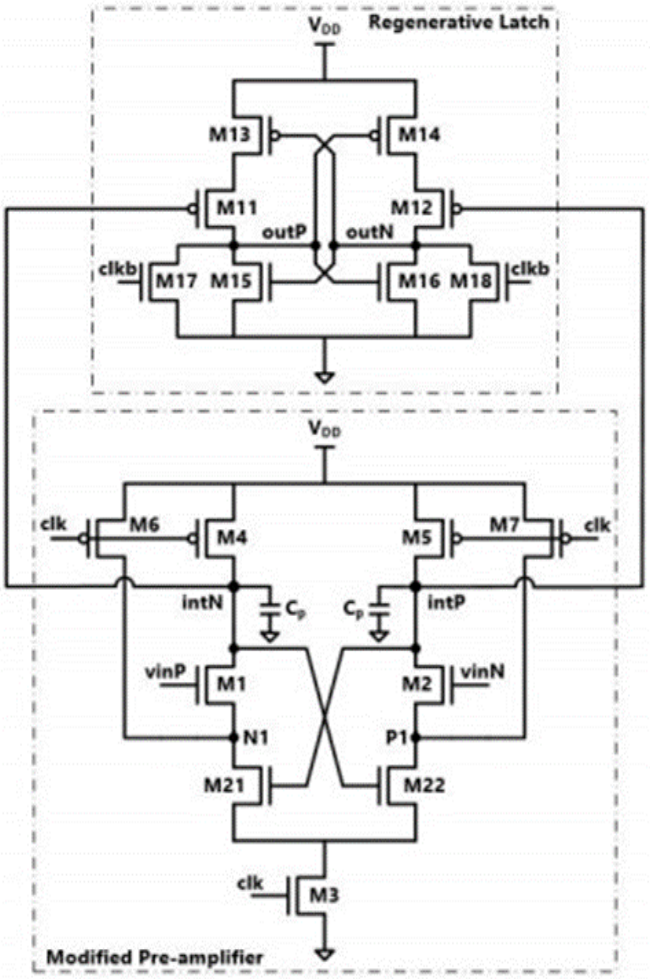

Fig3:- Proposed comparator schematic with the modified pre-amplifier and the regenerative latch.

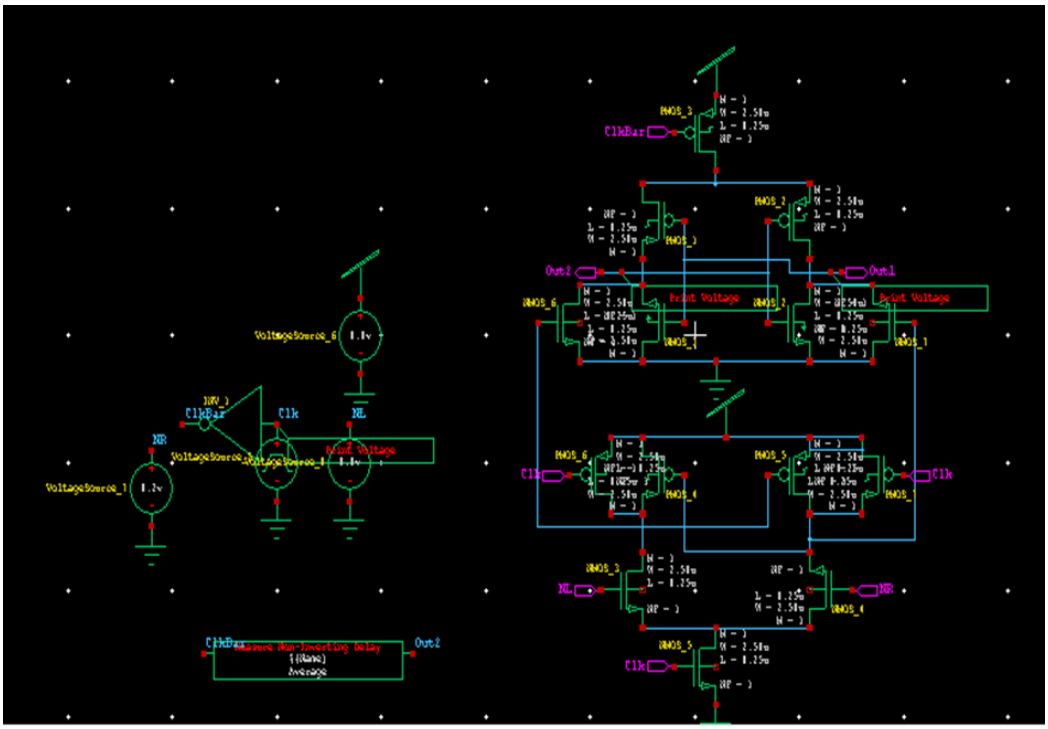

Fig 4: Schematic design of Existing method

Waveform:

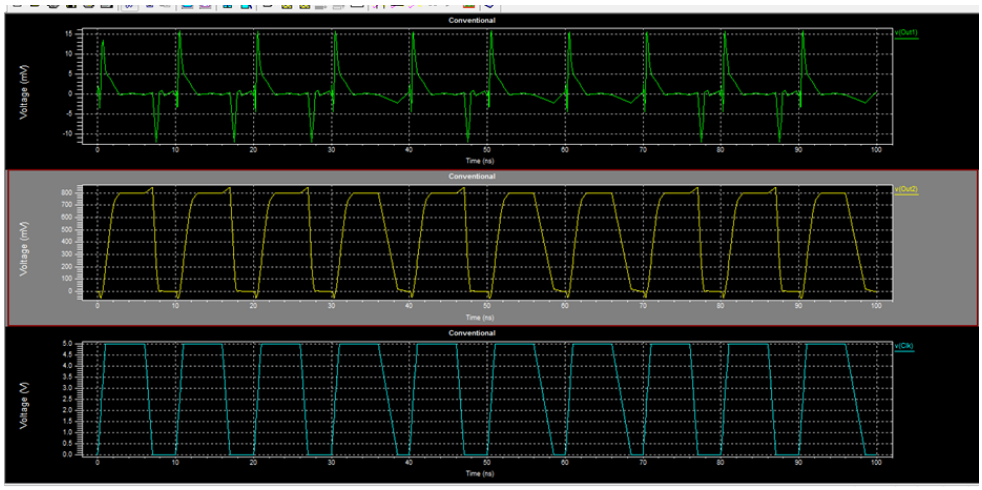

Fig 5: Waveform for existing method

Proposed System:

Proposed comparator schematic with the modified pre-amplifier is designed and design is run at1v supply voltage and the waveforms are verified.

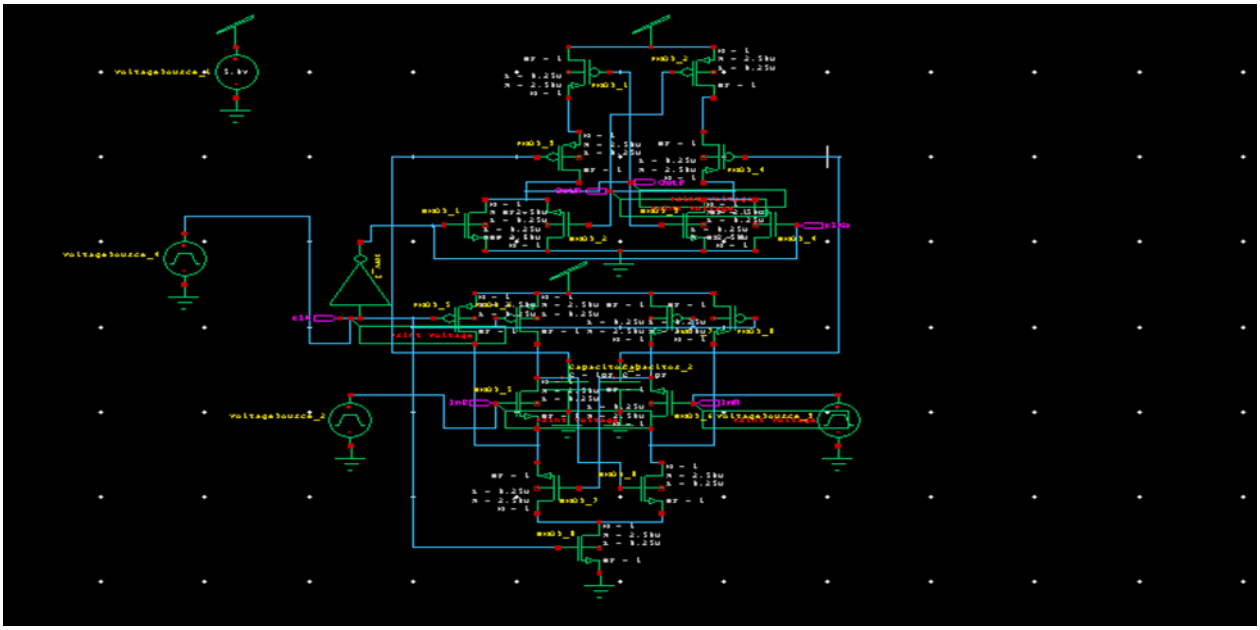

Fig 6: Schematic of Comparator schematic with the modified pre-amplifier

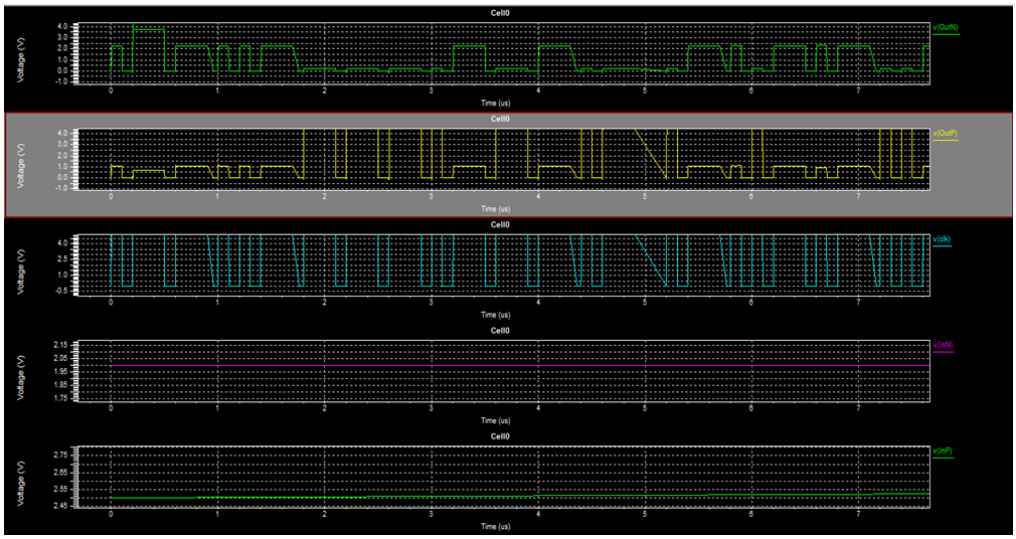

Fig 7: Waveform of Proposed System

The Average power consumption is reported in below table

Table 1: Comparison Table of power consumption

Methods	Average Power Consumption (mW)
Existing system	49.52
Proposed System	25.69

V. CONCLUSION

In conclusion the proposed comparator presented here achieves about reduction in measured power compared to the conventional comparator at a similar noise levels. This is achieved by only partially discharging the comparator internal nodes with the use of a simple cross-coupled mechanism. This makes the presented architecture a good design choice in ultra-low power applications. The proposed circuit is also a low area solution as it does not require any external capacitors or complex logic.

VI. REFERENCES

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