# Design and Optimization of 4-Bit ALU using FINFETS and CNTFETS for Nano Scale Technology

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***Abstract-*** This work aimed to develop low energy, low average power and low delay circuits. Here we are using the CNTFET for making these circuits in ALU and these circuit is compared to ALU FinFET circuits. The CNTFET having major role in electronics industry and these used to make different kind of electronics devices. The principle purpose for is the element of CNT in nanometer measure. The one of the fundamental highlights is edge voltage which are accustomed to making parallel adder circuits. CNTs would be a promising contender for future Nano-scale transistor gadgets. In addition, on account of the absence of limits in the ideal and empty chamber structure of CNTs, there is no limit dissipating. CNTs are likewise semi 1D materials in which just forward dissipating and back dispersing are permitted, and versatile dissipating implies that freeways in carbon nanotubes are long, ordinarily on the request of micrometers. In this work, the average power and delay of the system is improved by the use of CNTFET and is better than FinFET in 4-bit ALU.

***Keywords-*** carbon nanotube field-effect transistor, Fin Field Effect Transistor, Nano-scale transistor gadgets, ALU, Power, delay.

## I. INTRODUCTION

In VLSI innovation, constant scale down of the transistor demonstrates the Moore's law which depicts the transistors set in a chip copies in at regular intervals. As MOS transistors sizes scales down, difficulties and impediments additionally twofold in each contracting of the transistors, for example, short channel impacts and subthreshold voltage varieties and so forth [1]. It additionally a mix of rationale squares to play out the logical or arithmetic tasks. Presently a day's ALU is getting increasingly perplexing and littler in size to make the advancement of littler and most dominant PC frameworks. This undertaking structures An ALU utilizing MOSFET as a traditional strategy. In traditional ALU expends a lot of intensity and furthermore comprise a few confinements amid downsizing, for example, short channel impacts, gate dielectric spillage and so on. The ALU planned with a FINFET [2]. In any case, as we scale down the transistor estimate issues like Short Channel Effects (SCE), Sub-edge voltage variety, Drain Induced Barrier Lowering (DIBL), Gate oxide burrowing spillage and so on., comes into the record [3]. The greatest drain current creates by double gate mode is a lot higher than single gate mode. A 1-bit ALU has been structured utilizing MOSFET and FinFET and reenacted, which executes four fundamental activities like expansion, subtraction, AND, OR. All the are done utilizing H-zest reenactment apparatus [4]. an 8-bit ALU that performs fundamental logical, arithmetic, and moving activities has been planned utilizing FinFET just as MOSFET structures and their spillage power has been contemplated and analyzed [5]. A One-Bit ALU is structured and reproduced in 32nm innovation utilizing FinFET gadget innovation. Reenactment show that the method gives improvement in Average Power Consumption and the utilization of FinFET gadget expands execution speed of the gadget rationale [6]. Downsizing in the MOS transistor expanded the interconnections and limits the circuit thickness. There are significant structure issues in MOSFET because of scaling, for example, Gate oxide burrowing spillage, Self-warming, Soft Error Rate, Strained-Si channel and high-K gate. Because of these structure issues there are more confinements and the significant test is control utilization. To diminish such difficulties and continue contracting the measure of transistor will accomplish the specific dimension of accomplishments in Nano gadgets with the assistance of FinFET [7]. To change nanoscale CMOS, a multi gate gadget called FinFET is recommended. FinFET has its very own favorable circumstances over the CMOS, for example, decrease in spillage control, working force, spillage current and transistor gate delay, diminished edge level and more extreme subthreshold swing. The objective of this paper is to lessen and compute spillage intensity of 4-Bit ALU utilizing FinFET [8]. The desire to improve the exhibition of rationale circuits, when dependent on customary CMOS innovation, in the advancement of numerous rationale plan strategies amid the most recent two decades. MGDI (Modified Gate Diffusion Input) is a system of low power advanced combinationalstructure; Compared to other as of now utilized rationale configuration styles, permits less power utilization and diminished engendering delay with least number of transistors [9]. The 1-bitFinFET-based full ALU demonstrates an incredible decrease in every one of the four metric exhibitions. A decrease in proliferation deferral, PDP, and EDPisevidentinthe1-bitFinFET-based full adder of CPL, giving the best generally speaking presentation because of its fast execution and great current driving abilities [10].

## II. PROPOSED METHODOLOGY

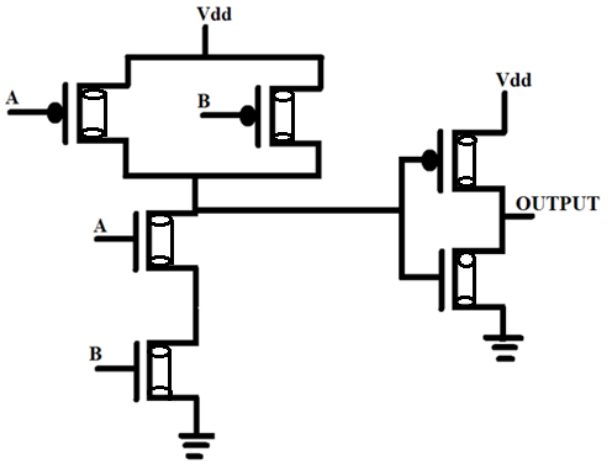


Fig.1: AND gate using CNTFET

The figure 1 shows the AND gate using CNTFET, here we are using P channel and N channel CNTFET .it is having four input and one output.

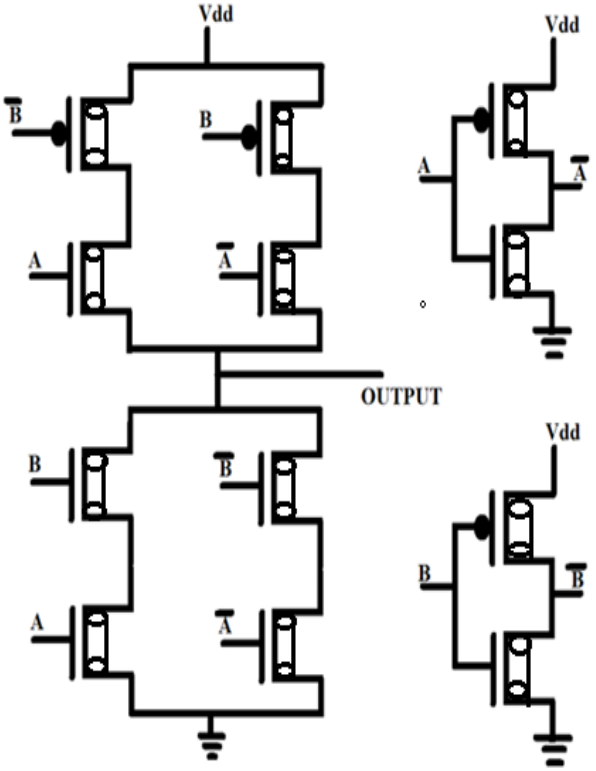


Fig.2: XOR gate using CNTFET

The figure 2 shows the XOR gate using CNTFET, here also using N channel and P channel CNTFET.it is having eight input and one output. Here we are giving vcc and ground.

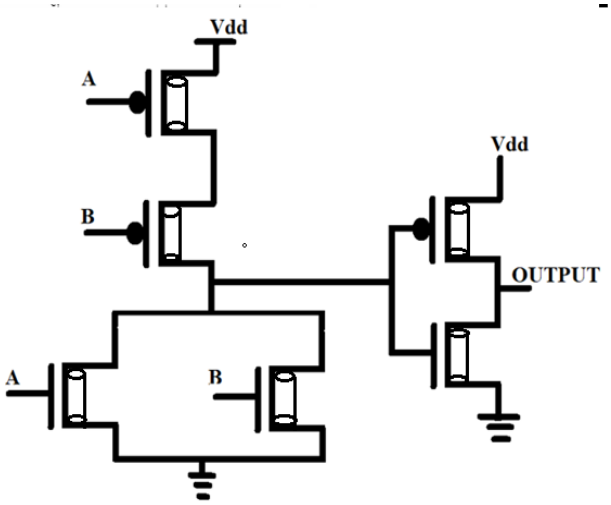


Fig.3: OR Gate using CNTFET

The figure 3 shows the OR gate using CNTFET, the circuit is making using N channel and P channel CNTFET.it is having four input and one output.

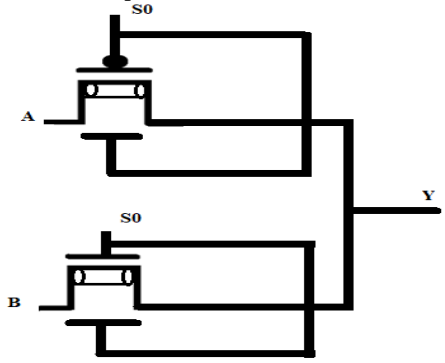


Fig.4: 2:1 mux logical using CNTFET

The figure 4 shows the 2:1 multiplexer it is having two inputs and one output. These circuit is made using P channel and N channel CNTFET.

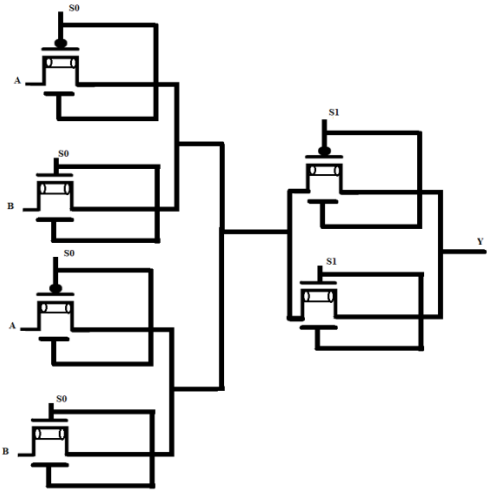

Fig.5: 4:1 mux logical using CNTFET

The figure 5 shows the 4:1 multiplexer and it is having four inputs and one outputs and these circuit made using N channel and P channel CNTFET.

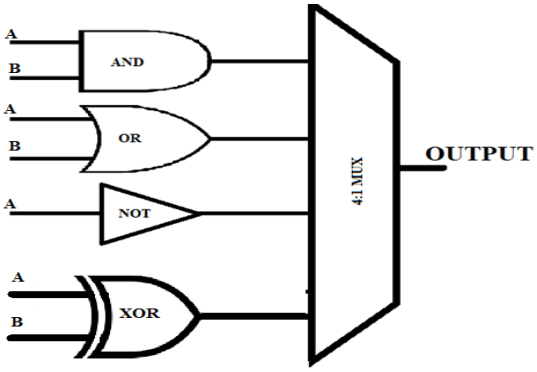


Fig.6: Mux Logical using CNTFET

The figure 6 shows the multiplexer logical circuit and it is having 4 input and one output. And the input is coming from outputs of AND gate, OR gate, NOT gate and XOR gate.

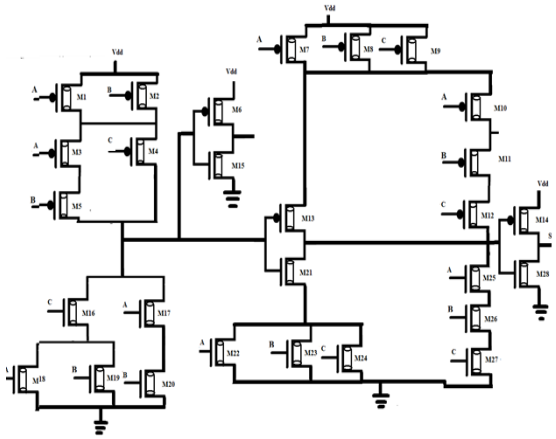

Fig.7: Full adder using CNTFET

The figure 7 shows the full adder circuit using CNTFET

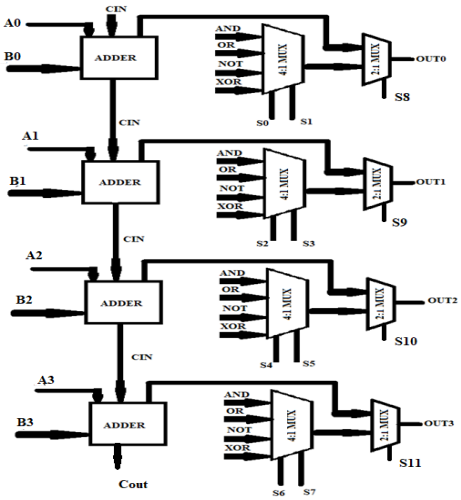


Fig.8: Proposed block diagram of 4-bit ALU

The figure. 8 shows the proposed block diagram of 4-bit ALU circuit. here we are using the six multiplexer and 4 adder circuit and different logic gates. And the proposed system has four outputs. And these proposed systems made up of N channel and P channel CNTFET.

## III. RESULT

**Table 1: Comparison of ALU FinFET and CNTFET**

| | ALU FinFET | ALU CNTFET |
|---|---|---|
| Average Power(W) | 5.58E-06 | 4.55E-06 |
| Delay(S) | 2.03E-09 | 2.00E-09 |
| Energy(J) | 1.13E-14 | 9.11E-15 |

The table 1 shows the comparison table of ALU using FinFET and CNTFET.here showing the comparison of average power, delay and energy of the ALU using FinFET and CNTFET circuits.

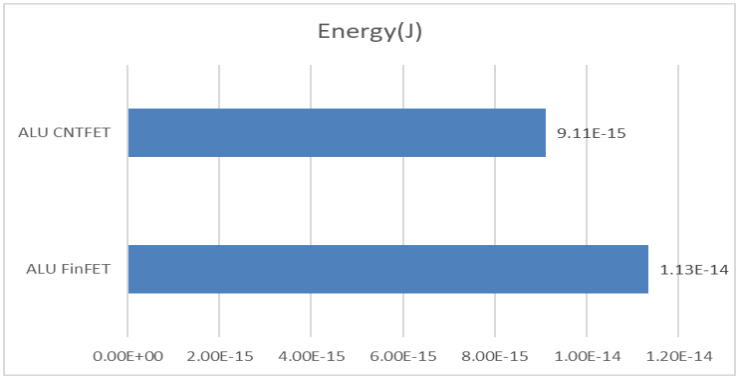


Fig.9: Graph diagram of energy

The figure 9 shows the graph diagram of energy comparison of ALU using FinFET and CNTFET.here we can see the energy is low in ALU using CNTFET and high in ALU using FinFET.

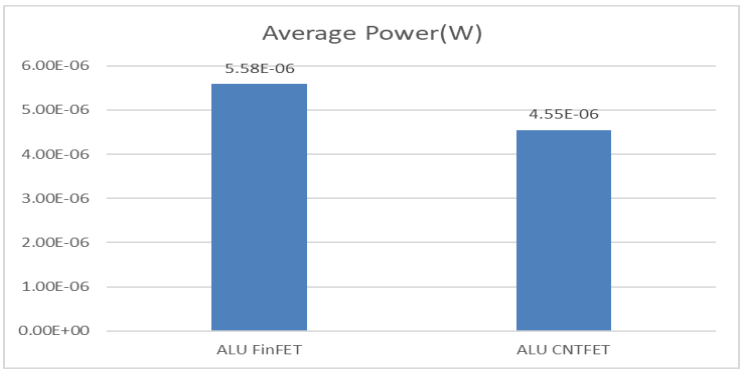


Fig.10: Graph diagram of average energy

The figure 10 shows the Graph diagram of average power comparison of ALU using FinFET and CNTFET.here we can see the average power is low in ALU using CNTFET and high in ALU using FinFET.

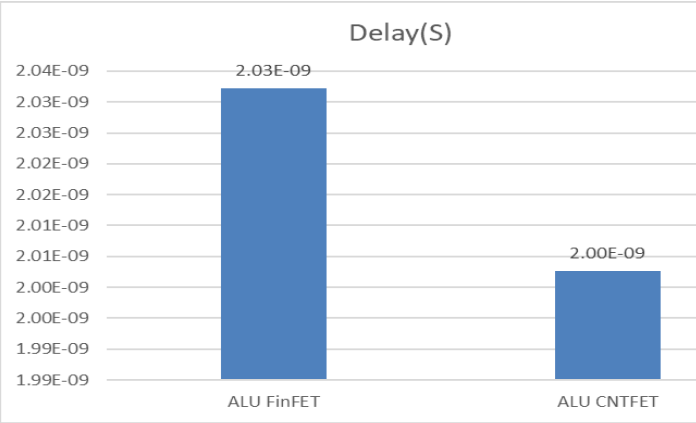


Fig.11: Graph diagram of delay

The figure 11 shows the Graph diagram of delay comparison of ALU using FinFET and CNTFET.here we can see the delay is low in ALU using CNTFET and high in ALU using FinFET.

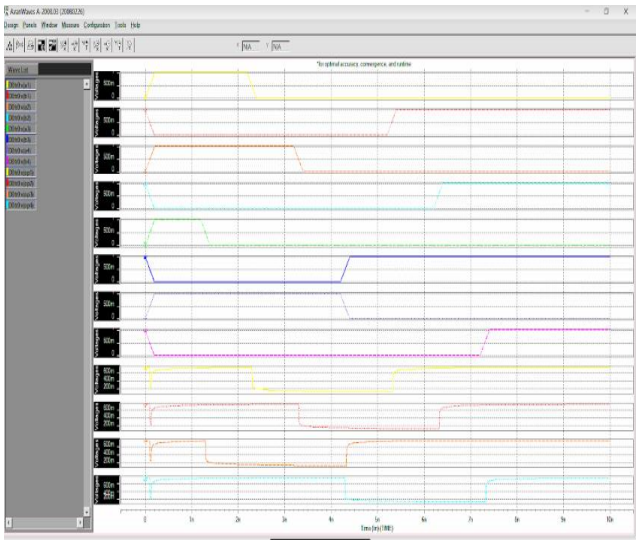

Fig.12: waveform of proposed 4-bit ALU

The figure 12 shows the waveform of proposed 4-bit ALU.here shows the comparison of average power, delay and energy of the ALU using FinFET and CNTFET circuits out puts.

## IV. CONCLUSION

Subsequently here we are considered Design and Optimization of 4-Bit ALU Using FINFETS and CNTFETS for Nano Scale Technology. Here we are utilizing distinctive cicuits utilizing CNTFET and looking at the ALU utilizing FinFET and CNTFET circuits out puts. Here we can see the normal power, vitality and postponement is low in ALU utilizing CNTFET and ALU utilizing FinFET high. Here we are utilizing diverse multiplexer (4:1 mux and 2:1), adder circuit and distinctive rationale gates (AND, OR, NOT and XOR gates). These proposed CNTFET circuits demonstrated the decrease of intensity, deferral and vitality. The exhibition parameter is likewise contrasted and ALU utilizing FinFET.

## V. REFERENCES

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