The Design and Verification of AMBA AHB Protocol by Using System Verilog

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***Abstract*—** Today electronic devices are becoming smaller in size, but have high performance and high operating range that is possible only because of System on-Chip(SoC) design mythology. A System on-Chip design have number of blocks are integrated on a single chip. While multiple blocks are integrating in single IC they required powerful communication architecture to access their functionality. In order to fulfill their requirements that is possible only by on chip bus Architecture. As today, different companies has different on-Chip Bus architectures but one of the most preferable architecture is AMBA by ARM in 1996.AMBA has three buses i.e., Advanced System Bus(ASB), Advanced Peripheral Bus(APB), Advanced High Performance Bus (AHB).Among these buses AHB has high performance, high bandwidth and for high clock frequency system modules so, system designers choose AHB as their first choice. The problem occurs while multiple master are trying to access a single bus and then resolution occurs as a big issue in SoC . In order to resolve the resolution problem that depends on system performance. AMBA Protocol use logical assignment to masters based on their priority they access the bus to transmit data. Arbiter block is important to decide which master get access to bus based on arbitration algorithm. The purpose of the arbitration algorithm is to assure that at one time only one master get access to the bus then remaining masters are should be idle state until they are granted by bus. These paper presents the design and verification of AMBA AHB Protocol with single master single slave, single master mutli slave, multi master single slave, mutli master mutli slave along with arbitration algorithms. The design architecture is written by verilog code and verification by system verilog code using MODELSIM 10.5b tool.

***Keywords*—** AMBA AHB, Arbiter, VerilogHDL, System Verilog.

I. INTRODUCTION

Due to VLSI technology, semiconductor industry has improved a lot because it achieved very high density of components in a single chip. But demand of market increased due to which complexity also increased. SoC is one of the emerging techniques. Multiple blocks are integrated on a single chip in SoC design. AMBA(Advanced Microcontroller Bus Architecture) is used as on-chip bus Architecture in SoC design. AMBA has three buses, namely Advanced High Performance Bus (AHB)[1], Advanced System Bus (ASB), Advanced Peripheral Bus(APB).When compared with other buses AHB has higher bandwidth and high performance because of this AHB is the first choice for system designers. This paper proposes the verification of AMBA AHB Protocol with single master single slave, multi master single slave , single master multi slave ,mutli master multi slave and arbitration algorithms such as High-Priority ,Round Robin .

II. AMBA OVERVIEW

AMBA is an open specification protocol, which describes number of bus and interface. It is enrolled by trademark of ARM in 1996.AMBA has three buses that is show in below architecture.

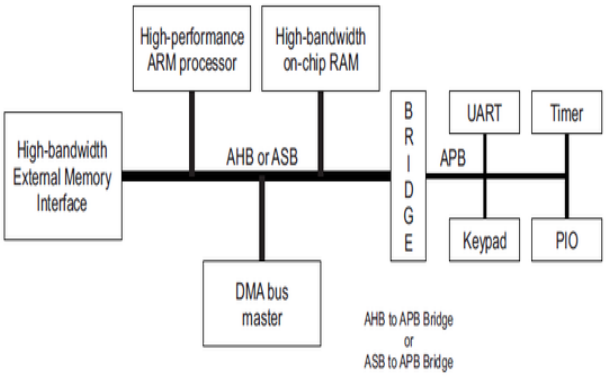

Fig.1 Advanced Microcontroller Bus Architecture

A. Advanced High Performance Bus

AMBA AHB is for high-performance, high clock frequency system modules. The AHB features are [1]:-

- Burst transfer
- Split transactions
- single cycle bus master handover
- Single clock edge operation
- Pipelined operation
- multiple bus masters

B. AMBA AHB Description

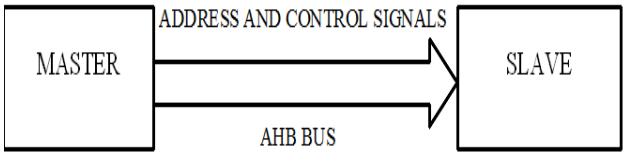

Fig.2 Single Master Single Slave

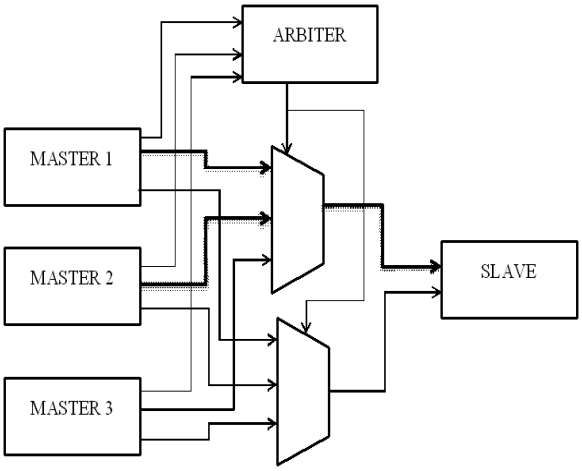

Fig.3 Multi Master Single Slave

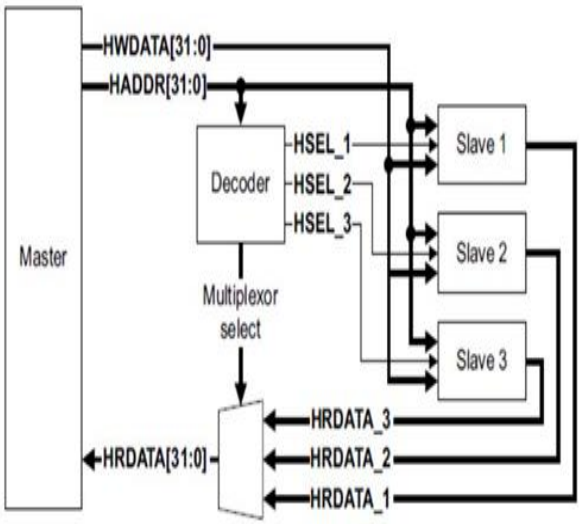

Fig.4 Single Master Multi Slave

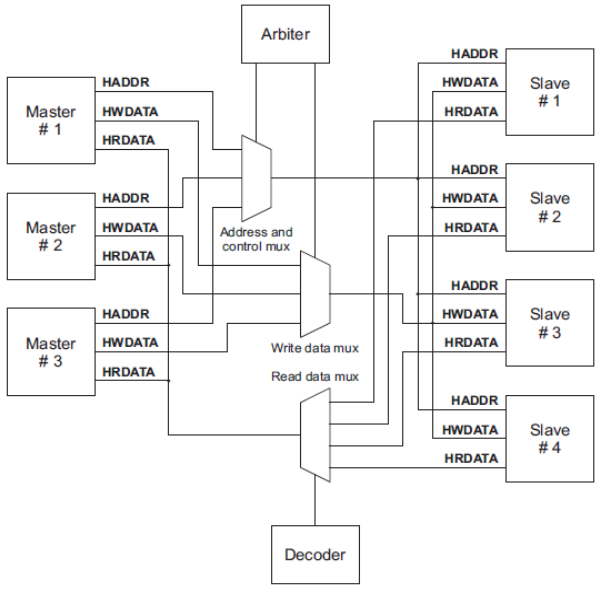

Fig.5 Multi Master Mutli Slave

III. BLOCKS IN AHB

A. Master

The write and read operation between the master and slave should be done after driving the address and control signals but at one time only one master should be active.

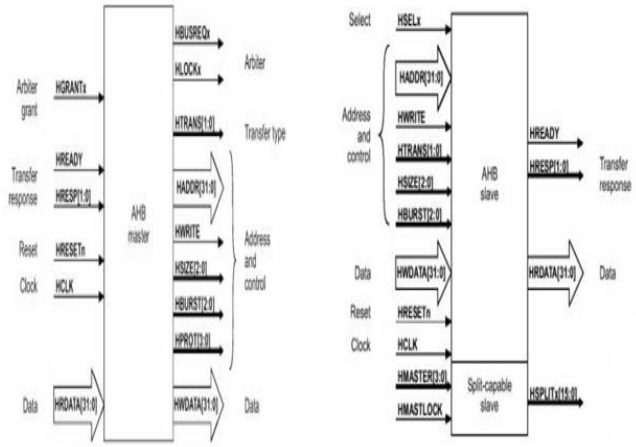

Fig. 6 AHB Master and Slave

B. Slave

Slave device responds to communication requests from a master.

C. Arbiter

AHB arbiter is to grant the particular master to access the data bus using arbitration techniques.

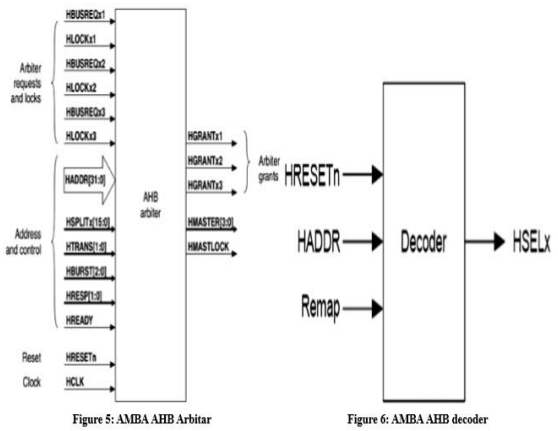

Figure 5: AMBA AHB Arbitar Figure 6: AMBA AHB decoder

Fig. 7 AHB Arbiter and Decoder

D. Decoder

It decodes the address of each data transfer to select the particular signal from the slave for read operation. Before AHB transfer, the bus master must be granted access to the bus. In this process first all master sends a request signal to an arbiter. After receiving the request from the master by using the arbitration algorithms such as high priority, round robin algorithms it grants particular master to access the data bus. The granted bus master transfers the data after driving address and control signals.

IV. ARBITER BLOCKS

Figure 8 shows AHB arbiter block diagram. The maximum number of masters used in arbiter is 16, but we used four masters (master 0 tomaster3) in this project. In this project arbiter has arbitration schemes such as high Priority, Round Robin algorithm that can be selected using a input signal ARBITRATION show in below table.

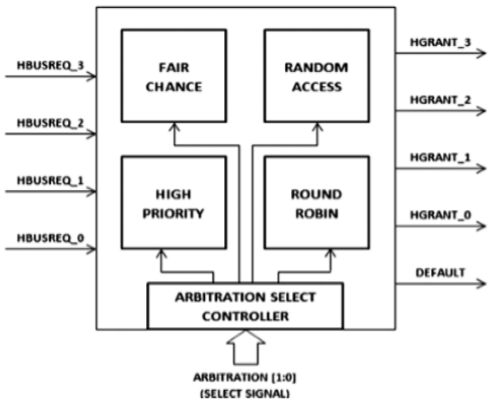

Fig. 8 Arbiter block diagram

With these functionality, it can assign any arbitration scheme among these which are designed, depending on the requirements of blocks. First of all. any master in the four can send request to arbiter to grant the master to access the bus. Then depending on the requirement of an application, we can select any arbitration scheme using input signal ARBITRATION [1:0] . Now, as per the selected arbitration scheme, grant signal will be generated to any particular master and hence master will get bus access [3].

Table 1 Selection of Arbitration Algorithm

ARBITRATION [1:0]	Arbitration Selection Algorithm
00	High Priority Algorithm
01	Fair Chance Algorithm
10	Random Access Algorithm
11	Round Robin Algorithm

A. High Priority:

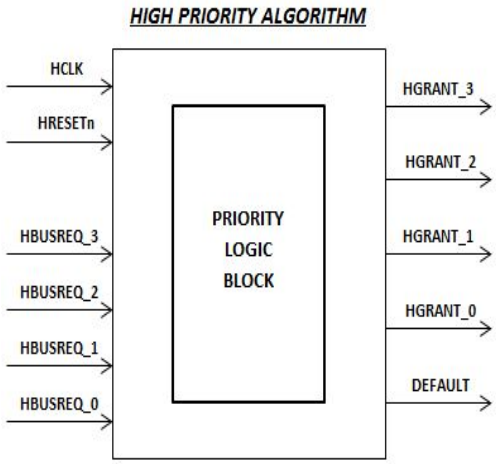

Fig. 9 High-Priority algorithm

When we select "ARBITRATION =00" it enters to High-priority state. In High-Priority arbitration algorithm, already priorities of masters are fixed based on these master requests will be granted. Request signals for Master0, Master1, Master2 and Master3 are assigned to HBUSREQ_0, HBUSREQ_1, HBUSREQ_2,HBUSREQ_3 respectively.

Suppose Master1 and Master3 are sending request for bus access, in arbiter it compares the two masters that which master has high priority that means first it will grant master1 to access the data bus and other master will be granted after the first master.

B. Round Robin :

When arbitration scheme selected signal "ARBITRATION=01", arbiter enters into this state. In Round Robin algorithm master1 as shown in the figure 10 have grant to access the share bus. In clock1, after data done signal master1 move to the bottom and in next clock, grant is given to master2, this process continues till all the master get grant to access to bus. After fourth clock master11 is again in top position have grant to access the bus.

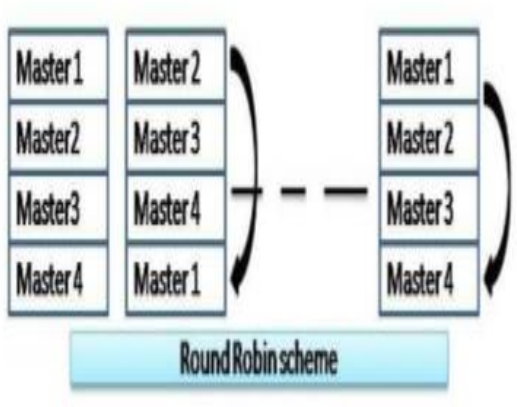

Fig. 10 Round Robin algorithm

V. VERIFICATION ENVIRONMENT

The verification environment to verify AMBA AHB Protocol shown in fig.11.The different modules of environment are explained.

Verification environment is group of class's performing specific operation. Above figure shows that in base packet we are declaring the variables and next in tx_gen we are generating the stimuli's for that input variables that are declared in base packet. From tx_gen the data is giving to driver. Then data transactions will drive through driver to DUT through interface. The monitor receives the data from DUT through interface and it displays the various messages according to the operation. Monitor sends the actual input to Scoreboard and driver sends the expected output Scoreboard verify the actual and expected results are matched or not.

Test is the top layer of verification specification and work as the functional block. Under the base packet, tx_gen, driver, monitor and scoreboard are using to create the design of the modules to generate the signals and output are to check the monitor and scoreboard.

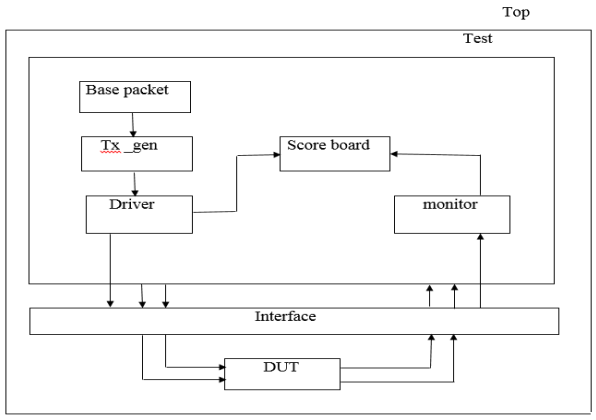

Fig.11 Verification Environment

VI. PROPOSED METHOD

First, AMBA AHB Protocol was designed by using verilog HDL that should be compile using Modelsim 10.5b software after compilation completed .simulate the program and check the waveforms of design and check the address ,write data and read data. And the proposed method is to create the system verilog verification environment for the AMBA AHB protocol compile and simulate it by using Modelsim 10.b software after the simulation is succeed and verify the output results with verilog HDL results.

VII. SIMULATION RESULTS

Simulation results of design and verification of AMBA AHB Protocol with arbitration algorithms were given below.

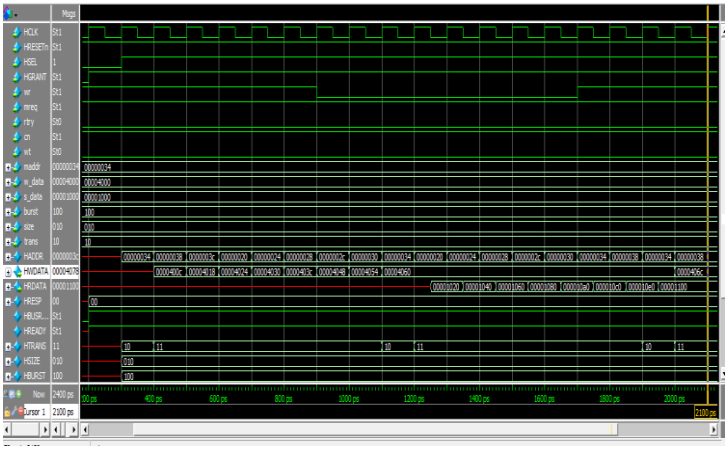

Fig.12 single master single slave without wait and retry (design)

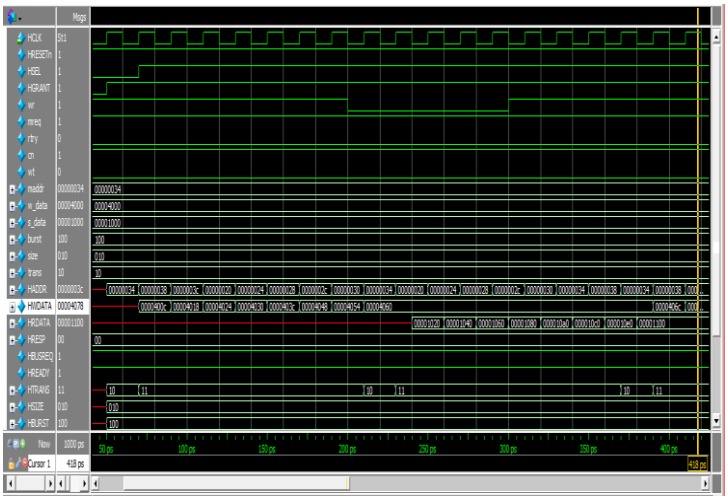

Fig. 13 single master single slave without wait and retry (verification)

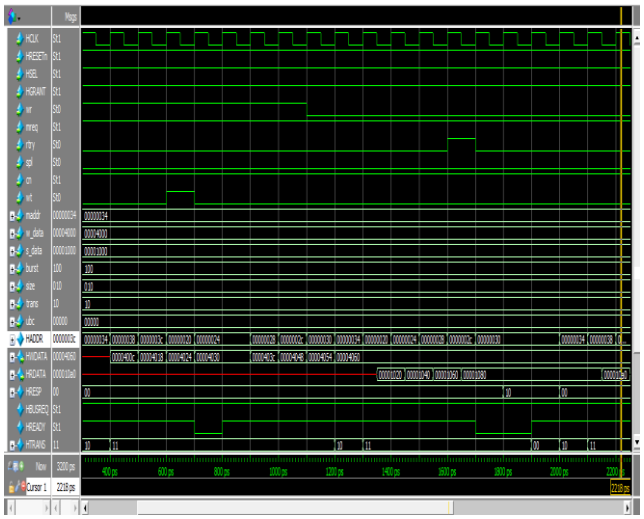

Fig. 14 single master single slave with wait and retry (design)

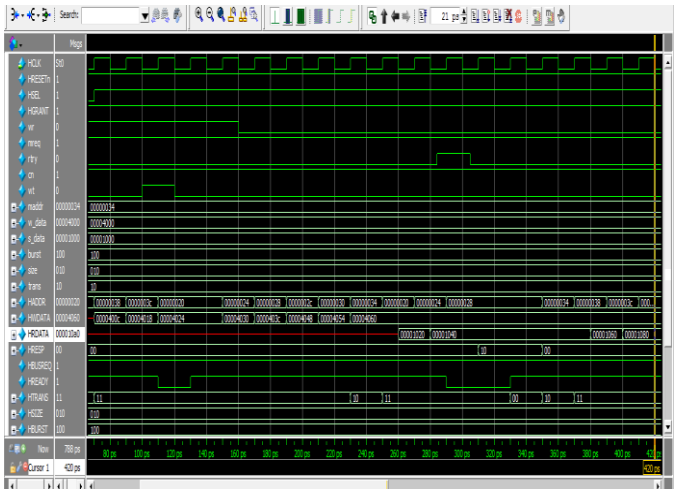

Fig. 15 single master single slave with wait and retry (verification)

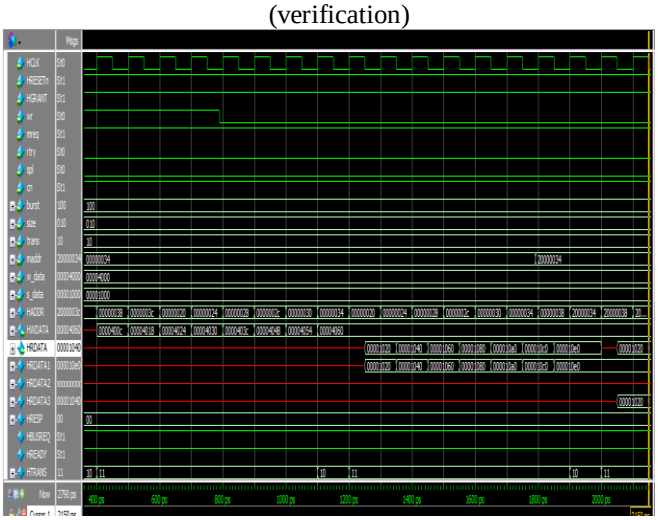

Fig. 16 Single Master Mutli Slave without wait(design)

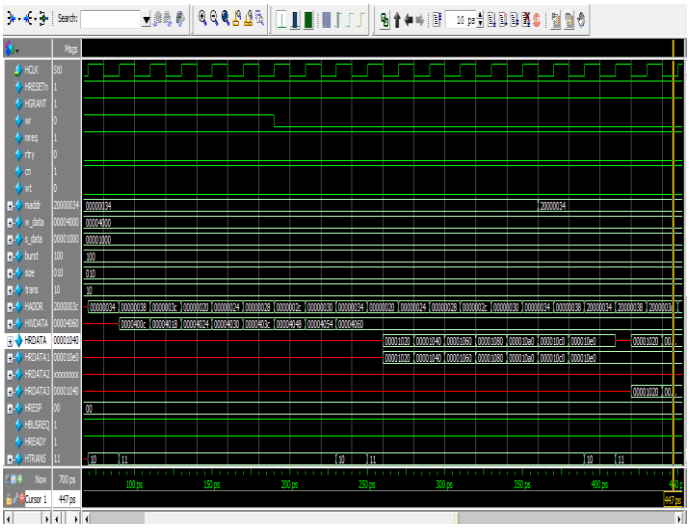

Fig. 17 Single Master Multi Slave without wait (verification)

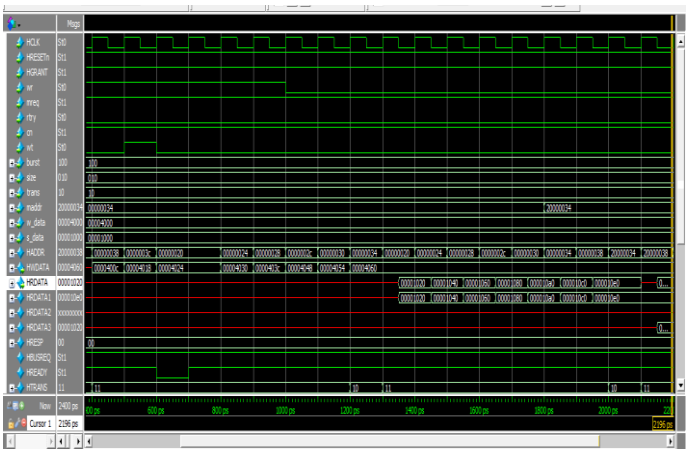

Fig. 18 single master multi slave with wait (design)

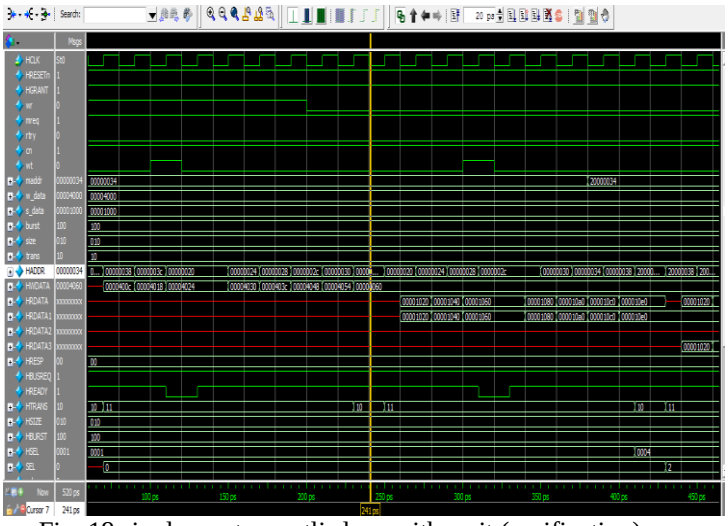

Fig. 19 single master mutli slave with wait (verification)

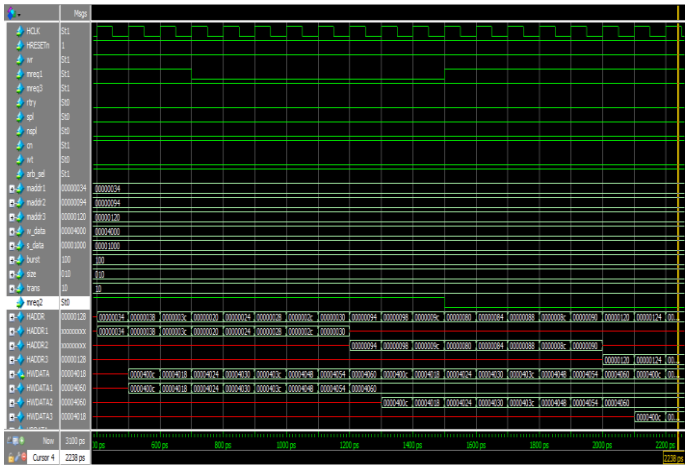

Fig. 20 mutli master single slave with round robin algorithm (design)

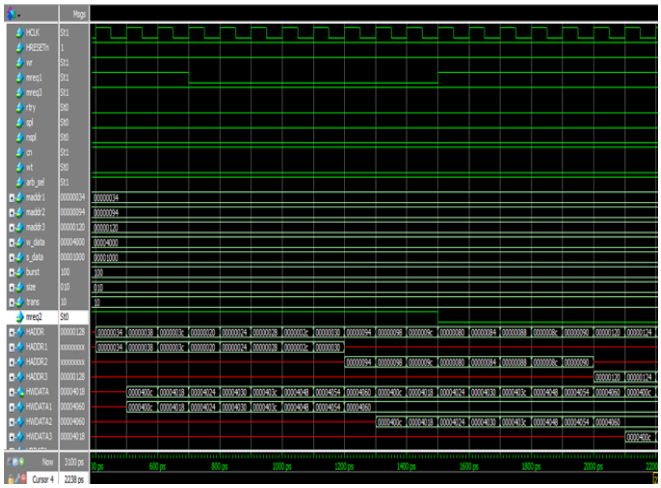

Fig. 21 mutli master single slave with round robin algorithm (verification)

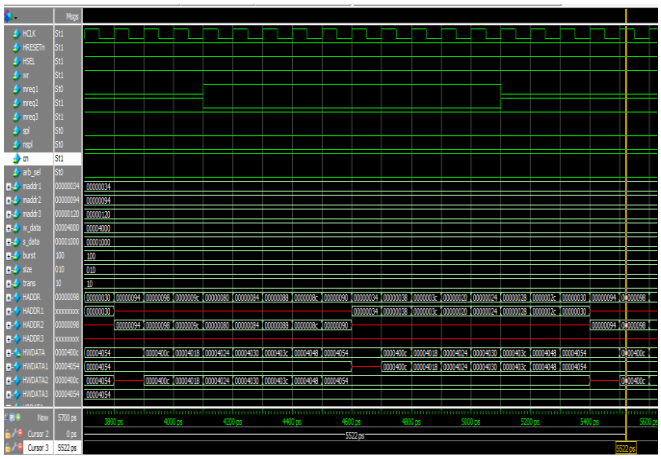

Fig.22 multi master single slave with high priority (design)

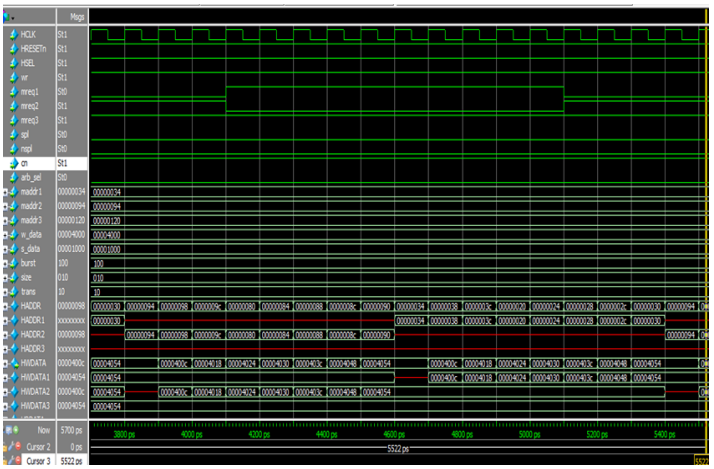

Fig. 23 mutli master mutli slave with high priority (verification)

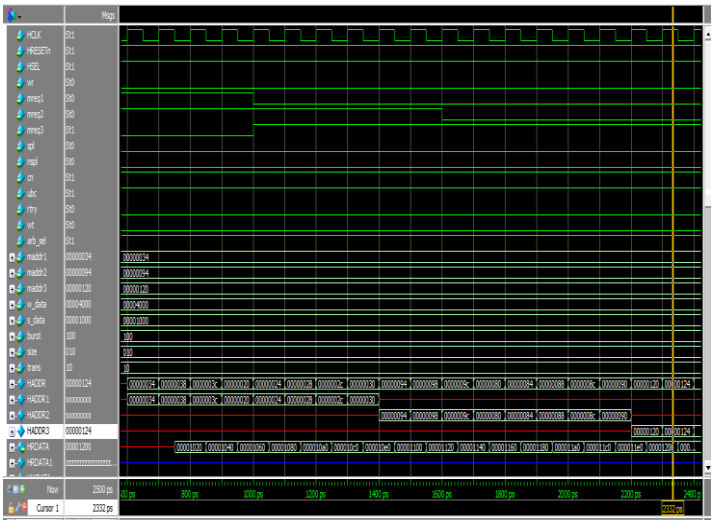

Fig. 24 mutli master single slave read operation (design)

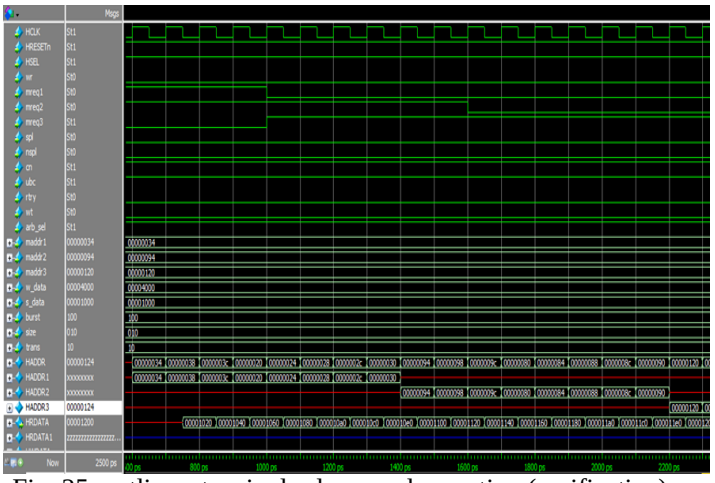

Fig. 25 mutli master single slave read operation (verification)

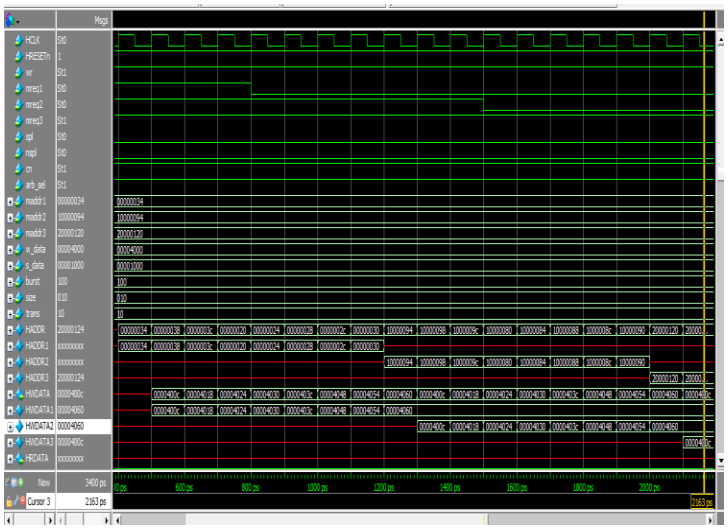

Fig. 26 mutli master mutli slave round robin algorithm (design)

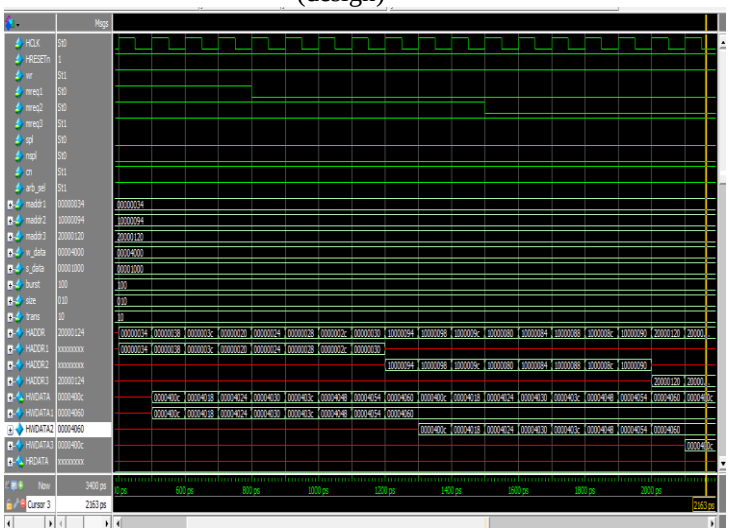

Fig. 27mutli master mutli slave round robin algorithm (verification)

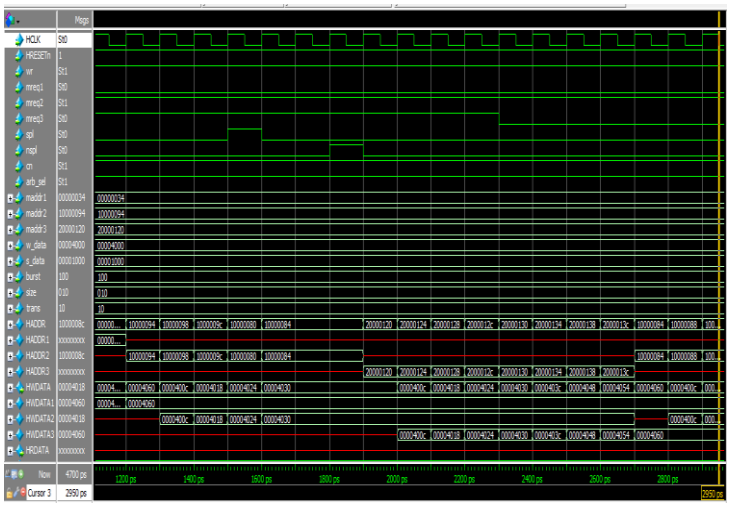

Fig. 28mutli master mutli slave round robin algorithm split (design)

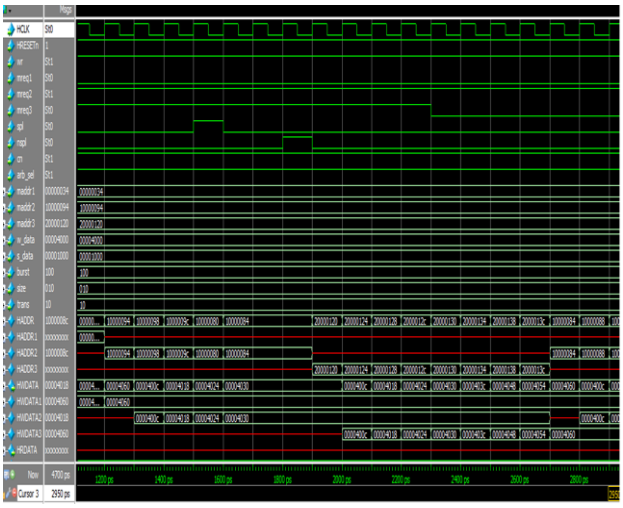

Fig. 29 mutli master mutli slave round robin algorithm with split (verification)

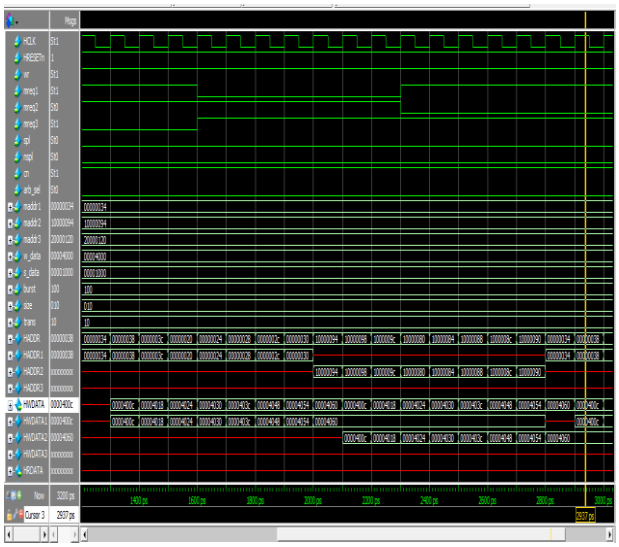

Figure 30 multi master mutli slave high priority (design)

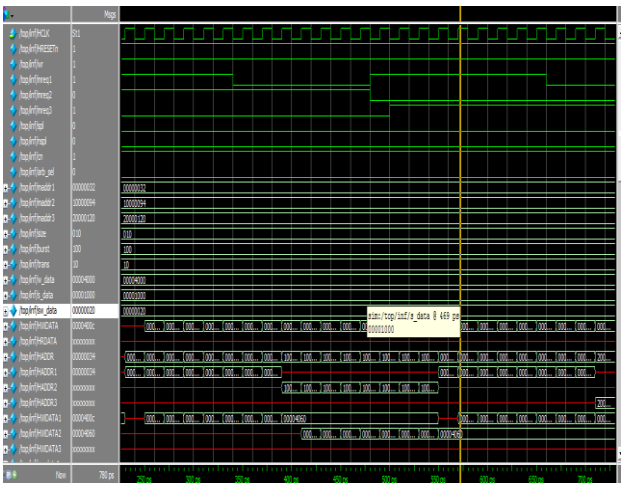

Fig 31mutli master mutli slave high priority (verification)

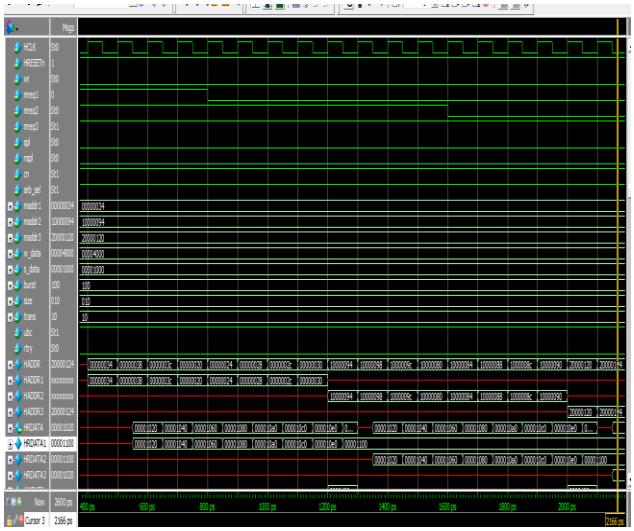

Fig 32mutli master mutli slave read operation(design)

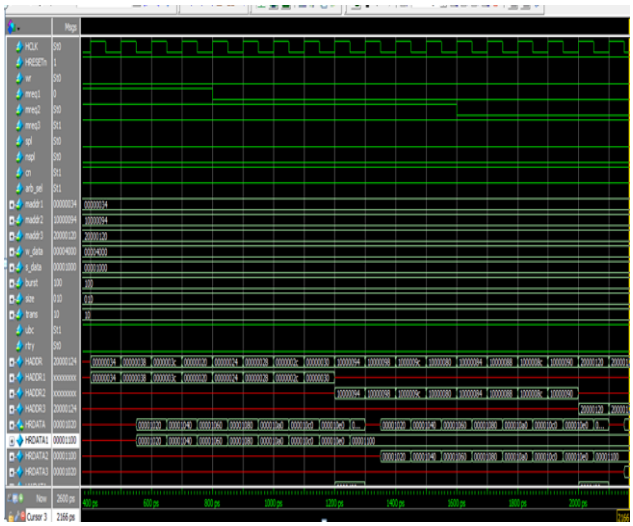

Fig. 33mutli master mutli slave read operation(verification)

VIII. CONCLUSION

In this paper, design of AMBA AHB Protocol using single master single slave, single master multi slave, multi master single slave and mutli master mutli slave was successfully designed using verilog and simulated using Modelsim 10.b software. The proposed method is verification of entire design of AMBA AHB was created using system Verilog. The proposed verification environment comprised of base packet,tx_gen, driver, interface, DUT, monitor, score board were implemented by using OOP concepts. The functionality of the design verified by the system verilog verification environment. The advantage of this design is that we can have take care of latch formation and this helps in achieving better compatibility with different blocks on SoC platform.

IX. REFERENCES

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