



16-Mbit (1M x 16) Static RAM

Part Number: DPA71061DV3302A

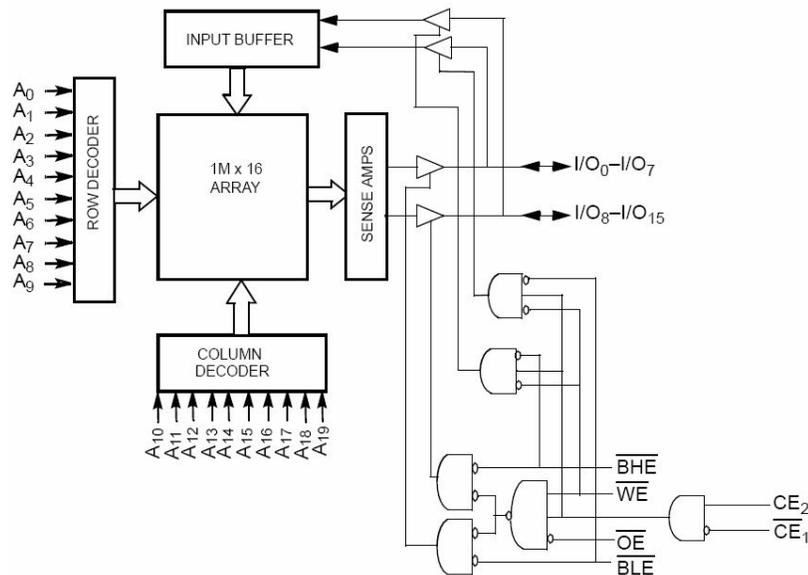
The DPA71061DV3302A is a high-performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

Writing to the device is accomplished by enabling the chip (\overline{CE}_1 LOW and CE_2 HIGH) while forcing the Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by enabling the chip by taking \overline{CE}_1 LOW and CE_2 HIGH while forcing the Output Enable (\overline{OE}) LOW and the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ through I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₈ to I/O₁₅.

The Input/ Output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH/ CE_2 LO), the outputs are disabled

Logic Block Diagram



- -55° to +125°C operating temperature
- High speed
 - $t_{AA} = 12 \text{ ns}$
- Low active power
 - $I_{CC} = 125 \text{ mA @ } 12 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 25 \text{ mA}$
- Supply voltage
 - 3.3 V dc
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- 54-pin SO ceramic flatpack, same footprint as 54-pin TSOP II
- Custom packaging is available
- This product uses Cypress CY7C1061DV33 die and is tested to meet military and space operational environment requirements

Pin Configuration

