A Review on Dynamic Power Minimization in VLSI Circuits using Glitch Reduction Techniques

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Abstract **-** The use of Very-Large Scale Integration (VLSI) circuits has augmented in terms of popularity and deployment due to improvement in process technologies, architectures and CAD tools. Nonetheless, the static and dynamic power consumption in VLSI circuits has been a challenging issue which makes the circuit design more complex, irrespective of the advancements made in the circuit. Therefore, reducing the power consumption is an important task in VLSI circuit design. This paper reviews the various techniques for reducing glitch power in VLSI circuits. Different techniques are available for reducing glitch power such as gate sizing, gate freezing, hazard filtering, balancing path delay, clock gating, transistor sizing, clock skew scheduling, etc. Apart from reviewing these techniques, this paper makes a comparative analysis based on the techniques developed by various researchers by highlighting their corresponding advantages, drawbacks and limitations.

Keywords- *Dynamic power consumption, Very-Large Scale Integration (VLSI), gate sizing, gate freezing, hazard filtering and clock skew scheduling.*

I. INTRODUCTION

Several advancements in abundant process technologies, logic architectures, and CAD tools permits progressively larger and faster systems to be applied in integrated circuit designs. As a consequence, these huge integrated systems consume large amount of power (Girard et al., 2002). Reducing the power consumption of the integrated circuit systems not only reduces the cost, but also allows the integrated system to be wide open to many other applications. The power exhausted in Complementary metal oxide semiconductor (CMOS) is categorized as leakage or static power consumption and dynamic power consumption (BVP et al., 2013). The static power is dissipated when the current leaks between various terminals of a transistor switch, while the dynamic power is dissipated when the individual circuit nodes toggle. Even though the static power increases relative to the dynamic power for innovative process technologies, the dynamic power remains the dominant source of power dissipation in integrated circuits (Lamoureux et al., 2007). "Under a timing constraint" is one such design problem to minimize the power as much as possible. Although the rising importance of static power in CMOS circuits, the dynamic power is still the main provider to power consumption (Saini& Mehra, 2012). Dynamic power is mainly consumed by glitches which are the unwanted transitions and require to be eliminated. Glitch and leakage power both are the main contributors to the power consumption and requires to be minimized. The minimization is based on the dynamic power consumption model; where to maintain the performance, size of gates on the critical paths remain unchanged while the sizes of the gates on non-critical paths are sized down to make use of their timing slack. This leads to reduced gate capacitance which results in reduced dynamic power consumption. The leakage power consumption is reduced by dual threshold (Huang et al. 2006). The gate sizing up will increase the gate capacitance and hence, the large dynamic power with minor leakage will be attained. The lower threshold assignment will cause large leakage power increase. The dynamic power consumption is owing to the low impedance path between the rails created via the switching devices. The switching at the outcome of logic gates is due to required functional transitions or spurious or false transitions called glitches (Wang et al., 2011). The glitches at the output of logic gates are due to differences in arrival times at various inputs. The various techniques described in this paper are discussed based on the various researchers. There are various conventional techniques to remove glitches in the logic circuits to accompany required functioning of the logic circuit (Benini, et al., 2000). Glitch less is a circuit level technique which minimizes the dynamic power consumption in incorporated circuits by actively preventing each of the logic output from toggling till all the inputs have been completely resolved. The glitch less technique provides the potential to remove all the glitches that are present in the circuits, thereby saving consistent amount of power (Lamoureux et al. 2008).This research study conducts a review on dynamic power minimization in VLSI circuits by using glitch reduction techniques.

II. RELATED WORKS

Glitches are the false transitions which generated due to difference in arrival times of signals at the inputs of gate. These are not essential for the correct functioning of the logic circuit. Power consumed by glitches is known as the glitch power. But in the real situation there are output transitions switching greater than once in each clock cycle and these redundant transitions will also consume power and they supply considerably to unpredicted peak currents which are higher than that of original designs specifications.

Hence, there are various techniques are developed by the researchers to reduce the glitches such as gate sizing, transistor sizing, gate freezing, balancing algorithm and various statistical approaches. Fig.1 shows that the various glitch minimization techniques to reduce dynamic power.

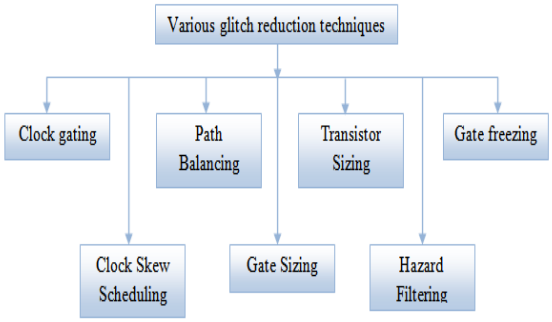

Fig.1 various glitch reduction techniques.

A. Clock gating

Srinivasan et al., (2015) proposed a smart grid technique where the construction blocks are such as control units and sensor system are developed in Silicon on Chip (Sock) in Very-Large Scale Integration (VLSI) circuits. In VLSI circuits, the sequential circuit's clock is the primary resource of dynamic power consumption. The clock gating technique is used to minimize the consumption of clock power by cutting off the inactive clock cycles. Besides, a VHDL based approach to introduce clock gating circuit and the dynamic power due to this is computed. The experimental is developed by using Xilinx ISE tool for simulating and computing power. The results demonstrate that the dynamic power is minimized for the sequential benchmark circuits measured. Wilmer et al., (2012) proposed a probabilistic design of the probabilistic which permits to estimate the expected power savings and the implicit overhead. The power saving representations in the gated clock tree are developed and the best gate fan-out is derived using flip-flops toggling probabilities and process parameters. The examination and the results attained for a 16-bit microcontroller and a 3D graphics processor, both developed at 65-nanometer technology. The experimental shows that the gating technique acquires 10% savings of the entire clock tree switching power. Besides, the timing implications and the grouping of FFs for a combined clocked gating are presented. Low power design with high computing capability is an essential task due to the increasing requirement of battery functioned portable devices. It is an important issue in ASIC design, because featured size is scaled down. A huge amount of power consumed is due to the high switching activity and the clock distribution network at the nodes. Sudhakar et al., (2015) proposed a clock gating technique used to decrease the clock power. To save power, by using clock gating where triggering the clocks in a logic block only when there is a function to be done. Each unit on the chip has a power reduction technique, and approximately each Functional Unit Block (FUB) includes the clock gating logic. Also, they verified the way of Glitch minimization for ISCAS 85 bench mark circuits using clock gating theory. Clock gating technology can reduce the consumption of clock signal's switching power of flip-flops. The clock gate enable functions can be identified by Boolean analysis of the logic inputs for all adders. Kaushik et al., (2013) considered clock gating for power reduction and presented that clock gating capability be integrate at different points in the clock distribution network. Also implemented AND gate based clock gating circuit for 3-bit full adder circuit. Depending on the architecture and clock activity, clock power can be reduced by over 50%.

B. Clock Skew Scheduling

Dong & Lemieux, (2009) described programmable delay elements (PDEs) based an architectural approach to minimize dynamic power through clock skew scheduling (CSS) and delay padding (DP). It is incorporated into VPR 5.0, and is invoked after the routing phase. They employ programmable delay elements (PDEs) as a new architecture alteration to put in delay on FF clock inputs, activating all optimization processes to share it, and removing multiple architecture modifications. The major concept is assuming the trade-off between power and performance, and computing a suitable cooperation considering development variation and timing uncertainties. Furthermore, a novel design to calculate flitching power is presented by considering the analogy performance of glitch pulse width minimization as it travels along FPGA routing paths. The experimental results demonstrate that the innovative glitch evaluation technique can miscalculate glitching power by up to 48%, and overestimate by up to 15%. The method eliminate on average 16% of flitching power.

Liao et al., (2014) proposed clock skew scheduling technique for power reduction. In addition, they developed the data path synthesis using gate sizing and buffer insertion. In this, they present an integer linear programming for the concurrent application of clock skew scheduling and data path synthesis. From this analysis, the designed technique is the primary function to contribute with this issue. The performance evaluation of these techniques demonstrates the better results compared to conventional techniques.

In VLSI circuits, the dynamic power consumption is directly connected to the number of signal transitions. Glitches are undesired false transitions caused by inputs of a gate arriving at different times, therefore causing redundant power dissipation. Vijayakumar&Kundu, (2014) proposed clock skew scheduling to minimize the number of glitches in a circuit for decreasing the dynamic power. In this, diverse flip flops receive clocks at different times in clock skew scheduling. Thus, they formulate the scheduling based on an Integer linear Programming problem and develop vector-independent clock skew schedule to minimize glitches. In addition, they propose linear objective functions based on timing window of gates for optimization. The

results demonstrate that the method acquire an average reduction of approximately 32% in glitch power.

C. Path Balancing

Dinh et al., (2010) proposed a new technique to minimize dynamic power in field-programmable gate arrays (FPGAs) by minimizing glitches during routing. It determines alternative paths for early arriving signals, thus signal arrival times at look-up tables are associated. They designed an effective algorithm to estimate routes with target delays and then constructed a glitch-aware router at minimizing dynamic power. Experimental results demonstrate that an average of 27% reduction in glitch power is obtained. Then it translates into an 11% minimization in dynamic power.

Sun&Choi, (2013) proposed a new techniques based on register-transfer level (RTL) circuits. The conventional technique aims on killing glitches in both the control and data path of the circuit to minimize power consumption. By simulating and analysing the propagation of glitches in some benchmark circuits, arises some issues when killing glitches using conventional technique. In sometimes, the conventional technique reducing glitches still consume a large amount of power via glitches. Besides, it can't kill glitches in control path when two selected data are not correlated.

D. Gate Sizing

Jacobs et al., (2000) proposed gate sizing based on the statistical delay representation. It demonstrates the gate sizing issue matches accurately for a given statistical delay model. The formulation used provides various forms of objective functions. It is directly optimize the delay improbability at the circuit outputs. Also they create the gate sizing problem as a nonlinear programming challenge and demonstrate that if we do this carefully. They solved these issues precisely for circuits up to a few thousand gates using the openly accessible large scale nonlinear programming solver namely LANCELOT.

Wang et al., (2011) proposed a quantity known as power parameter and its effective computation technique due to the complexity in computing dynamic power at the gate level. In this, a heuristic gate sizing model for glitch power minimization is presented for semi-custom design based on power parameter. The new heuristic technique reduces the total power parameter of a circuit. The experimental is conducted based on 5 real industrial circuits, 8 ISCAS85 benchmark circuits. From this, the technique achieved 15.5% average total power reduction and more than 30% average glitch power minimization. The obtained enhancements of proposed technique are better when compared to the existing gate sizing techniques.

Kim et al., (2001) proposed an effective path balancing approach to decrease glitch power dissipation in CMOS logic circuits. This technique applies gate sizing and buffer insertion techniques to obtain path balancing. The gate sizing approach minimizes not only glitches, but also the efficient capacitance in the circuit. For the paths which remain disturbed after gate sizing due to the drawback of gate size, buffer insertion is performed. Determining the location of the inserted buffer is a complicated issue, because the power reduction obtained by an inserted buffer is directly related to the locations of the other inserted buffers. The ILP (integer linear program) has been applied to estimate the locations of inserted buffers. The experiments are tested on LGSynth9 1 benchmark circuits. The results demonstrate that 61.5% of glitch reduction and 30.4% of power reduction are attained without increasing the significant path delay.

E. Transistor Sizing

Wróblewski et al., (2002) proposed a combinatorial block of static CMOS circuit's transistor sizing is employed for delay balancing. To avoiding glitches, the guarantee synchronously arriving signal slopes at the input of logic gates. Because the delay of logic gates depends directly on transistor sizes, their variation permits equalizing various path delays without influencing the total delay of the circuit. In addition, the power consumption circuits depend on the transistor sizes. To attain best results, transistor lengths have to be enlarged which outcomes in both increased gate capacitances and area.

Kumara Swamy et al., (2013) proposed a new technique called complementary metal-oxide semiconductor (CMOS) gate design which has different delays along different input to output paths surrounded by the gate. The delays are realized by inserting selectively sized series transistors at the inputs of the gate. The effort is made show the use of the variable input delay CMOS gates for a completely glitch-free least dynamic power realization of digital circuits. The major contributions includes the technique to model and removal of glitch activity in digital circuits using various techniques and modified circuit for removal of glitch is proposed.

F. Hazard Filtering

In CMOS circuit, the power is dissipated mainly due to transitions which are the hazard pulses produced by a logic gate when signals appear by paths of changing delays. The highest width of a hazard pulse generated by a gate is the highest difference between the delays of incident paths, which is much smaller than the clock period. Agrawal, (1997) presented a suppression of hazard pulses by rising the gates delay where hazards has been produced. Therefore, a hazard filtering gate has a delay which is at least as much as the differential delay of its input. The instance demonstrate the new technique and also represents that the entire reduction in the circuit speed may not be too much with appropriate sizing of transistors, while there is an important minimization in power consumption.

Slimani&Matherat, (2011) described the issue of circuit level design for low power. They proposed a novel technique for the reduction of glitch power using threshold voltage adjustment which is based on hazard filtering. This technique obtains both dynamic and leakage power minimizations. In addition, they establish an optimization

algorithm that transforms the circuit net list in an optimized one attaining glitch energy reductions without affecting the entire circuit delay constraints. Employing the algorithm to C17 benchmark circuit developed in a 65nm industrial Low Power CMOS process. The technique obtained 14% of whole energy savings and 78% of leakage energy savings at the cost of just 5% of delay increase.

G. Gate freezing

Benini et al., (2000) proposed a technique for glitch power reduction in combinational circuits. The total number of glitches is minimized by exchanging few conventional gates with functionally equivalent ones namely F-Gates which is freezing by asserting a control signal. A freezing gate cannot transmit glitches to its output. Algorithms for gate selection and clustering that exploit the percentage of filtered glitches and minimize the overhead for generating the control signals are initialized. Also, a power efficient CMOS circuit's implementation of F-Gates is developed. A significant feature of the technique is that it can be employed in place directly to layout-level descriptions; therefore, it guarantees very predictable results and reduces the impact of the transformation on circuit size and speed.

One of the most important techniques supplying to the power dissipation in CMOS circuits is the switching activity. There are many types of switching activities include spurious pulses known as glitches. Lee et al., (2004) proposed a novel approach of glitch reduction by gate freezing, gate sizing and buffer insertion. This method integrates gate freezing, gate sizing and buffer insertion into a single optimization design to exploit the glitch reduction. The efficiency of this approach is demonstrated experimentally using LGSynth91 benchmark digital circuits with a 0.5um standard cell library. This optimization approach minimizes glitches by 65.64% and the power by 31.03% on average.

III. COMPARISON OF VARIOUS TECHNIQUES

The comparative analysis of various glitch reduction techniques for dynamic power minimization is shown in Table1. This comparison table provides advantages and research gap of each glitch reduction technique.

Table1: Comparative analysis of various glitch reduction techniques.

S. No	Paper Title	Technique used	Outcomes	Research Gap
1.	A gate sizing method for glitch power reduction (Wang et al., 2011)	Gate sizing	15.5% average total power reduction and 30% average glitch power reduction.	Large runtime.
2.	Power Reduction by Clock Gating Technique (Srinivasan et al., 2015)	Clock gating	21.91% of power reduction for 4-bit counter circuit.	The size of the circuit is large.
3.	Simultaneous data path synthesis and clock skew scheduling for leakage and glitch power minimization (Liao et al., 2014)	Clock Skew Scheduling	30.10% of power reduction for s641 circuit.	Large path delay.
4.	Novel Techniques For Circumventing The Glitch Effects On Digital Circuits For Low Power VLSI Design (Kumara Swamy et al., 2013)	Transistor Sizing	62.5% of logic activity reduction.	The transmission gate adds capacitance which causing additional power consumption
5.	Glitch elimination by gate freezing, gate sizing and buffer insertion for low power optimization circuit (Lee et al., 2004)	Gate freezing	Reduces the glitches by 65.64% and the power by 31.03%.	The technique doesn't consider the delay.
6.	Multiple threshold voltage for glitch power reduction (Slimani&Matherat, 2011)	Hazard Filtering	14% of total energy savings and 78% of leakage energy savings.	5% of delay increase.
7.	GFCG: Glitch free combinational clock gating approach in nanometer VLSI circuits (Sudhakar et al., 2015)	Clock gating	22% of average power savings.	Low Speed.
8.	Glitch power reduction via clock skew scheduling (Vijayakumar&Kundu, 2014)	Clock Skew Scheduling	32% of average glitch power reduction.	Tunable buffers for generating clock schedules have dissipate extra power.

IV. CONCLUSION

In this paper, the various glitch reduction techniques such as gate sizing, gate freezing, hazard filtering, balancing path delay, clock gating, transistor sizing, and clock skew scheduling have been discussed for minimizing the dynamic power in VLSI circuits. Each technique is determined according to the required specification in terms of the parameters used. Also, comparative analysis of glitch reduction techniques is studied with advantages and future recommendations.. This research study serves as a beneficial knowledge for future research direction.

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