Analysis and Design of CMOS 1 Bit Comparator Using Stacking Technique

J.E.N Abhilash[1], L.Ruchita sowmya[2], T.Satya Sree[3], P.Naga Lakshmki[4], M.Srinivasa Manikanta[5].
Swarnandhra college of engineering and technology

Abstract- This paper presents the design and analysis of a CMOS based efficient one bit comparator circuit. Comparator has been designed and simulated in 180nm TSMC technology. The proposed circuit uses a XNOR gate, two AND gates and two NOT gates. Stacking technique has been used to improve the conventional design. Power supply has been varied from 1.0V to 2.8V for the proposed and basic design. Result reflects that proposed approach shows less power consumption and improved power delay product (PDP)

Keywords- CMOS, Comparator, power dissipation, Stacking, VLSI.

I. INTRODUCTION

The comparator is an electronic circuit which compares the magnitude of one signal to another signal. The comparators are used in analog to digital converters [1], [2]. Comparator is the "Heart" of the Analog to digital converter (ADC). As we talk about the VLSI te+chnology, in this environment the device should be of higher speed, less cost and low power consumption. Many of the electronic devices like mobile devices and other portable computing devices have constraints in terms of power consumption [3]. Power consumption is the vital factor of VLSI circuit design for CMOS is the primary technology. The power consumption is considered as a major issue in VLSI circuit design. So, the reduction of power consumption of integrated circuits by the design improvement has become a vital challenge in portable system design. For solving the problem of power consumption , unique techniques from circuit level to device level and above have been proposed. However, there is no straight forward ways to meet the tradeoff between power, delay and area. In CMOS comparator design there are some points of consideration like chip size, speed, power consumption are taken into account [4]. To overcome the constraints, several logic styles have been developed to improve power consumption.

Unique techniques provide an appropriate way to reduce leakage power. Coming to its disadvantages in which each technique limit the application of each technique.

II. BASIC COMPARATOR

The comparator is basically 1-bit analog to digital converter [5]. Fig.1 shows general block diagram of comparator and Fig.2 shows symbol of comparator.

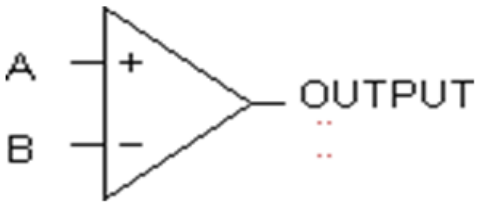

Fig.1: symbol of comparator

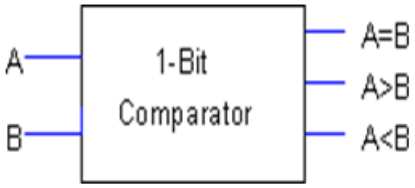

Fig.2: Symbol of Comparator

Truth table of CMOS 1-Bit Comparator

A	B	A=B	A<B	A >B
0	**0**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**1**	**0**	**0**	**0**

The equation for A=B is **AΘB** **(1)**

The equation for A>B is **A** **(2)**

The equation for A<B is **B** **(3)**

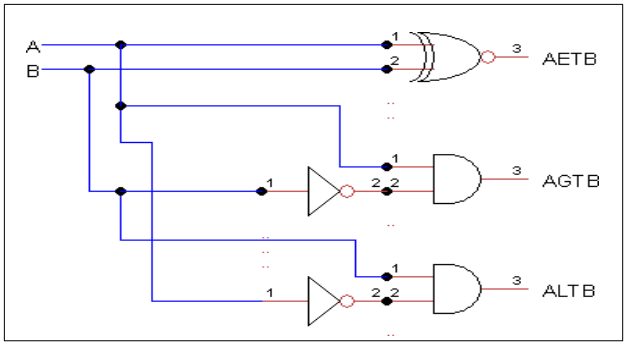

Fig.3: Logic diagram of 1-Bit Comparator

The basic 1 bit Comparator circuit consist of three basic building blocks, two AND gates and one XNOR gate. Each AND gate consists of six MOSFET, three PMOS and three NMOS. XNOR gate consists of fourteen MOSFET, seven PMOS and seven NMOS.

The comparator basically a analog to digital converter, Analog signal is converted into digital signal with the help of sampling .The sampling frequency (f_S) is defined as the reciprocal of time period T.

$$f_S = 1/T$$

The propagation delay time (t_p) of comparator is determined with the help of slew rate (SR) of the comparator.

where, t_p=prpropagation

SR= slew rate

III. PROPOSED COMPARATOR

In this work the stacking techniques has been applied to conventional comparator to reduce the power consumption. Fig.3 shows stacking technique [6], [7]. In stacking technique every transistor is divided into two transistors each have W/L is half of parent transistor as shown in the Fig.4.

The number of transistor increases but area is not affected much since W of parent transistor is divide into two transistor of W/2 width each.

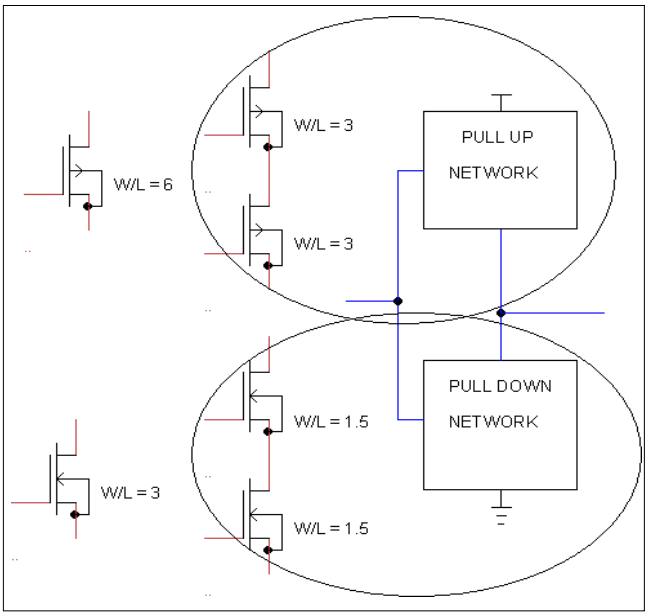

Fig.4: Stacking technique

When two transistors are turned off together induced reverse bias between the two transistors results decrease in power. This technique is based on the fact that natural stacking of MOSFET helps in achieving leakage current. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect [8]. An effective way to reduce leakage power in active mode is stacking of transistor [8]. In proposed comparator circuit there are three building blocks, two AND gates and one XNOR gate. Each AND gate consists ten MOSFETS, five PMOS and five NMOS each. XNOR gate consist of twenty two MOSFETS including eleven NMOS and eleven PMOS. The proposed comparator circuit is shown in Fig.6. For AGTB and ALTB, AND gate has been used because in AND gate whenever both inputs are high then output will be high otherwise output will be zero. For AETB a XNOR gate has been used as in XNOR gate whenever both inputs are same then output will be high otherwise it will be zero. The basic comparator circuit shown in Fig.5 and proposed comparator circuit shown in Fig.6 In n Bit comparator the truth table consists 2^{2n} terms in which number of terms for equal condition will be 2^n and for greater than and less than number of terms will be In 1 bit comparator number of AETB conditions are 2 and number of AGTB or ALTB conditions are 1 as shown in TABLE 1.

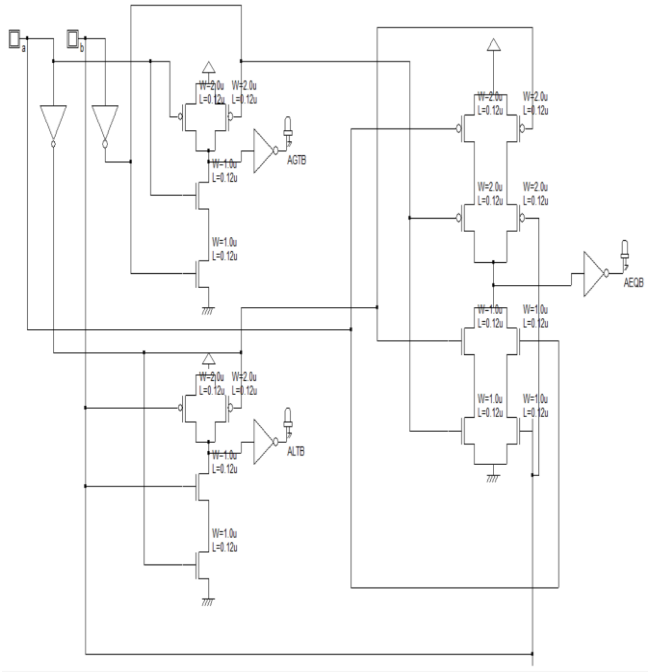

Fig.5: Basic comparator circuit

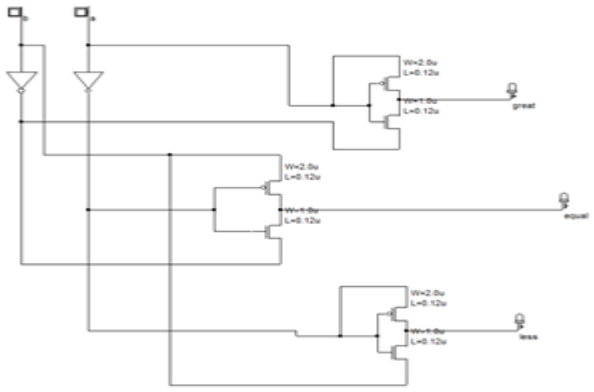

Fig.6: Proposed comparator circuit

Results of proposed and conventional comparator has been obtained in TSMC 180nm technology for different power supply voltages varying from 1.0 V to 2.8V. The simulation waveform of 1-bit conventional comparator is shown in Fig.7

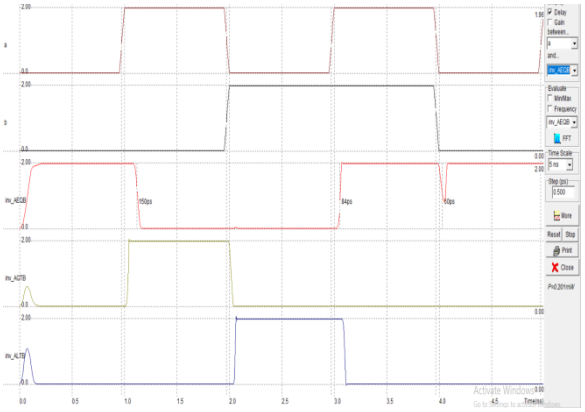

Fig.7: Schematic simulation of Basic 1-Bit Comparator

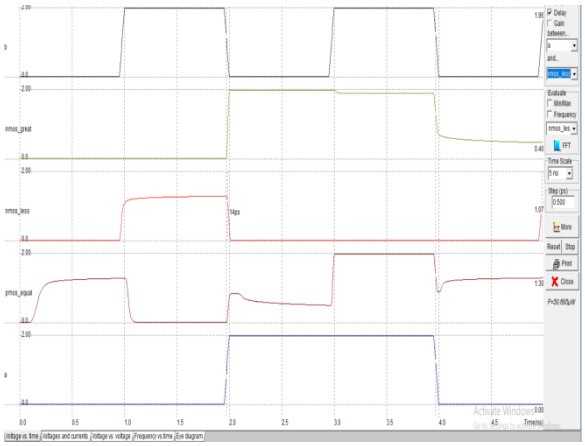

Fig.8: The simulation waveform of 1-bit proposed comparator

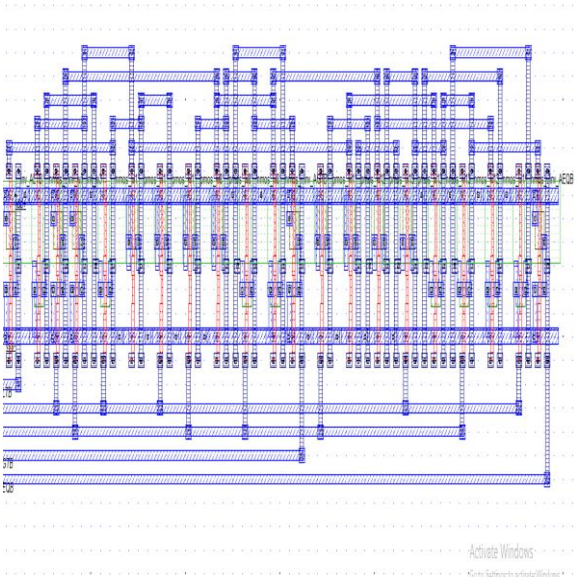

Fig.9:Basic comparator output

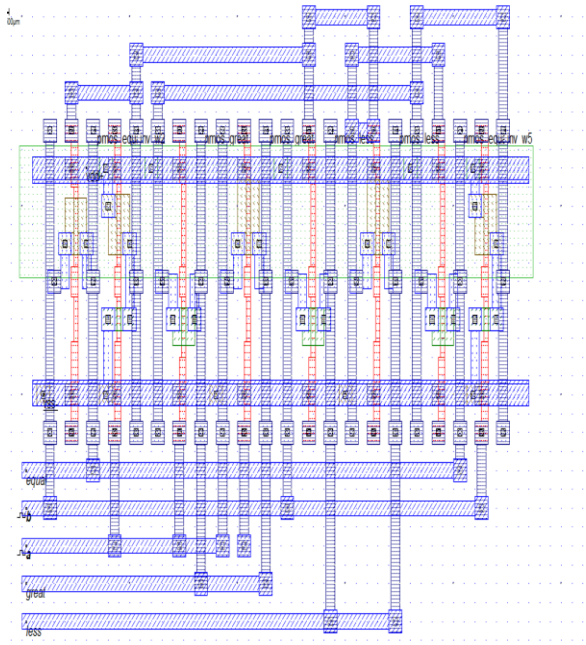

Fig.10: Proposed comparator output

Figure 10 represent the proposed comparator output wave form The comparative analysis of power consumption between two comparators is shown in TABLE 2. It has been observed that as Vdd increases the power consumption increases because power is directly proportional to V_{dd}^2.

TABLE2 COMPARISSON OF POWER CONSUMPTION

Parameter	Basic	Proposed
Delay	86ps	29.2 ps
Power	0.201 mw	50.895 uw
No.of transistor	26(13 nmos,13 pmos)	13(5 nmos,5 pmos)
Gain	1.046(0.4 db)	0.893(-1.16db)
TSMC technology	180nm	180nm
Input voltage	1v	1v

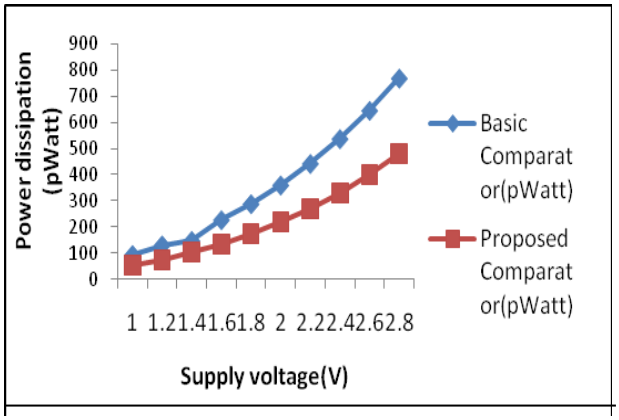

Fig.11: Variation of Power dissipation in Basic Comparator and Proposed Comparator.

In this work a new design of comparator has been proposed and power consumption, delay and PDP results have been obtained for the basic design and proposed circuit.it is noticied The Proposed Comparator has less power consumption, less delay and less PDP as compared to basic comparator. that the power consumption in proposed comparator is 174.352pWatt whereas the power consumption in basic comparator circuit is 287.93 pW, in terms of delay the delay in both circuits are almost same there is very little difference, PDP of proposed comparator is smaller than basic comparator. Proposed comparator shows less power consumption and improved power delay product.

IV. REFERENCES

[1]. arvind kumar ,manoj kumar University School information CommunicationTechnology Delhi, India arvindbtech2014@gmail.com

[2]. B. M. Dharmendra, B. Arun, B. Nandurbarkar, " Study and Implementation of Comparator in CMOS 50 NM Technology" International Journal of Research in Engineering and Technology(IJRET),) ISSN: 2321- 7308, Volume-3,Issue-2, pp. 252- 255, Feb- 2014.

[3]. M.E. Johnson, D. Somasekhar, and K. Roy, "Models and Algorithms for Bounds on Leakage in CMOS Circuits," IEEE Transactions on Computer Aided Design on Integrated Circuits and Systems, vol. 18, no. 6, pp. 714-725, June 1999.

[4]. J.C. Park, V. J. Mooney III and P. Pfeiffenberger, Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation,pp. 148-158, September 2004.

[5]. S. Kang and Y. Leblebici "CMOS Digital Integrated Circuit, Analysis and Design" (Tata McGraw-Hill, 3rd Ed, 2003).

[6]. 1.C. Park, V. 1. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," in Proc. 2004 International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 148- 158, September 20041. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[7]. B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," IEEE J. Solid-State Circuits, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[8]. H. E. Neil,Weste, D. Harris and A. Banerjee, "CMOS VLSI Design, Pearson Education,Third Edition,pp.9-10,2008.

[9]. M.E. Johnson, D. Somasekhar, and K. Roy, "Models and Algorithms for Bounds on Leakage in CMOS Circuits," IEEE Transactions on Computer Aided Design on Integrated Circuits and Systems, vol. 18, no. 6, pp. 714-725, June 1999.

[10]. M. Hassan, R. Mehra, "Design Analysis of 1-bit CMOS comparator", International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882, pp. 68-72, March, 2015.