Design and Implementation of Low Power Dual Edge Triggered Flip-Flop Using Pseudo Nmos

P.J.L.S Phanishri, G. Deepthi, M. Ramesh, S. Suresh

Abstract- In this paper, a technique for implementing low-power Dual Edge Triggered Flip Flop (DETFF) is introduced. Dual edge triggered flip flops has many advantages in low power VLSI compared to SETFF. The Proposed low power DETFF is implemented and compared with conventional DETFF at same simulation conditions. DSCH tool based simulation and comparison between the non-conventional DET flip-flop with the conventional DETFF shows that the proposed DETFF reduces power dissipation by reducing the no. of transistors used while keeping the same data rate.

Keywords- Dual Edge Triggered Flip Flop (DETFF),pseudo NMOS, Low power VLSI

I. INTRODUCTION

In modern digital world, flip-flops are used in maximum sequential VLSI circuits. A flip-flop is a basic memory cell which works on either the rising edge or the falling edge of the clock pulse. A flip-flop along with the clock distribution network accounts for 30%to 60% of the power consumed by the entire circuit [1]. Hence, it is very much significant that the power consumption of the flip flop and the clock distribution network should be lessened. With the rapid development in VLSI technology, the demand to advance the performance of logic circuits has lead to the expansion of different logic design techniques. Hence it is important to design a circuit which is both power efficient and has less power latency.The sequence of the CMOS design was introduced through CMOS Digital Integrated Circuits Analysis and Design by Sung Mo Kang and Yusuf Leblebci[2] which was an inspiration from Digital Electronics [3]. Few designs of Low Power Dual Edge Triggered Static D Flip-Flop was described by Anurag ,Gurmohan Singh and V. Sulochana [4]. Power Efficient Explicit Pulsed Dual-EdgeTriggered Sense-Amplifier Flip-Flops by Myint Wai Phyu, Kangkang Fu, Wang LingGoh and Kiat-Seng Yeo was used for Power efficiency for dual edge trigger circuits [5]. Many researchers have designed low power DETFF[6]-[9]. Another power-Efficient Method (GDI) for Digital Combinatorial Circuits was introduced by Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner [10][11]. DETFF is a significant approach to reduce the power.

To start with our baseline circuit we used a conventional D-flip flop, a SETFF circuit, where we analyzed the speed and the power consumed by the design. Since we know that in DETFF the clock frequency is reduced by a factor of two it is more appropriate to use this design in VLSI technology. In this paper we've worked on DETFF designing, where we've used two methods, conventional and non-conventional, to design it. As we progress through the work, we see that the second method takes less power and area in comparison with the first method. We also see that the latency is minimized. For the rest of the paper, the discussion is organized in the following manner. In Section II we reviewed the basic SETFF i.e. D-flip flop. Section III

presents the conventional methods used to design the DETFF circuit. Section IV includes the non- conventional methods used to design the DETFF circuit. Comparison between the two methods used for the DETFF designing is shown in Section V. Finally section VI ends with conclusion.

II. TRADITIONAL SINGLE EDGE TRIGGERED FLIP-FLIP

For the designing of a traditional SETFF, we've used a conventional CMOS based D-flip flop. A schematic diagram of conventional D-flip flop is illustrated inFig.1.P

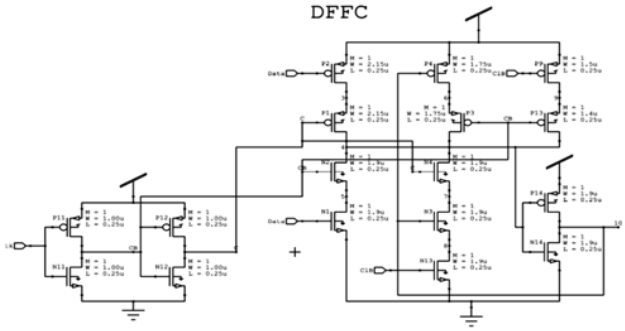

Fig.1: Conventional CMOS SETFF

throughput as SETFF in half the clock frequency [12Compared to the conventional SETFF the clock weight of the DETFF is lesser, which results in almost half power consumption in the clock distribution network. Therefore overall power savings in a system can be achieved since the clock sharing network holds a considerable part of the total power consumed of the design consumption in the clock sharing system. The DETFF works on mutually the rising and the falling edge of the clock, making the system more power efficient and achieving the same data Conventional flip-flops work on the positive edge of the clock. When the clock goes high the input given to the flip-flop is reflected at the output, which is shown in Fig 2. When the clock goes low, the

previous output is carried forward. We also see that the no. transistors used in this circuit are 17. Using 250nm technology the average power consumed is 2.136mW, for 50 Mbps data rate which is high for any VLSI design circuit.

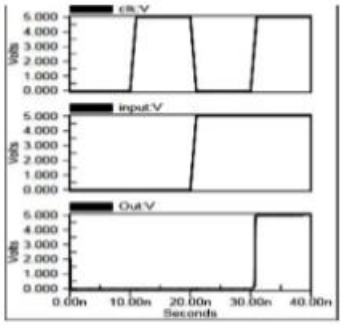

Fig.2: Behavioral response of SETDFF.

III. CONVENTIONAL METHODS FOR DETFFDESIGN

In this section two conventional circuits are demonstrated for the DETFF designing, one using D flip-flop along with multiplexer and the other only based on multiplexer.

A. DETFF based on D-flipflop

In Fig. 3, a conventional DETFF has been designed using a set of D-FF and a 2:1 MUX. Same data input is applied to both the flip flops. A clock pulse is applied to one of the flip-flops and its inverted pulse is applied to the other flip-flop, making the circuit work in both halves of the cycle. In the positive half of the cycle the first flip-flop works and in the negative half of the cycle the other flip-flop works. The outputs of the two flip- flops are then multiplexed using the multiplexer to generatethe desired output. The functional response is given below in fig. 4.

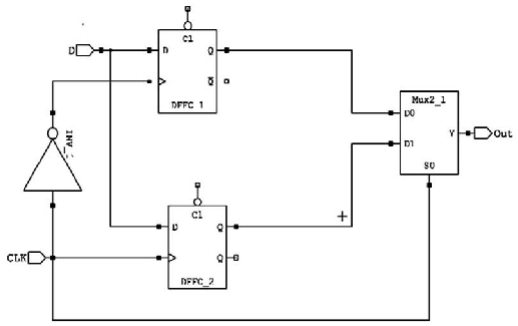

Fig.3: Conventional CMOS DETFF using a set of D-FF

In Fig 4, the first plot is the clock pulse of the circuit, the second plot is the input to the circuit and the third plot is the generated output. We see that the output is generated at the positive edge of the clock pulse as well as the negative edge of the clock pulse. This increases the efficiency of the circuit. Fig.5 shows the power consumed by the DETFF circuit using D Flip-Flop.

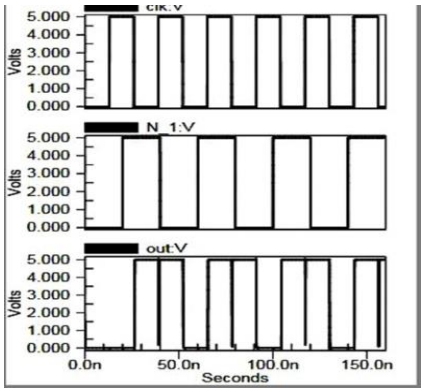

Fig.4: Behavioral response of DETFF using set of D-FFs

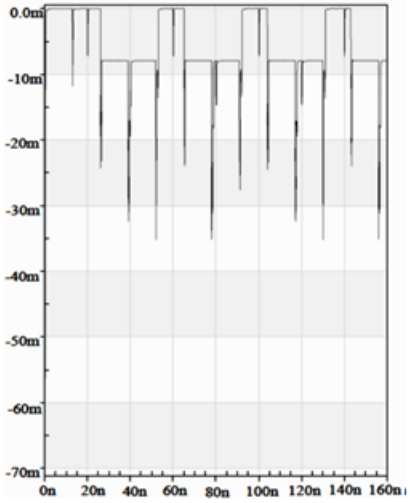

Fig.5: Power Consumed by conventional DETFF using D-FF

B. DETFF based onMultiplexer

Here we've divided the circuit into 3 stages, where in the first stage a positive latch using the multiplexer is designed. In the second stage a similar negative latch using the multiplexer is designed and in the third stage we've combined the two circuits to design the DETFF based onmultiplexers.

a. Positive latch

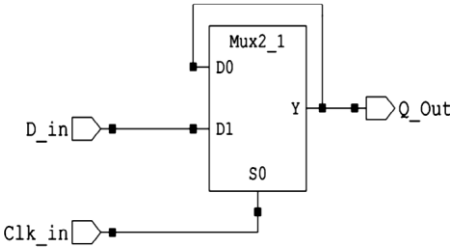

Fig.6: Positive latch using a multiplexer

TABLE I. TRUTH TABLE OF A POSITIVE LATCH USING MULTIPLEXER

D	CL K	Q
X	0	NO CHANGE
0	1	0
1	1	1

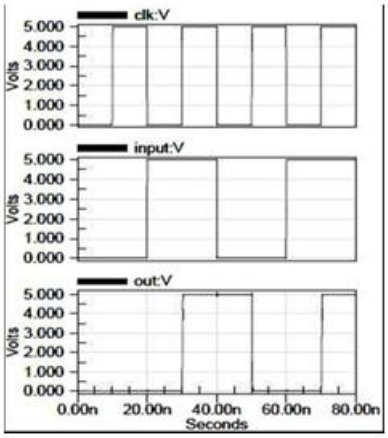

Fig.7: Behavioral response of positive latch using multiplexer

b. Negativelatch

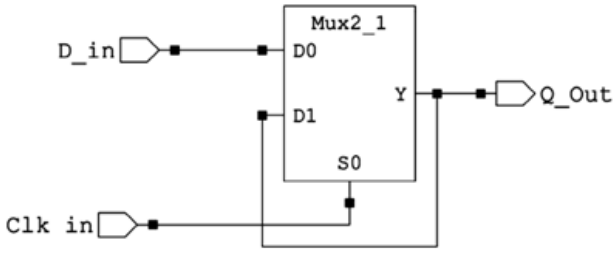

Fig.8: Negative latch using multiplexer

TABLE II. TRUTH TABLE OF A NEGATIVE LATCH USING MUX

D	CL K	Q
X	1	NO CHANGE
0	0	0
1	0	1

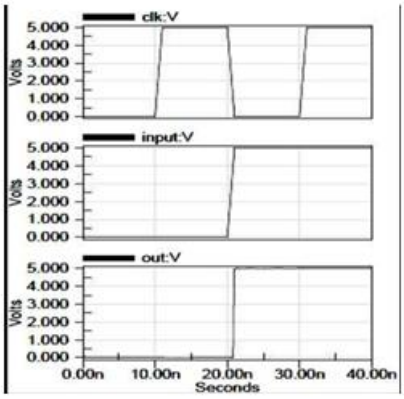

Fig.9: Behavioral response of negative latch using multiplexer

c. DETFF usingmultiplexers

In Fig 10, we have replaced D flip-flop circuits by multiplexers. One multiplexer acts as a positive latch doing the job of a positive edge triggered D flip-flop. The second multiplexer acts as a negative latch and doing the job of a negative edge triggered D flip-flop. The third multiplexer multiplexes the output of the two multiplexers and produces the output.

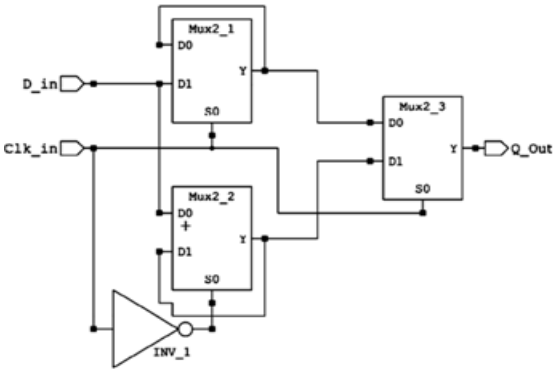

Fig.10: DETFF using multiplexers

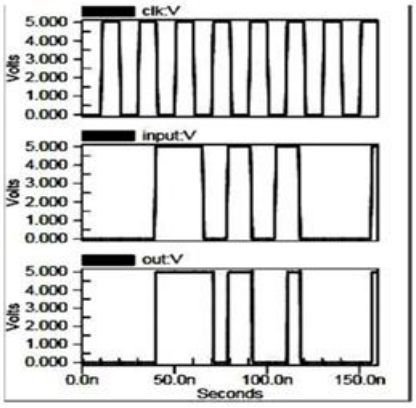

Fig.11: Behavioral response of DETFF using multiplexers

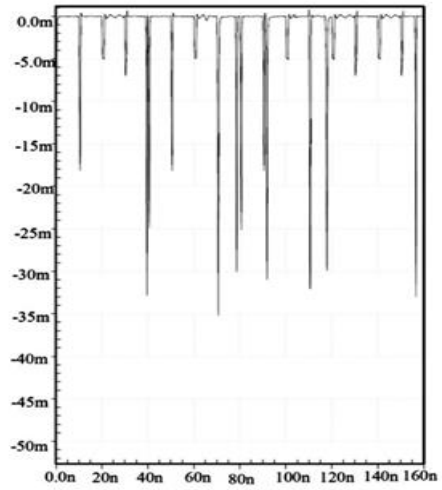

Fig.12: Power Consumed by the DETFF using multiplexers

We see that the output in Fig 11. Is the same as the output in Fig 4. We also see that we get a better result in the output of the DETFF using multiplexers. Fig.12. shows the power consumed by the circuit. Hence now we modify the circuit by modifying the multiplexers.

IV. NON-CONVENTIONAL METHODS FOR DETFF DESIGN

In this section two non-conventional circuits are used for the DETFF designing, one being a gate diffusion input (GDI) and the other a transmission gate (TG).

A. DETFF Based onGDI

Gate Diffusion Input (GDI) is a popular method for low power digital circuit design. More about GDI can be read from paper "Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits" by Arkadiy Morgenshtein, Alexander Fish, and Israel A.Wagner[10].

Here we use a GDI multiplexer for the DETFF circuit design. A 2:1 multiplexer can be made with a simple 2 transistor based GDI cell. Structure of a GDI cell is similar to that of a CMOS inverter but there are some important differences between the two.

- A CMOS has one input where as a GDI cell has 3inputs
- One input of the GDI is connected to the P terminal and the other is connected to the Nterminal.

The GDI multiplexer is illustrated below in fig.13.

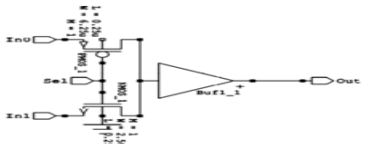

Fig.13: Multiplexer based on GDI

Here we have connected a PMOS and a NMOS whose two terminals have two inputs d0 and d1 respectively. Using CMOS logic, the implementation of a 2:1 multiplexer requires twelve nos. of transistors, and four transistors are needed in the transmission gate logic implementation. In GDI technique, a 2:1 multiplexer can be implemented using only 2 transistors. Even to find out the rail to rail swing of output extra four transistor based buffer circuit can be introduced. The schematic diagram of a DETFF based on GDI multiplexer is illustrated inFig.14

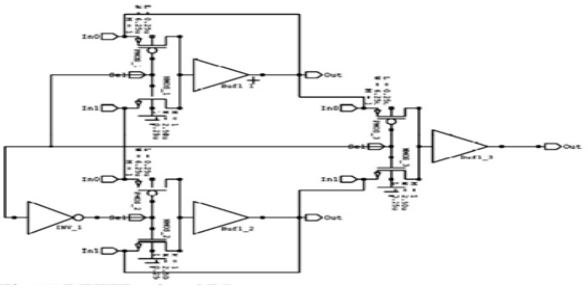

Fig.14: DETFF using GDI

In the above figure, three GDI multiplexers are used. Here one GDI multiplexer acts as a positive latch and the other one as negative latch. The third GDI multiplexer multiplexes the output from both the latches and generates the required output. The output as well as the power consumed is shown below in Fig.15 and Fig.16 respectively.

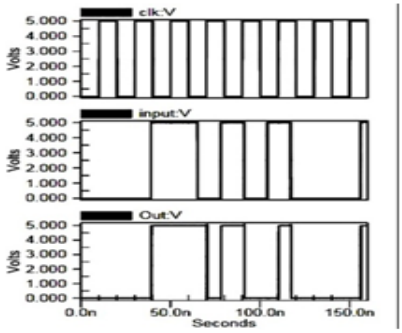

Fig.15: Behavioral response of DETFF using GDI

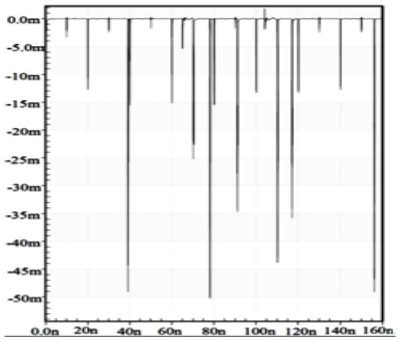

Fig.16: Power Consumed by DETFF using GDI

B. DETFF Based on TransmissionGates

A transmission gate which is illustrated in Fig.17 acts like an analog switch that selectively blocks or passes a signal level from input to output. It comprises of a PMOS transistor and a NMOStransistor.

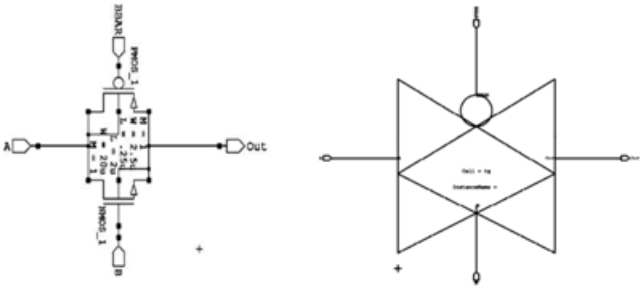

Fig.17: Transmission Gate (TG); (a) schematic, (b) symbol

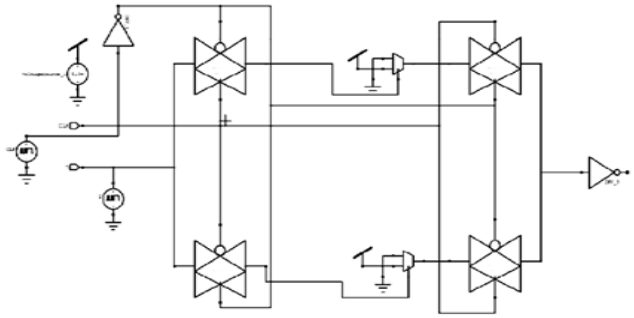

Fig.18: DETFF using TG and GDI based MUX

Fig.18 shows the DETFF based on transmission gates. In this circuit 4 transmission gates, two PMOS transistors and three inverters are used. The upper data path is triggered on the rising edge of the clock and lower data path is triggered on falling edge of the clock. An inverter and a PMOS transistor are used to hold the logic level when the TG is closed. When the data value is high, the inverter switches the signal to low, which will make the PMOS transistor pull the data up to high. When data value is low, the inverter switches the signal to high, which will isolate the data from VDD and keep the value low. This flip-flop provides static functionality for high output since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. This will make the circuit to behave like a dynamiccircuit.

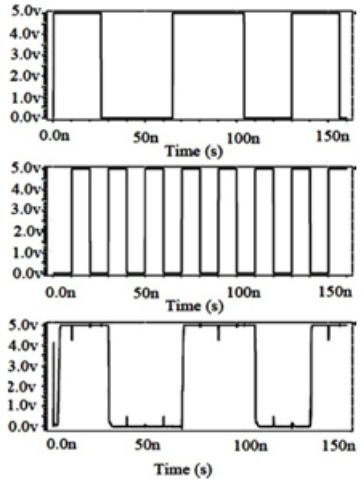

Fig.19: Behavioral response of DETFF using TG

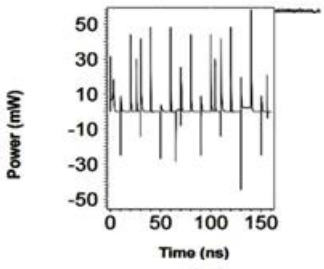

Fig.20: Power Consumed by DETFF using TG

Fig. 19 and fig.20 shows the output and the power consumed of the circuit respectively. We see that the required output has been achieved.

V. SIMULATIONRESULTS

We've used D flip-flops and multiplexers for designing the DETFF. The DETFF based on multiplexers uses less transistors and the average power consumed is drastically less than the DETFF based on D Flip-flop. With an aim to design a low power consumption circuit, we move on to using non-conventional techniques to design our DETFF circuits. This is done in order to reduce the no. of transistors used in the circuit and hence making the circuit power efficient. The non-conventional methods used consume less power and area, reduce propagation delay and hence have less latency than the conventional circuits. We also see that the DETFF based on transmission gates uses the least area as the no. of transistors used are minimum and also the power consumed is less than the other three circuits. The detailed comparisons have been made in table III.

TABLE III. COMPARISON OF VARIOUS DETFF CIRCUITS

Comparison table						
DETFF - Conventional circuits						
	No. of Tr.	**Rise delay**	**Fall delay**	**Avg. time delay**	**Avg. power consump**	**Power delay product**
based on D-FF	**72**	**476.13 ps**	**38.8 ns**	**19.65 ns**	**5.65 mW**	**111.02**
based on MUX	**38**	**784.11 ps**	**436 ps**	**610.14ps**	**1.10 mW**	**0.67**
DETFF - Non-conventional circuits						
based on GDI	**20**	**758.82 ps**	**366 ps**	**562.52ps**	**0.420 mW**	**0.23**
based on TG	**18**	**230.59 ps**	**582 ps**	**406.59 ps**	**1.613 mW**	**0.65**

VI. CONCLUSION

The basic aim of this attempt is to design a low power, low voltage DETFF. DETFFs demonstrate a power saving of 10 percent and an energy saving of as much as 23 percent comparing to the standard SETFF. The non-conventional DETFF based on GDI exhibits the best energy efficient and consumes the least power among the various digital circuits studied. Hence the DETFF circuit based on GDI should be used in the DETFF implementations of VLSI circuits. This will reduce the area overhead of the DETFF designs and improve their performance. It will also encourage further research on DETFF circuits and applications. DETFF circuits could be used to design FIR filter circuits, making them faster and more powerefficient.

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