Comprehensive Study of Flow to Program FPGA Kit Using VHDL

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Abstract- This paper deals with the comprehensive study of flow to program FPGA kit using VHDL. This will enhance the description, simulation and hardware realization of complex system and improvement of the performance of system. VHDL is a hardware description language that is used to model a digital system. The VHDL coding of design is compiled and simulated using Xilinx ISE tool and then incorporate it into FPGA chip to check the feasibility of the proposed design and then the required hardware can be brought into effect.

Keywords- *FPGA, Spartan, VHDL, Xilinx*

I. INTRODUCTION

HDL (hardware description language) and FPGA (field programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. In this paper, we illustrates the FPGA and HDL development and design process using Xilinx software by an example of a comparator. We consider a simple example of comparator that is implemented on a Xilinx-based prototyping board and the codes are synthesized by Xilinx ISE software using VHDL code. Developing a large FPGA-based system is an involved process that consists of many complex transformations and optimization algorithms. Software tools are needed to automate some of the tasks. We use Xilinx ISE package for synthesis and implementation.

Xilinx ISE means Xilinx Integrated Software Environment (ISE). This Xilinx design software suite allow design from design entry to Xilinx device programming. The ISE Project Navigator manages and processes design through several steps in the ISE design flow. These steps are Design Entry, Simulation or Functional Verification, Synthesis, Implementation and Device Configuration.

II. TOOL USED

The Xilinx ISE tools allow the digital design to be entered several ways including graphical schematics, state machine diagrams, VHDL, and Verilog. This paper will focus on VHDL entry. To implement the design, VHDL tool is used. The Xilinx ISE package includes a simple schematic editor utility that can perform schematic capture in graphic format and then convert the diagram into an HDL structural description. The ISE Design Suite is the Xilinx design environment, which allows to take design from design entry to Xilinx device programming. With specific editions for logic, embedded processor, or Digital Signal Processing (DSP) system designers, the ISE Design Suite provides an environment tailored to meet specific design needs.

Xilinx ISE controls all aspects of the development flow. There are four basic steps:

1. Create the design project and HDL codes.
2. Create a test bench and perform RTL simulation.
3. Add a constraint file and synthesize and implement the code.
4. Generate and download the configuration file to an FPGA device.

The ISE design flow is shown in the following figure.

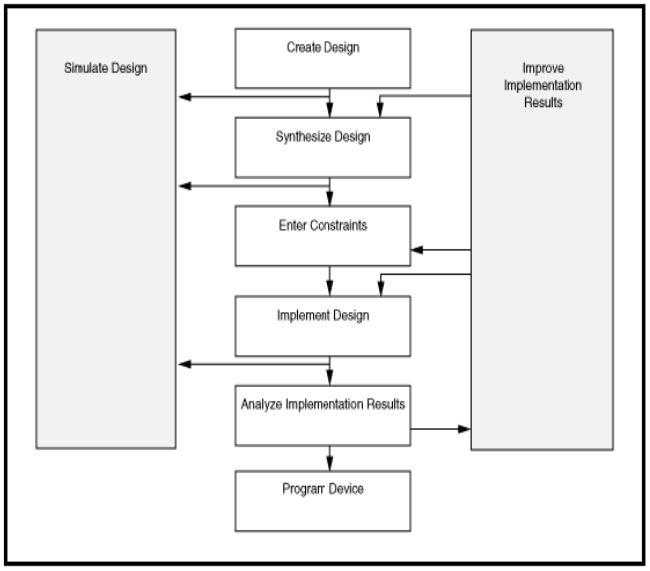


Figure1: ISE Design Flow Overview

III. PROGRAMMING LANGUAGE USED

VHDL is an acronym for VHSIC Hardware Description Language where VHSIC stands for Very High Speed Integrated Circuits. It is a hardware description language that can be used to model a digital system at many level of abstraction, ranging from the algorithmic level to the gate level. VHDL is a standard language design for modelling and synthesizing digital hardware circuit. VHDL was first standardized in 1987, and the standard was called IEEE Std 1076-1987.

VHDL describe the behaviour and structure of system and circuit designs. The VHDL simulation serves as a basis for testing complex designs and validating the design prior to fabrication. This will result in reduction of redesign, the design cycle is shortened, and the product is brought to market sooner.

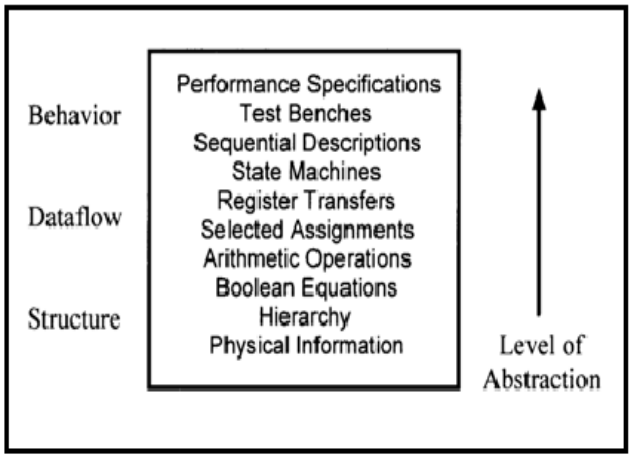


Figure2: Level of abstraction for design description

The VHDL software interface used in the design of system reduces the complexity and also provides a graphic presentation of the system. The prime objective of VHDL when used for systems design is that it allows the behaviour of the required system to be described (modelled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires). This software not only compiles the given VHDL code but also produces waveform results. Graphical blocks, chip design and planner are the advanced options available and are used in the software mentioned. Altera's Quartus II and Xilinx web pack are few of the sophisticated Computer Aided Design (CAD) tools to perform the compilation and simulation of any logic circuit design.

IV.FPGA KIT

A field programmable gate array (FPGA) is a logic device that contains a two-dimensional array of generic logic cells and programmable switches. The conceptual structure of an FPGA device is shown in Figure3. A logic cell can be programmed to perform a simple function, and a programmable switch can be customized to provide interconnections among the logic cells. A custom design can be implemented by specifying the function of each logic cell and selectively setting the connection of each programmable switch. Once the design and synthesis is completed, we can use a simple adaptor cable to download the desired logic cell and switch configuration to the FPGA device and obtain the custom circuit.

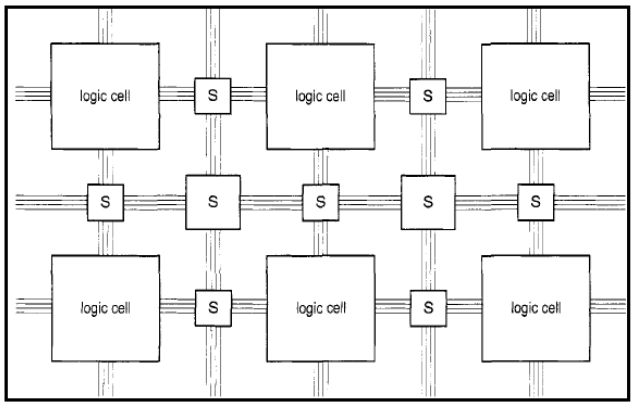


Figure3: Conceptual structure of an FPGA device.

FPGA prototyping board- The Digilent S3 board is based on a Spartan-3 device (usually an XC3S200) and has an array of built-in peripherals. Spartan3 Starter (S3) board contains all the peripherals and no additional accessory module is needed. All HDL codes and discussions can be applied to this board directly.

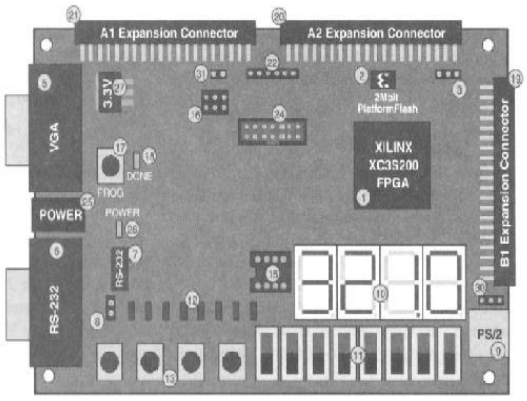


Figure4: Simplified layouts of the FPGA board

Steps by step design process for FPGA-

- Architectural design
- Choice of language(HDL- VHDL/Verilog)
- Editing Programs
- Compiling programs
- Synthesizing the programs(.EDIF)
- Placing and routing programs(.VO, .SDF, .TTF)
- Loading programs to FPGA
- Debugging FPGA programs
- Documenting programs
- Delivering programs

A. An Example:1-bit Comparator

Consider a 1-bit equality comparator with two inputs i0 and i1 and an output eq. The eq signal is asserted when i0 and i1 are equal. The truth table of this circuit is shown in Table. Assume that we want to use basic logic gates, which include not, and, or, and xor cells, to implement the circuit.

One way to describe the circuit is to use a sum-of-products format. The logic expression is

eq = i0.i1 + i0'.i1'

TABLE 1. TRUTH TABLE OF 1-BIT COMPARATOR

input *i0 i1*	output *eq*
0 0	1
0 1	0
1 0	0
1 1	1

Now we examine the language constructs and statements of this. The best way to understand the VHDL program is to think in terms of hardware circuits. This program consists of three portions. The I/0 port portion describes the input and output ports of this circuit, which are i0 and i1 and eq respectively. The signal declaration portion specifies the internal connecting signals, which are p0 and pl. The body portion describes the internal organization of the circuit. There are three continuous assignments in this code. Each can be thought of as a circuit part that performs certain simple logical operations.
The graphical representation of this program is shown in Figure.

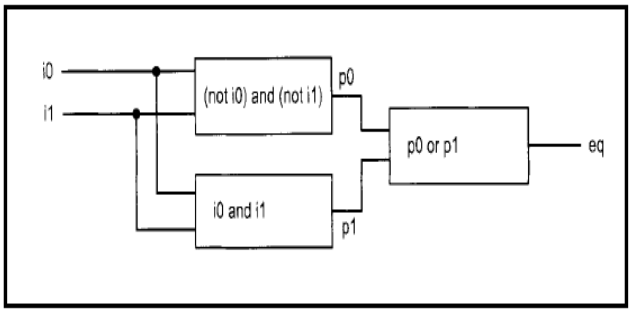


Figure5: Graphical representation of a comparator program

A. *VHDL CODE*

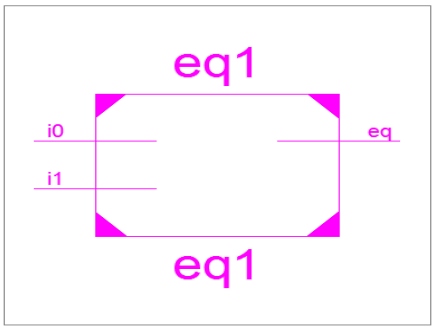
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity eq1 is
   Port ( i0, i1 : in  STD_LOGIC;
eq : out  STD_LOGIC);
end eq1;

architecture Beh_eq1 of eq1 is
signal p0, p1 : STD_LOGIC;
begin
p0 <= (not i0) and (not i1);
p1 <= i0 and i1;
eq <= p0 or p1;
end Beh_eq1;
```

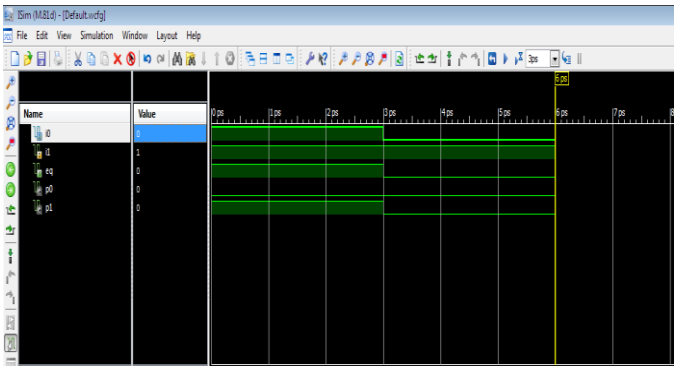
V. SYNTHESIS RESULTS

A. *RTL View*



B. *Simulation Result*

By behavioural simulation for i0-i1 where i0 = 1 & i1 = 1:- eq = 1 and i0 =0 & i1 =1 :- eq =0, gives following results:



VI. CONCLUSION

Programming with FPGA using VHDL enhance the description, simulation and hardware realization of complex system and improve the performance of system. Once the program has been developed, it will be burnt on to a FPGA chip with which the required hardware is obtained. This study helped to understand the complete flow of RTL design, starting from designing a top level RTL module for using hardware description language, VHDL. Verification

of the designed code using simulation techniques, synthesis of code to obtain gate level netlist using Xilinx ISE tool and system was successfully designed and implemented using Very High Speed Hardware Descriptive Language and Xilinx Spatan-3E Field Programmable Gate Array.

VII. REFERENCES

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