# A Single Phase Isolated Transformer based asymmetrical nine level inverter with reduced number of switches

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**Abstract -** The proposed reduced switch multilevel inverter topology makes use of a lower total standing voltage for a required output voltage as compared to the prevailing ones. one among the main advantages of the proposed multilevel inverter over other existing topologies is that, the circuit are often extended to a higher-level inverter, by cascading a couple of proposed inverter modules and may even be extended to the three-phase structure very easily, thereby making the inverter structure simple. thanks to reduced switch count of this proposed topology, the size, weight and price of the switched capacitor multilevel inverter is reduced. The proposed topology produces a staircase waveform with nine level output voltage employing fewer components compared to many existing multilevel inverters. This project deals with harmonic reduction content for switched capacitor multilevel inverter with asymmetric dc sources. It also can step-up the input supply voltage without employing a bulky transformer. Utilizing the available DC sources from renewable energy farms as inputs for one inverter solves the main problem of connecting several inverters in parallel. This inverter inherently solves the matter of capacitor voltage balancing as each capacitor is charged to the worth adequate to one among input voltage every cycle. The modulation technique used for switched capacitor multilevel inverter is Level Shifted Multicarrier Pulse Width Modulation. The entire harmonic distortion is acknowledged through five differing types of level shifted multicarrier pulse width modulation. The performance and feasibility of the proposed multilevel inverter topology is modeled and simulated using MATLAB/Simulink.

## I. INTRODUCTION

Multilevel inverters (MLIs), which came into existence in 1975, are very appropriate when the need of power, voltage becomes high.1,2 The MLIs also ordered a better-quality staircase output voltage waveform with reduced harmonics, total harmonic distortions (THD), reduced dv/dt stress on switches, lesser need of passive filters, lower torque ripple when applied for motor drives and may provide fault tolerant operation. However, a number of the drawbacks related to the foremost popular traditional MLIs like cascaded converter, neutral point clamped (NPC) and flying capacitor (FC), are the need of an outsized number of switching devices and associated gate driver circuitry.4 This increases the complexity of the entire MLI circuit and reduces the reliability in comparison with two-level inverter.5 These drawbacks made researchers specialize in different inverter structures with reduced number of power electronic components.6 one among the well-known reduced switch MLI may be a hybrid structure embodying H-bridge with the other topology This structure can further be sub-categorized as symmetric and asymmetric hybrid MLI topologies.

In symmetrical MLI topologies, the amount of IGBTs keeps on increasing with the rise in number of inverter output voltage levels. On the opposite hand, asymmetrical hybrid multilevel inverter designed with an equivalent number of components has different DC link voltage ratios can generate an output voltage of upper levels and better quality. Nevertheless, the aim of this auxiliary H-bridge in these reduced switch hybrid MLIs is to get the negative polarity voltages like voltages generated by the extent generating part. However, the rating of the switches of this H-bridge becomes adequate to the sum of all the DC voltages, leading to an economically less viable topology. On the opposite hand, the asymmetric cascaded H-bridge (CHB) configuration also uses high-voltage switches in one among the H-bridge, thereby increasing the voltage stress and reducing the efficiency within the configuration. Hence, the hybrid nine-level MLIs proposed.

These exciting features and benefits over DC PDS makes HFAC PDS a brighter alternative for future power net.HFAC PDS architecture consists of a front-end HFAC power source, a HF distribution line and point-of-load transformer modules. These systems employ resonant converters which can enhance efficiency, power factor and energy density, and alleviate adverse EMI effects. In 1980s, NASA make research on HFAC PDS for its space platform . one phase system rated at 25 kW include 20 kHz line frequency and 440Vrms line voltage was done successfully [3]. At this frequency, the energy transferred per cycle which can reduce by 50 times as compared to a 400 Hz system (which may fail to supply efficient and reliable solution [4]. the amount of components is lowered by an element of 5 and power loss are going to be reduced by 67% in comparison to three-phase systems.

High Frequency AC (HFAC) Power Systems provide frequencies above the standard 60 Hz – may have more benefits in certain applications, like telecommunication, computer and aerospace systems has been presented in [7] and also reach lighting systems [2], motor drives, automotive [8] AND circuit drivers [9], especially where small size and weight is more significant (aircraft, ships, etc.), or in situ of variable operating. speed increases efficiency. While 400 Hz systems are widely utilized in aircraft, which never include parallel connected generators that operate at megawatt power levels for several industrial [10] and commercial applications, especially ship and marine systems.

The enhancement in number of voltage levels may have synthesized output waveform with more steps, which reduces the harmonic content within the output. MLI are often generally classified into neutral point clamped, capacitor clamped and cascaded types [11]. Unbalanced DC link capacitor voltage and more component count to get higher output voltage levels are the most drawbacks for diode clamped (DCI) and capacitor clamped (CCI) types, whereas cascaded H-bridge (CHB) MLI need relatively higher number of isolated DC voltage sources to get higher output voltage levels. Coupled inductor based MLI are presented in [12], [13]. This structure is easier but it's not feasible to get higher levels. Renewable energy farms may have more DC sources, usually batteries. These inverters can effectively be needed in such renewable energy based micro grids because it employs multiple DC input sources of various magnitudes. HFAC PDS include compact transformers, smaller filters and high density power converters which can provide several benefits to the micro-grids user. Multilevel inverters (MLI) may overcome exciting features they provide MLI output staircase waveforms which greatly reduce the harmonic content in comparison to standard square wave inverters. MLI are often generally classified into diode clamped, capacitor clamped (also referred to as flying capacitor) and cascaded multilevel inverters [1], [5]. Diode clamped MLI demand several additional diodes for enhancing the output voltage levels and therefore the capacitor voltages are unbalanced and it requires high voltage rating for the blocking diodes. Capacitor clamped MLI also suffer from voltage imbalance issue and wish several additional storage capacitors for increasing the output voltage level which makes it costlier and difficult during the package process. the most drawback in cascaded MLI need separate isolated DC sources.

Symmetric configurations of MLI permit obtaining2N C 1 output levels from N stages while asymmetrical configurations allow a higher number of levels depending on the ratio between the inverter stages. Using a binary geometric progression to dene the ratio between stages, the maximum number of levels at the output will be 2NC1+ 1. Using a ternary geometric progression, the number of levels obtained will be 3N . For example, considering a multilevel inverter with three stages (ND3),a symmetric ratio 1:1:1 allow obtaining a 7-level signal, an asymmetric binary ratio 1:2:4 allows obtaining a 15-level signal and an asymmetric ternary ratio 1:3:9 allows obtaining a 27-level signal. To obtain each level, the converter stages commutate with positive, negative or null contribution. The way in which the stages of the inverter are commutated to obtain different levels is denied as a switching pattern. As it can be noted, after analyzing the case based on geometric progression of ratios, there is a single way to commutate the inverter stages to obtain each desired level. However, for symmetric ratios, there are multiple possibleswitching patterns building the same output signal and givingadditional properties to the inverter operation

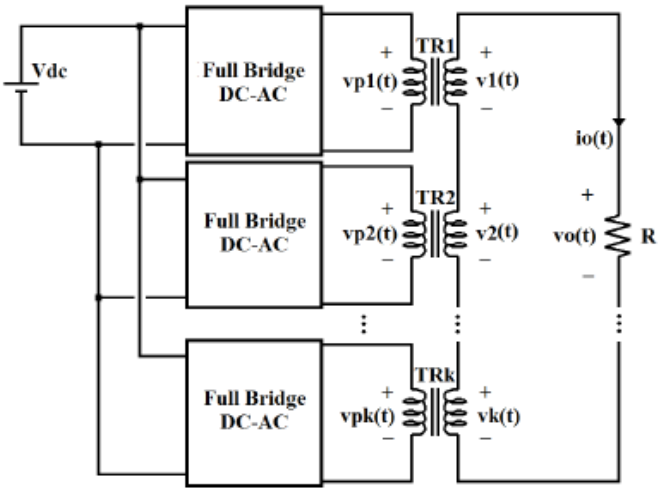


Fig 1: Basic Transformer based cascaded Multilevel Inverter

## II. CASCADED ASYMMETRICAL TRANSFORMER-BASED MULTILEVEL INVERTER

The selected transformer- based topology corresponds to Figure 1 when the number of inverter stages is four. The following subsections give fundamentals to understand inverter operation and design its components.

For N Cascaded H bridge stages the output voltage of the inverter computed as follows:

$V_o(wt)=V_1(wt)+V_2(wt)+\ldots\ldots..V_N(wt)$

$\sum_{K=1}^{N} V_K(wt)\text{--}\rightarrow 1$

Where $V_k(wt)$ is the instantaneous output voltage of each stage which is defined by

$V_K(wt = V_{dc}{*}T_{rk}S_{fk}$-→2

Where Vdc is the magnitude in the output voltage Trk is turns ratio of the transformer. Sfk is the instantaneous switching operation.Sfk takes the -1 0 1. Thus sum of the outputs are obtaining a positive signal with M positive integer values. Multilevel inverters have made another surge of enthusiasm for industry and investigation. While the set up topologies have wound up being an achievable choice in a broad assortment of high-power medium-voltage applications, there has been a dynamic energy for the advancement of fresher topologies. Decrease in general part considers contrasted with the traditional topologies has been a vital objective in the as of late presented topologies. In this paper, a segment of the starting late proposed multilevel inverter topologies with decreased power switch number are studied and evaluated. This paper will serve as an associate and a redesign with these topologies, both to the extent of subjective and quantitative parameters.

## III. TRANSFORMERS TURNS RATIO

The maximum output voltage Vmax can be obtained as the algebraic sum of the stage output voltages, each of them having a maximum defined by Vkmax. Considering a waveform with positive integer levels which is build using an inverter with N stages, each of one having a weight wk, these weights define the ratio between stages (w1 V w2 V w3 V w4). Then, the turns ratio for the transformer of each stage 1 VTRk is obtained as the relation between its maximum output voltage Vkmax and the input voltage Vdc. Design can be performed by using the following expression:

$T_{rk} = \frac{V_{kmax}}{V_{dc}} = \frac{w_{kV_{max}}}{MV_{dc}}$ --→3

## IV. OUTPUT POWER OF THE INVERTER STAGES

The output voltage of each inverter stage is a square wave that can be modeled using Fourier expression

$V_k(wt)=V1_{k-max}$*sin (wt)+$\sum_{j=2}^{\propto} V_{j-max}$→4

## V. THD AND RMS AS FUNCTIONS OF THE NUMBER OF INTEGER LEVELS

The number of levels from which the sinusoidal signal is obtained determines the total harmonic distortion (THD) of the output voltage. Hence, with a higher number of levels, we obtain a lower harmonic distortion, but a greater amount of stages is also required in the inverter. The root mean square (RMS) value of the output signal of the inverter also depends on the number of levels but in a smaller proportion. To evaluate the quality of the output waveform, THD and RMS values are determined. The RMS value considering the symmetry of the signal is defined by

$V_0 = \frac{v_{max}}{M}\sqrt{M^2 - \frac{2}{M}\sum_{m=1}^{M}(2m-1)\sin^{-1}(\frac{2m-1}{2M})}$--→5

On the other hand, the output signal defined from the Fourier series expansion can be expressed as follows

$$V_0(wt) = \sum_{n=1}^{\infty}(a_n \cos nwt + b_n \sin nwt) \; ---\rightarrow 6$$

TRANSFORMERS TURNS RATIO

The maximum output voltage Vmax can be obtained as the algebraic sum of the stage output voltages, each of them having a maximum defined by Vkmax. Considering a waveform with M positive integer levels which is build using an inverter with N stages, each of one having a weight wk, these weights define the ratio between stages (w1 : w2 : w3 : w4). Then, the turns ratio for the transformer of each stage 1: TRk is obtained as the relation between its maximum output voltage Vkmax and the input voltage Vdc. Design can be performed by using the following expression

$TR_k = \frac{V_{kmax}}{V_{dc}} = \frac{w_k V_{max}}{MV_{dc}}$→7

**Pulse width Modulation Technique**

A hysteresis control based approach is presented to obtain Closed-loop regulation of the output voltage. The idea is to enforce the RMS value of the output voltage to be constrained into an acceptable range around the nominal value the higher the number of levels the higher the quality of the output signal. Although the power distribution is optimized for the five possible signals, the best balance corresponds to the nominal case of 9 -levels. Taking measurement of the output voltage, it is determined if the voltage increases or decreases outside the hysteresis band enforcing the change of the switching pattern.

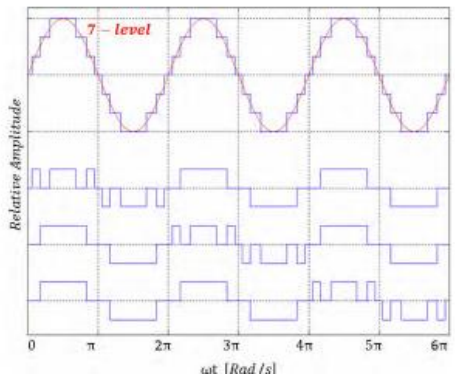


Fig2 : Repeating sequence method for generation of the multilevel sinusoidal signal from three inverter stage

## VI. SIMULINK DESIGN & RESULTS

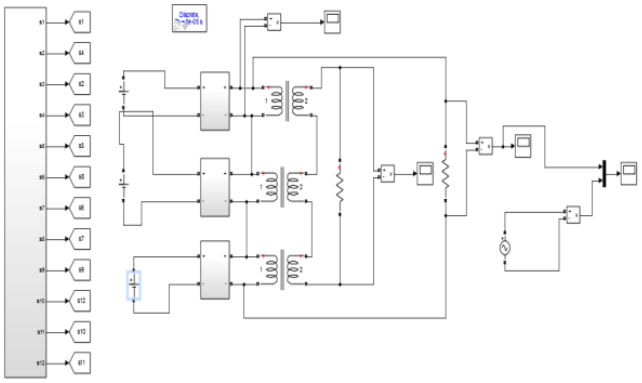

Fig 3: Simulink Design of A single phase Transformer based Asymmetrical Seven Level Inverter

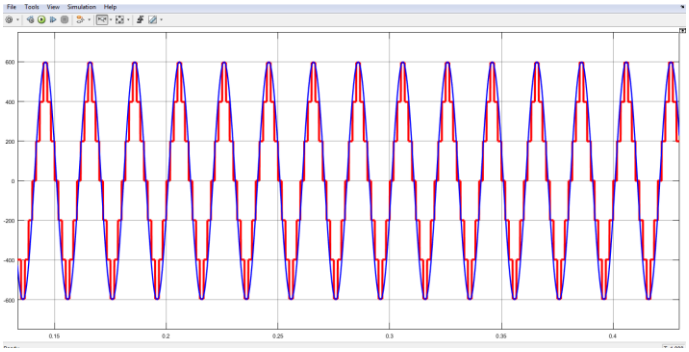

Fig 4: Seven Level Multilevel Asymmetrical Inverter

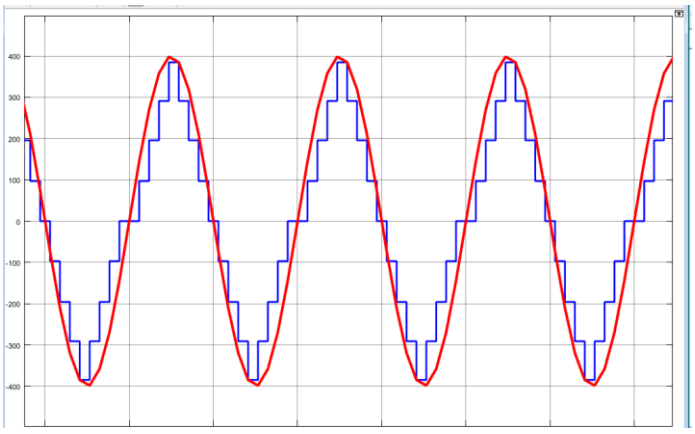

Fig 5: Single stage Transformer based Multilevel Inverter Asymmetric 9 Level Inverter Topology

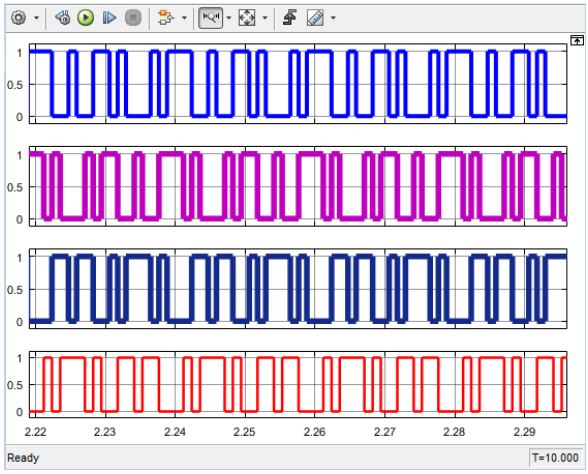


Fig 6: Gate Pulses for Asymmetrical Multilevel Inverter

## VII. CONCLUSION

This project has presented a method to enforce balanced power distribution on a transformer less-based cascaded asymmetrical multilevel inverter. The method is founded on the selection of an optimal switching pattern for each stage of the inverter given by an off-line algorithm. The proposal has been developed using Asymmetrical based hybrid inverter output voltage signal obtained from a four- stage common DC source inverter after selecting the best combination of integer weights for the stages of the inverter. The output power and harmonic distortion have and a balanced distribution deviation lower than 10%. This appropriate behavior of the system has been verified for resistive loads and improves what has been reported as yet in the technical literature. It has been demonstrated that the proposed asymmetric ratio 1:3 allows that the inverter can be controlled using optimized switching patterns. The patterns can be stored in a digital device to easily support a voltage regulation control loop improving the inverter performance while avoiding the use of high-frequency modulation. Current research and future work are oriented to this goal together with the integration of fault-tolerant properties in one of the inverter stages.

## VIII. REFERENCES

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