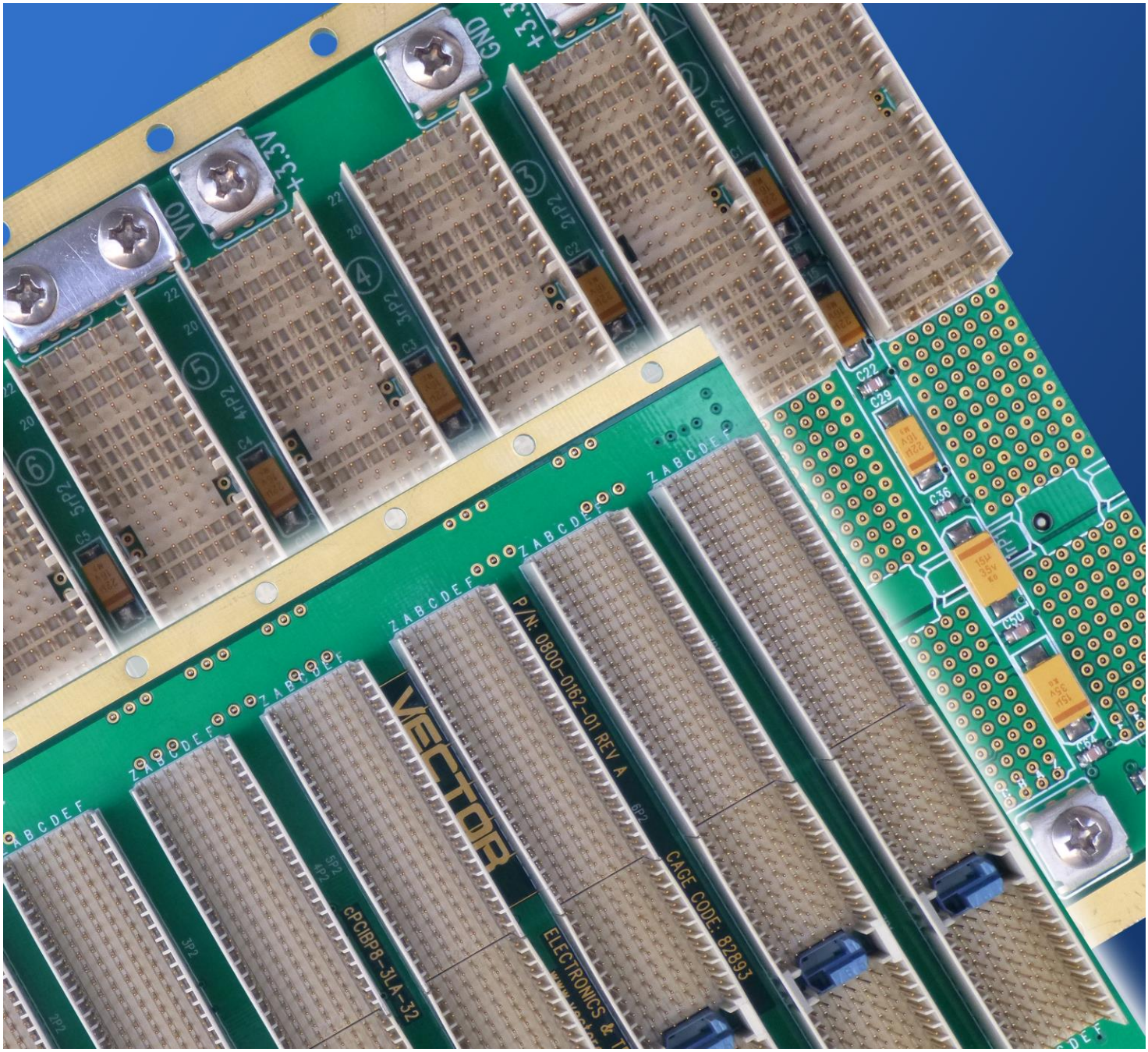
VECTOR
ELECTRONICS & TECHNOLOGY, INC.

**ITAR REGISTERED**
**ISO 9001:2008 & AS9100C CERTIFIED**

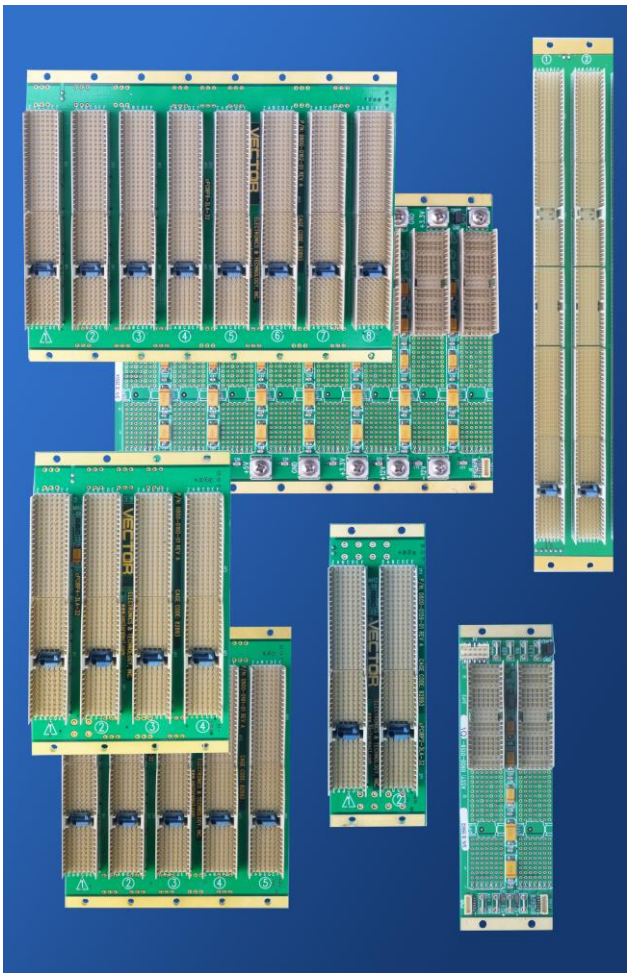
MADE IN U. S. A.

# User Manual
# CompactPCI Backplanes




IN404 REV. A, 03/26/2014

Vector Electronics & Technology, Inc.
11115 Vanowen Street,
North Hollywood, CA 91605
Phone : (800) 423-5659
www.vectorelect.com



## What is CompactPCI®

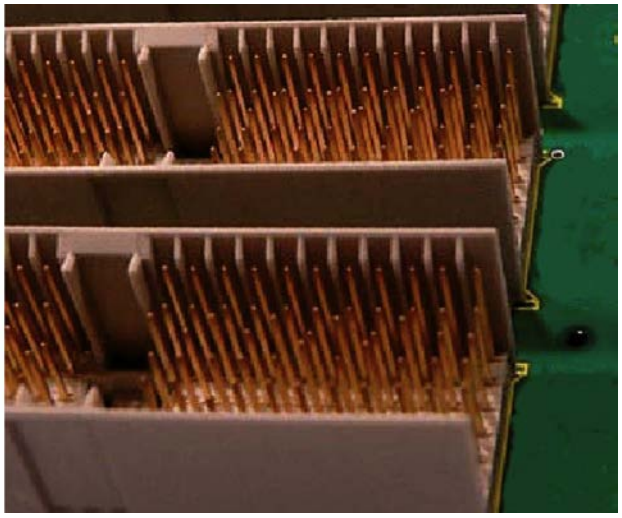
The latest specification for PCI-based industrial computers is called CompactPCI. It is electrically, a superset of desktop PCI with a different physical form factor. CompactPCI utilizes the Eurocard form factor popularized by the VME bus.

Defined for both 3U (100mm by 160 mm) and 6U (160mm by 233 mm) card sizes, CompactPCI has the following features:

- Standard Eurocard dimensions (compliant with IEEE 1101.10 mechanical standards)
- High density 2mm Pin-and-Socket connectors (IEC approved)
- Excellent shock and vibration characteristics
- Metal front panel
- User I/O connections on front or rear of module
- Uses standard PCI silicon, manufactured in large volumes
- Staged power pins for Hot Swap capability
- Eight slots in basic configuration.

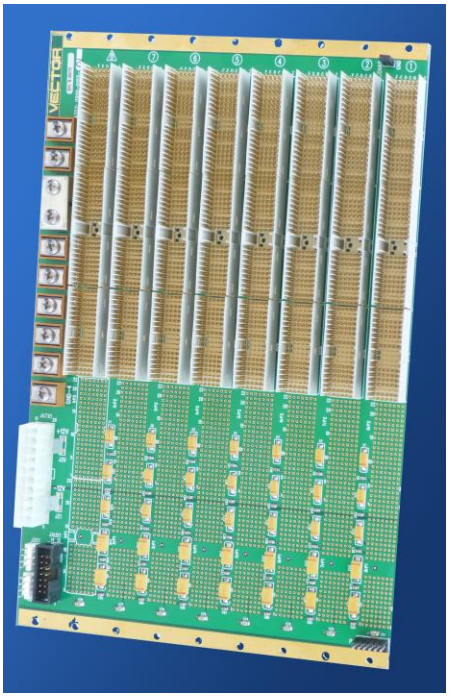
## What is PICMG

PICMG (**P**CI **I**ndustrial **C**omputer **M**anufacturers **G**roup) is a consortium of over 600 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications. The members of the consortium have a long history of developing leading edge products for these industries.



## CompactPCI Connectors

The CompactPCI connectors are shielded 2mm pitch, 5+2 row connector, compliant to IEC 61076-4-101. Main features of this connectors are the pin stagging for hot swap and shielding for EMI/RFI protection.

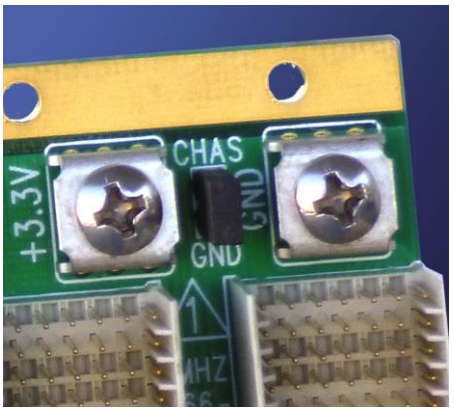


## CompactPCI Backplanes

Vector CompactPCI backplanes are fully compliant to the latest PICMG specifications.

| | |
|---|---|
| PICMG 2.0 R 3.0 | cPCI Core Specification PICMG |
| PICMG 2.1 | cPCI Hot Swap Specification |
| PICMG 2.9 | System Management Bus Specification |
| PICMG 2.10 | Keying Specification |

Vector CompactPCI backplanes are specially designed to achieve exellent power distribution, best signal integrity, virtually zero cross talk, and minimum clock skew. The SMD components used on CompactPCI backplanes lead to a much lower failure rate than conventional components.

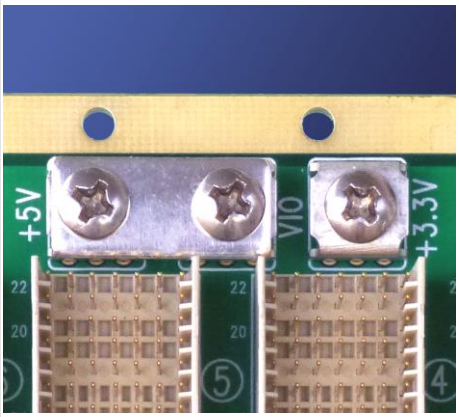



## CompactPCI Backplane Features

### Connection to ChassisGND

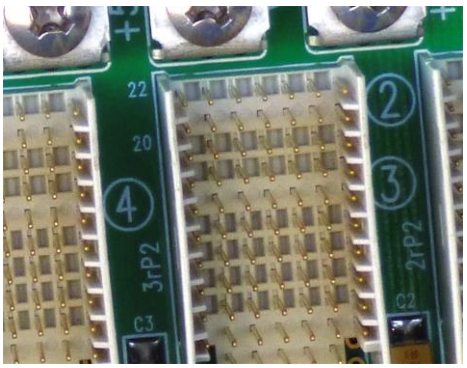
cPCI backplanes have a jumper between DigitalGND and ChassiGND to either isolate or connect between BackplaneGND and Chassis GND.

If noise reduction shall be achieved by connecting DigitalGND to ChassisGND jumper in installed position is recommended instead of isolating BackplaneGND and Chassis GND.




### VI/O

CompactCPCI backplanes have a complete power plane for the VI/O voltage. The VI/O plane can be connected using a bridge on the power bugs to either +3.3V or +5V.



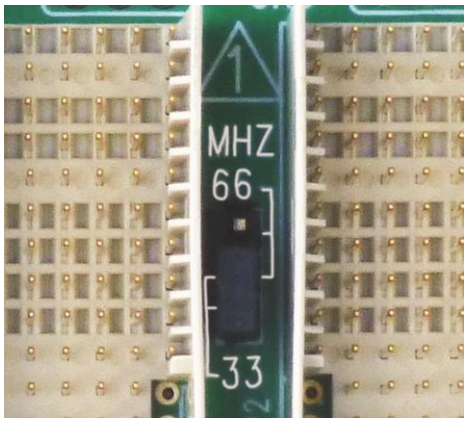

## Geographical Addressing (GA)

Geographical addressing is set by default to start from number one from left (upper) position within the chassis.

### Physical Slot Addresses

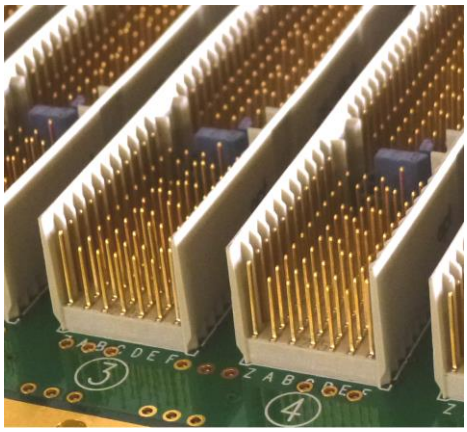
| Physical Slot# | 0(1) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GA[4] (J2-A22) | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| GA[3] (J2-B22) | GND | GND | GND | GND | GND | GND | GND | GND | open | open | open |
| GA[2] (J2-C22) | GND | GND | GND | GND | open | open | open | open | GND | GND | GND |
| GA[1] (J2-D22) | GND | GND | open | open | GND | GND | open | open | GND | GND | open |
| GA[0] (J2-E22) | GND | open | GND | open | GND | open | GND | open | GND | open | GND |

| Physical Slot# | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GA[4] (J2-A22) | GND | GND | GND | GND | GND | open | open | open | open | open | open |
| GA[3] (J2-B22) | open | open | open | open | open | GND | GND | GND | GND | GND | GND |
| GA[2] (J2-C22) | GND | open | open | open | open | GND | GND | GND | GND | open | open |
| GA[1] (J2-D22) | open | GND | GND | open | open | GND | GND | open | open | GND | GND |
| GA[0] (J2-E22) | open | GND | open | GND | open | GND | open | GND | open | GND | open |




## 66MHz Operation

cPCI backplanes are designed in accordance with the requirements of cPCI Core Specification PICMG 2.0R3.0, backplanes up to 5 Slots are possible to have 66MHz operation. Backplanes of higher slot count are set for 33MHz operation only. Backplanes 5 slots or less have jumper which can be set to either 66 or 33MHz operation.




## Hot Swap

cPCI backplanes fulfill the requirements for Basic Hot Swap of the Hot Swap Specification PICMG 2.1 R2.0. The P1 connector on cPCI backplanes has pin stagging needed for hot swap capabilities.

## Pin Assignment CPCI Connectors

### Table 1: CompactPCI System Slot 64-Bit Connector Pin Assignment

| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | GND | CLK6 | GND | RSV | RSV | RSV | GND |
| 20 | GND | CLK5 | GND | RSV | GND | RSV | GND |
| 19 | GND | GND | GND | SMB_SDA(11) | SMB_SCL(11) | SMB_ALERT#(11) | GND |
| 18 | GND | BRSVP2A18 | BRSVP2B18 | BRSVP2C18 | GND | BRSVP2E18 | GND |
| 17 | GND | BRSVP2A17 | GND | PRST# | REQ6# | GNT6# | GND |
| 16 | GND | BRSVP2A16 | BRSVP2B16 | DEG# | GND | BRSVP2E16 | GND |
| 15 | GND | BRSVP2A15 | GND | FAL# | REQ5# | GNT5# | GND |
| 14 | GND | AD[35] | AD[34] | AD[33] | GND | AD[32] | GND |
| 13 | GND | AD[38] | GND | V(I/O)(2) | AD[37] | AD[36] | GND |
| 12 | GND | AD[42] | AD[41] | AD[40] | GND | AD[39] | GND |
| 11 | GND | AD[45] | GND | V(I/O)(2) | AD[44] | AD[43] | GND |
| 10 | GND | AD[49] | AD[48] | AD[47] | GND | AD[46] | GND |
| 9 | GND | AD[52] | GND | V(I/O)(2) | AD[51] | AD[50] | GND |
| 8 | GND | AD[56] | AD[55] | AD[54] | GND | AD[53] | GND |
| 7 | GND | AD[59] | GND | V(I/O)(2) | AD[58] | AD[57] | GND |
| 6 | GND | AD[63] | AD[62] | AD[61] | GND | AD[60] | GND |
| 5 | GND | C/BE[5]# | GND | V(I/O)(2) | C/BE[4]# | PAR64 | GND |
| 4 | GND | V(I/O)(2) | BRSVP2B4 | C/BE[7]# | GND | C/BE[6]# | GND |
| 3(3) | GND | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2(3) | GND | CLK2 | CLK3 | SYSEN#(3) | GNT2# | REQ3# | GND |
| 1(3) | GND | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND |
| 24 | GND | AD[1] | 5V | V(I/O)(2),(4) | AD[0] | ACK64# | GND |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V(4) | AD[2] | GND |
| 22 | GND | AD[7] | GND | 3.3V(4) | AD[6] | AD[5] | GND |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND |
| 20 | GND | AD[12] | GND | V(I/O)(2) | AD[11] | AD[10] | GND |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND(4) | AD[13] | GND |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND |
| 17 | GND | 3.3V | IPMB_SCL | IPMB_SDA | GND(4) | PERR# | GND |
| 16 | GND | DEVSEL# | GND | V(I/O)(2) | STOP# | LOCK# | GND |
| 15 | GND | 3.3V | FRAME# | IRDY# | GND | TRDY# | GND |
| 14 | | | | KEY AREA | | | |
| 13 | | | | KEY AREA | | | |
| 12 | | | | KEY AREA | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND(4) | C/BE[2]# | GND |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND |
| 9 | GND | C/BE[3]# | GND | AD[23] | GND(4) | AD[22] | GND |
| 8 | GND | AD[26] | GND | V(I/O)(2) | AD[25] | AD[24] | GND |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND(4) | AD[27] | GND |
| 6 | GND | REQ0# | GND | 3.3V(4) | CLK0 | AD[31] | GND |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND(4) | GNT0# | GND |
| 4 | GND | IPMB_PWR | HEALTHY#(13) | V(I/O)(2),(4) | INTP | INTS | GND |
| 3 | GND | INTA# | INTB# | INTC# | 5V(4) | INTD# | GND |
| 2 | GND | BRSVP1A2(10) | 5V | BRSVP1C2(10) | RSV(10) | RSVI(10) | GND |
| 1 | GND | 5V | -12V | BRSVP1C1(10) | +12V | 5V | GND |
| Pin | Z | A | B | C | D | E | F |

## Table 2: CompactPCI Peripheral Slot 64-Bit Connector Pin Assignment (1)(10, 11)

| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | GND | RSV | RSV | RSV | RSV | RSV | GND |
| 20 | GND | RSV | RSV | RSV | GND | RSV | GND |
| 19 | GND | RSV | RSV | RSV | RSV | RSV | GND |
| 18 | GND | BRSVP2A18 | BRSVP2B18 | BRSVP2C18 | GND | BRSVP2E18 | GND |
| 17 | GND | BRSVP2A17 | GND | RSV | RSV | RSV | GND |
| 16 | GND | BRSVP2A16 | BRSVP2B16 | RSV | GND | BRSVP2E16 | GND |
| 15 | GND | BRSVP2A15 | GND | RSV | RSV | RSV | GND |
| 14 | GND | AD[35] | AD[34] | AD[33] | GND | AD[32] | GND |
| 13 | GND | AD[38] | GND | V(I/O)(2) | AD[37] | AD[36] | GND |
| 12 | GND | AD[42] | AD[41] | AD[40] | GND | AD[39] | GND |
| 11 | GND | AD[45] | GND | V(I/O)(2) | AD[44] | AD[43] | GND |
| 10 | GND | AD[49] | AD[48] | AD[47] | GND | AD[46] | GND |
| 9 | GND | AD[52] | GND | V(I/O)(2) | AD[51] | AD[50] | GND |
| 8 | GND | AD[56] | AD[55] | AD[54] | GND | AD[53] | GND |
| 7 | GND | AD[59] | GND | V(I/O)(2) | AD[58] | AD[57] | GND |
| 6 | GND | AD[63] | AD[62] | AD[61] | GND | AD[60] | GND |
| 5 | GND | C/BE[5]# | GND | V(I/O)(2) | C/BE[4]# | PAR64 | GND |
| 4 | GND | V(I/O)(2) | BRSVP2B4 | C/BE[7]# | GND | C/BE[6]# | GND |
| 3(3) | GND | RSV | GND | RSV | RSV | RSV | GND |
| 2(3) | GND | RSV | RSV | UNC(3) | RSV | RSV | GND |
| 1(3) | GND | RSV | GND | RSV | RSV | RSV | GND |
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND |
| 24 | GND | AD[1] | 5V | V(I/O)(2),(4) | AD[0] | ACK64# | GND |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V(4) | AD[2] | GND |
| 22 | GND | AD[7] | GND | 3.3V(4) | AD[6] | AD[5] | GND |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND |
| 20 | GND | AD[12] | GND | V(I/O)(2) | AD[11] | AD[10] | GND |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND(4) | AD[13] | GND |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND |
| 17 | GND | 3.3V | IPMB_SCL | IPMB_SDA | GND(4) | PERR# | GND |
| 16 | GND | DEVSEL# | GND | V(I/O)(2) | STOP# | LOCK# | GND |
| 15 | GND | 3.3V | FRAME# | IRDY# | BD_SEL#(6) | TRDY# | GND |
| 14 | | | | KEY AREA | | | |
| 13 | | | | KEY AREA | | | |
| 12 | | | | KEY AREA | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND(4) | C/BE[2]# | GND |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND |
| 9 | GND | C/BE[3]# | IDSEL(6) | AD[23] | GND(4) | AD[22] | GND |
| 8 | GND | AD[26] | GND | V(I/O)(2) | AD[25] | AD[24] | GND |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND(4) | AD[27] | GND |
| 6 | GND | REQ# | GND | 3.3V(4) | CLK | AD[31] | GND |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND(4) | GNT# | GND |
| 4 | GND | IPMB_PWR | HEALTHY#(13) | V(I/O)(2),(4) | INTP | INTS | GND |
| 3 | GND | INTA# | INTB# | INTC# | 5V(4) | INTD# | GND |
| 2 | GND | BRSVP1A2(10) | 5V | BRSVP1C2(10 | RSV(10) | RSV(10) | GND |
| 1 | GND | 5V | -12V | BRSVP1C1(10 | +12V | 5V | GND |
| Pin | Z | A | B | C | D | E | F |

## Table 3: CompactPCI System Slot 32-Bit (Rear Panel I/O) Connector Pin Assignment

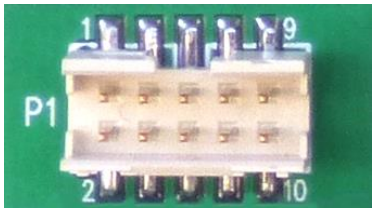
| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | GND | CLK6 | GND | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 20 | GND | CLK5 | GND | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 19 | GND | GND | GND | SMB_SDA(11) | SMB_SCL(11) | SMB_ALERT#(11) | GND |
| 18 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 17 | GND | BP(I/O) | BP(I/O) | PRST# | REQ6# | GNT6# | GND |
| 16 | GND | BP(I/O) | BP(I/O) | DEG# | GND | BP(I/O) | GND |
| 15 | GND | BP(I/O) | BP(I/O) | FAL# | REQ5# | GNT5# | GND |
| 14 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 13 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 12 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 11 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 10 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 9 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 8 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 7 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 6 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 5 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 4 | GND | V(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 3(3) | GND | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| 2(3) | GND | CLK2 | CLK3 | SYSEN#(3) | GNT2# | REQ3# | GND |
| 1(3) | GND | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND |
| 24 | GND | AD[1] | 5V | V(I/O)(2),(4) | AD[0] | ACK64# | GND |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V(4) | AD[2] | GND |
| 22 | GND | AD[7] | GND | 3.3V(4) | AD[6] | AD[5] | GND |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND |
| 20 | GND | AD[12] | GND | V(I/O)(2) | AD[11] | AD[10] | GND |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND(4) | AD[13] | GND |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND |
| 17 | GND | 3.3V | IPMBSCL | IPMBSDA | GND(4) | PERR# | GND |
| 16 | GND | DEVSEL# | GND | V(I/O)(2) | STOP# | LOCK# | GND |
| 15 | GND | 3.3V | FRAME# | IRDY# | GND | TRDY# | GND |
| 14 | | | | KEY AREA | | | |
| 13 | | | | KEY AREA | | | |
| 12 | | | | KEY AREA | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND(4) | C/BE[2]# | GND |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND |
| 9 | GND | C/BE[3]# | GND | AD[23] | GND(4) | AD[22] | GND |
| 8 | GND | AD[26] | GND | V(I/O)(2) | AD[25] | AD[24] | GND |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND(4) | AD[27] | GND |
| 6 | GND | REQ0# | GND | 3.3V(4) | CLK0 | AD[31] | GND |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND(4) | GNT0# | GND |
| 4 | GND | IPMBPWR | HEALTHY#(13) | V(I/O)(2),(4) | INTP | INTS | GND |
| 3 | GND | INTA# | INTB# | INTC# | 5V(4) | INTD# | GND |
| 2 | GND | BRSVP1A2(10) | 5V | BRSVP1C2(10) | RSV(10) | RSV(10) | GND |
| 1 | GND | 5V | -12V | BRSVP1C1(10) | +12V | 5V | GND |
| Pin | Z | A | B | C | D | E | F |

**Table 4: CompactPCI Peripheral Slot 32Bit (Rear-Panel I/O) Connector Pin Assignments (1)(3)(8,9)**

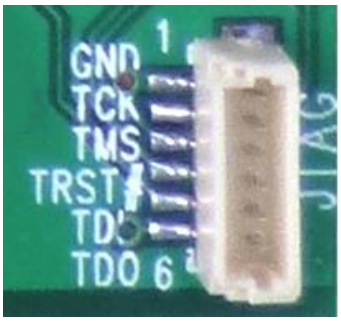
| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND |
| 21 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 20 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 19 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 18 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 17 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 16 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 15 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 14 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 13 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 12 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 11 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 10 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 9 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 8 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 7 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 6 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 5 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 4 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 3 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 2 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 1 | GND | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | BP(I/O) | GND |
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND |
| 24 | GND | AD[1] | 5V | V(I/O)(2),(4) | AD[0] | ACK64# | GND |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V(4) | AD[2] | GND |
| 22 | GND | AD[7] | GND | 3.3V(4) | AD[6] | AD[5] | GND |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND |
| 20 | GND | AD[12] | GND | V(I/O)(2) | AD[11] | AD[10] | GND |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND(4) | AD[13] | GND |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND |
| 17 | GND | 3.3V | IPMB_SCL | IPMB_SDA | GND(4) | PERR# | GND |
| 16 | GND | DEVSEL# | GND | V(I/O)(2) | STOP# | LOCK# | GND |
| 15 | GND | 3.3V | FRAME# | IRDY# | BD_SEL#(5) | TRDY# | GND |
| 14 | | | | KEY AREA | | | |
| 13 | | | | KEY AREA | | | |
| 12 | | | | KEY AREA | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND(4) | C/BE[2]# | GND |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND |
| 9 | GND | C/BE[3]# | IDSEL(6) | AD[23] | GND(4) | AD[22] | GND |
| 8 | GND | AD[26] | GND | V(I/O)(2) | AD[25] | AD[24] | GND |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND(4) | AD[27] | GND |
| 6 | GND | REQ# | GND | 3.3V(4) | CLK | AD[31] | GND |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND(4) | GNT# | GND |
| 4 | GND | IPMB_PWR | HEALTHY#(13) | V(I/O)(2),(4) | INTP | INTS | GND |
| 3 | GND | INTA# | INTB# | INTC# | 5V(4) | INTD# | GND |
| 2 | GND | BRSVP1A2(10) | 5V | BRSVP1C2(10) | RSV(10) | RSV(10) | GND |
| 1 | GND | 5V | -12V | BRSVP1C1(10) | +12V | 5V | GND |
| Pin | Z | A | B | C | D | E | F |

## Notes for CompactPCI Pin Assignment Tables 1 through 4

1. These diagrams define the pin assignments from the front of the system chassis.
2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.
3. Connector P2 pin C2 is grounded at the System Slot only. Peripheral slots leave C2 unconnected (UNC). Boards that use this signal (e.g., CPU boards that may be used in the System Slot or Peripheral Slot) shall provide a local pull-up to V(I/O). Boards designed for System Slot only use should tie this pin directly to the ground plane.
4. The following signals are long (level 3) pins in P1 for early power to hot swap boards: D3, D5, D7, D9, D11, D17, D19, D23, C4, C6, C22, C24.
5. Connector P1 pin D15 (BD_SEL#) is defined as a short length pin and is used for the final connection sequence by hot swap boards. Connector P1 pin B9 (IDSEL) is defined as a short length pin. Refer to PICMG 2.1, CompactPCI Hot Swap Specification for details.
6. These signals are defined as bussed reserve (BRSVPxxx) signals. They were defined as PCI cache signals SDONE# and SBO# (Defined in the PCI 2.1 Specification) in earlier revisions of this specification.
7. CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to allow the connectors to start at the bottom of the board and "grow" upward from J1/P1 through J5/P5.
8. BP(I/O) signals are defined as "long" tail connectors with 16.0 mm tails. Refer to IEEE 1101.11 for details. All other signals in P1 and P2 are defined to be "short" tail connectors with 4.5 mm tails.
9. BRSVPxxx signals accommodate PCI reserved signals. Bus segments shall bus these signals between connectors.
10. Usage of JTAG signals is discouraged. These signal definitions will be redefined in a future revision of the CompactPCI specification. Backplanes shall bus pins A2 (TCK), C2 (TMS) and C1 (TRST#) to all CompactPCI Slots. Pins D2 (TDO) and E2 (TDI) should be non-bussed.
11. System slot connector P2, pins C19 (SMBB_SDA), D19 (SMBB_SCL) and E19 (SMB_RSV) have been defined by the System Management Subcommittee as the appropriate rear-panel I/O pins to be used for a secondary $I^2C$ bus local to the system board. Refer to the PICMG 2.9 System Management Specification for further information.
12. Signals IDSEL and BD_SEL# are connected to GND on the System Slot. The Dual Host Subcommittee may further define their use on the system slot.
13. P1 pin B4 is reserved for HEALTHY#. Backplane must leave this pin open and include a bypass capacitor, refer to section 3.2.10 and the CompactPCI Hot Swap Specification, PICMG 2.1 for details.

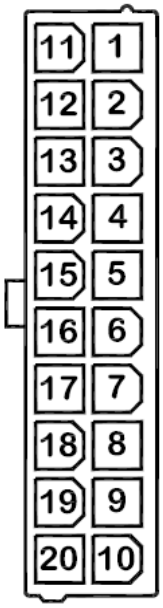







## Utility, IPMB, JTAG Connectors

| PIN # | 10-PIN UTILITY CONNECTOR (P1) | IPMB CONNECTOR | JTAG CONNECTOR |
|---|---|---|---|
| 1 | PRST# | IPMB_SCL | GND |
| 2 | FAL# | GND | TCK |
| 3 | DEG# | IPMB_SDA | TMS |
| 4 | +3.3V SENSE | IPMB_PWR | TRST# |
| 5 | +3.3V | SMB_RSV | TDI |
| 6 | GND SENSE (3.3V) | GND | TDO |
| 7 | +5V | | |
| 8 | +5V SENSE | | |
| 9 | GND | | |
| 10 | GND SESNSE (5V) | | |



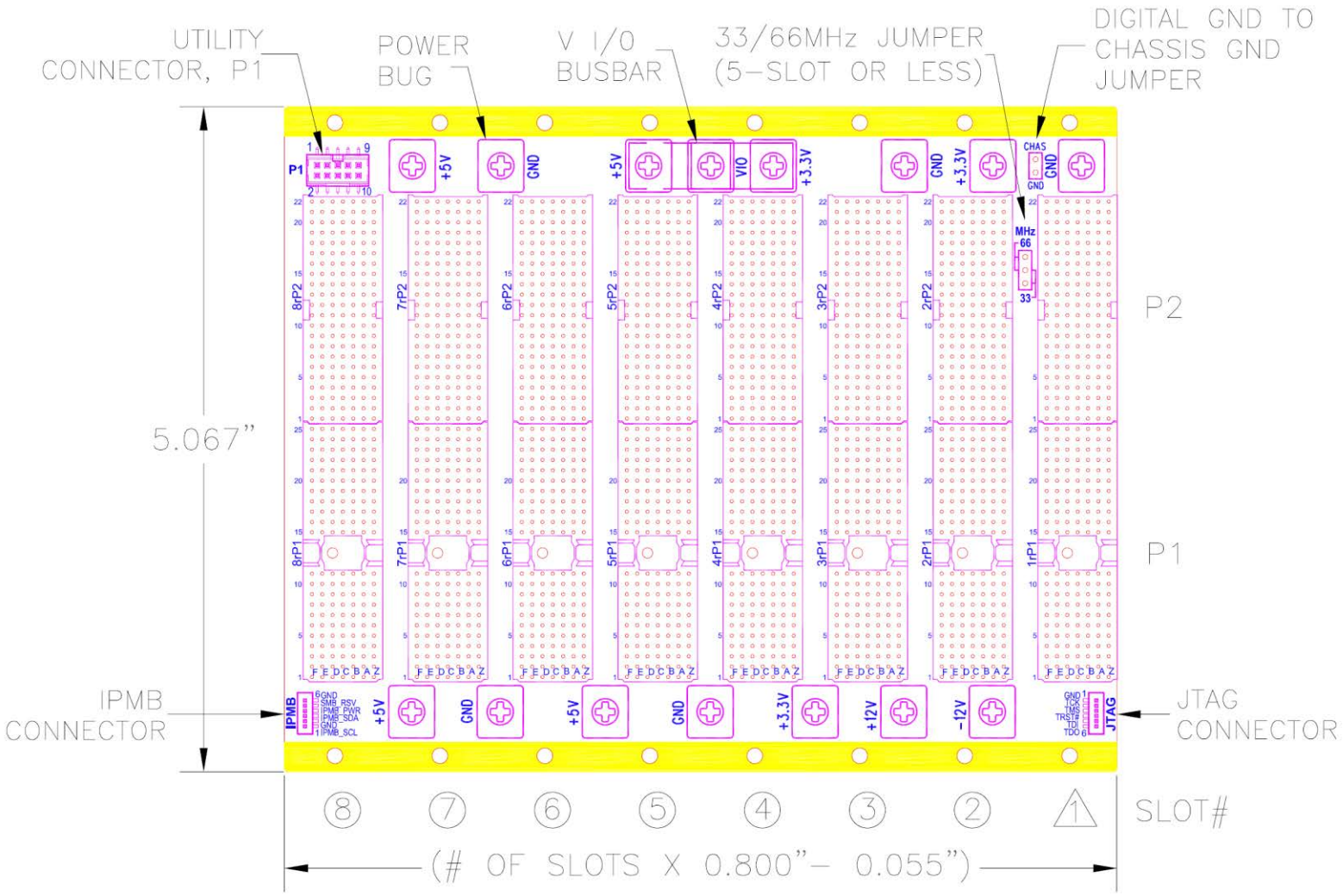

## ATX Connector

cPCI backplanes with system slots on right have option to supply power from either 20-pin ATX connector or power bugs/ faston blades. Pin assignments for ATX connector is shown in below table.

| PIN # | ATX CONNECTOR | PIN # | ATX CONNECTOR |
|---|---|---|---|
| 1 | +3.3V | 11 | +3.3V |
| 2 | +3.3V | 12 | -12V |
| 3 | GND | 13 | GND |
| 4 | +5V | 14 | PS_ON OR INH# (NOTE 2) |
| 5 | GND | 15 | GND |
| 6 | +5V | 16 | GND |
| 7 | GND | 17 | GND |
| 8 | PW_OK OR FAL# (NOTE 1) | 18 | -5V |
| 9 | +5V SB | 19 | +5V |
| 10 | +12V | 20 | +5V |

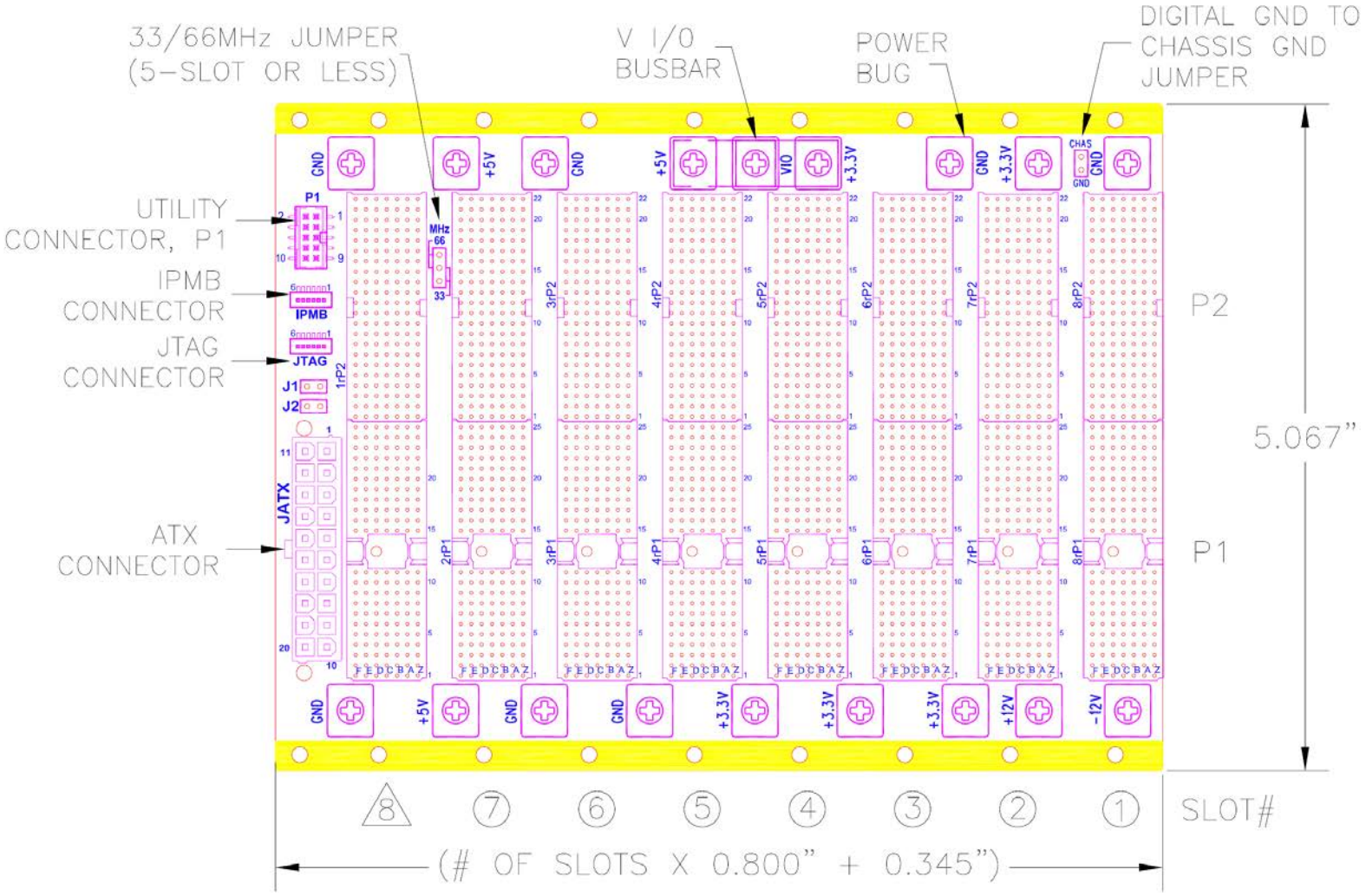
NOTE 1 : Via jumper J1 to DEG#
NOTE 2 : Via jumper J2 to GND

**Mechanical and Electrical Interface**
**3U cPCI Backplane, Rear view, system slot left**



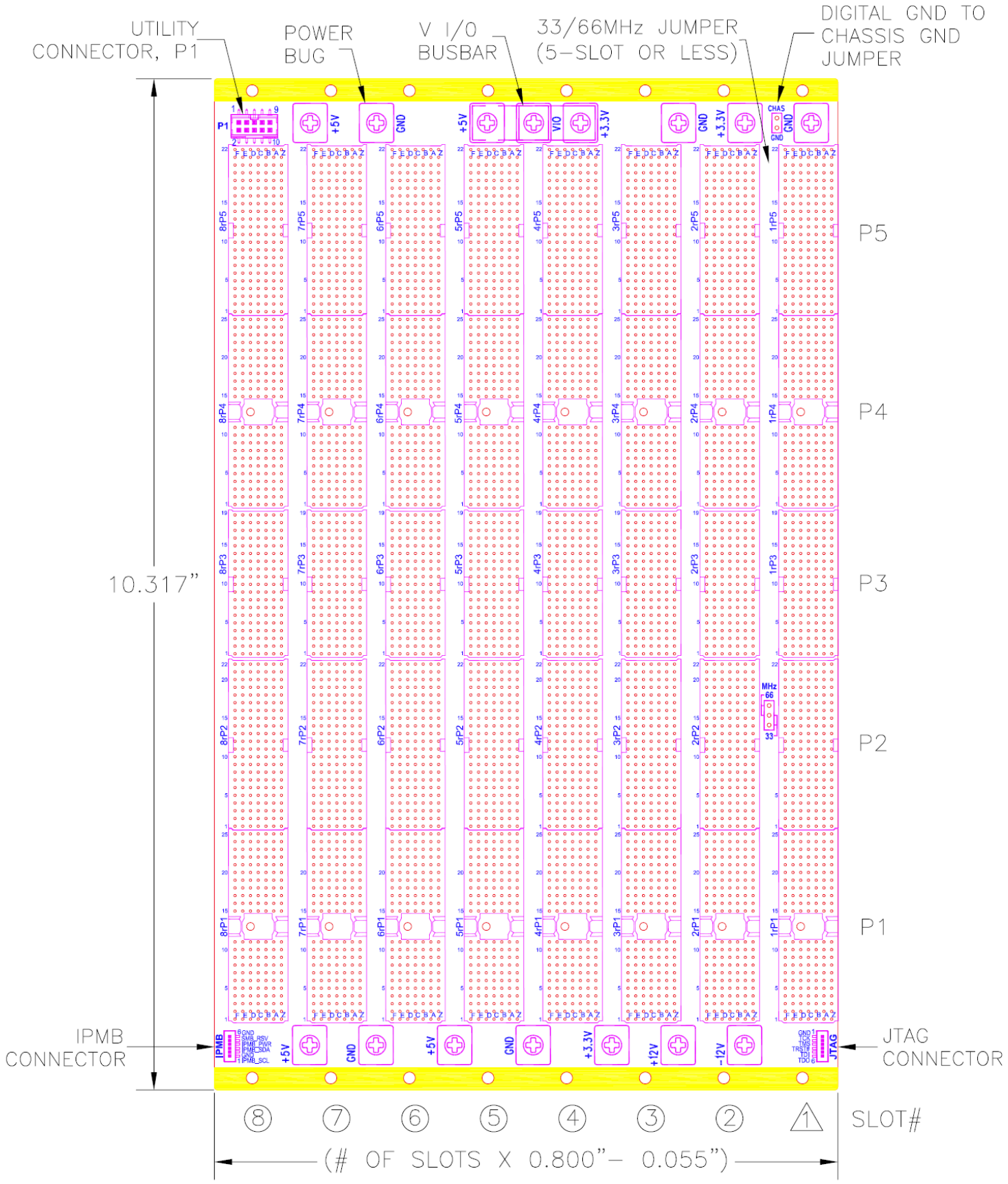
**Mechanical and Electrical Interface**

**3U cPCI Backplane, Rear view, system slot right**



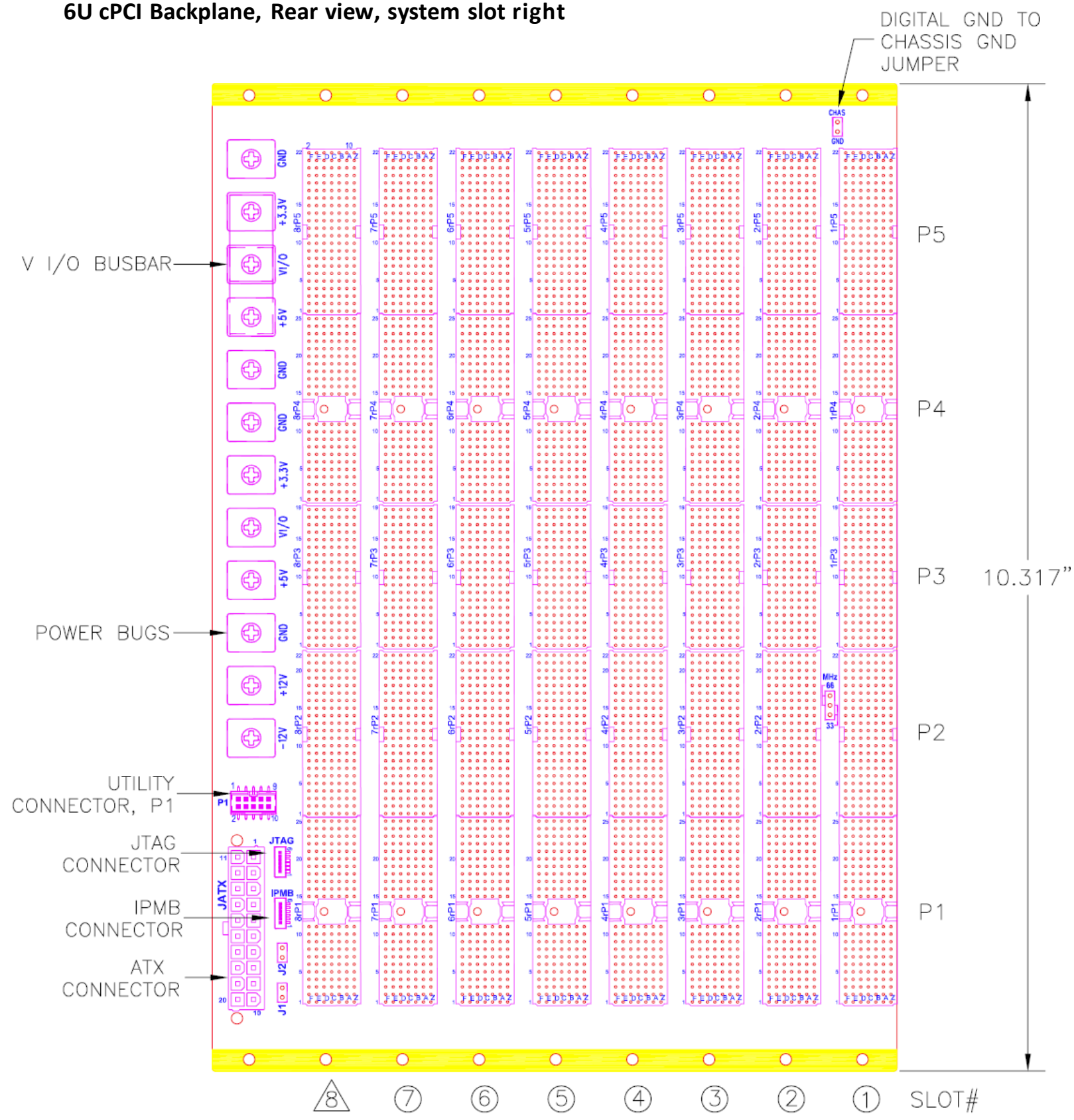
## Mechanical and Electrical Interface

## 6U cPCI Backplane, Rear view, system slot left



## Mechanical and Electrical Interface

### 6U cPCI Backplane, Rear view, system slot right



## Mechanical and Climatic Parameters

| | Backplanes |
|---|---|
| **Operating Temperature** | -40°C - +85°C<br>(-55°C - +125°C on request) |
| **Storage Temperature** | -55°C - +105°C<br>(-55°C - +155°C on request) |
| **Humidity** | max 95%, not condensing<br>(Conformal Coating on request) |
| **Flammability**<br>PCB, Connectors | UL 94 V-0 |
| **Connectors**<br>Performance level per IEC 61076-4-101<br>Mechanical Durability (Mating Cycles)<br>Total Insertion and Extraction Force (mating) | IEC 61076-4-101 (HardMetric 2mm Grid)<br>level 2 (level 1 on request)<br>>250 cycles (> 500 cycles on request)<br>< 0,75 N / Pin |
| **Vibration** acc. DIN 41640 Part 15 | 10Hz – 500Hz (5Hz – 2000Hz on request)<br>5g rms (20g rms on request) |
| **Shock** (10 pulses each direction x,y,z) | |
| **Low Pressure / Altitude**<br>(max Board voltage per single isolation gap doesn't exceed 12V) | |
| **Construction** | 10 layer, FR-4 |

## Electrical Parameters

| | |
|---|---|
| **Specifications** | PICMG 2.0 R3.0 CPCI Core Specification<br>PICMG 2.1 CPCI Hot Swap Specification<br>PICMG 2.9 System Management Bus Spec.<br>PICMG 2.10 Keying Specification |
| **Characteristic Impedance**<br>PCI traces<br>Clock traces<br>Clock trace length | <br>65 Ω ± 10 %<br>65 Ω ± 10 %<br>160 +/- 1,0mm; acc. to 66MHz spec for all backplanes |
| **Ohmic Resistance of Signal Tracks**<br>PCI traces | <br>< 95mΩ/Slot |
| **Hot Swap** | supported |
| **Power input** | Power bugs or fastons blades |
| **max. Current carrying Capacity**<br>5V/GND<br>3,3V/GND | <br>8 A per Slot<br>10 A per Slot |
| **max. Voltage Drop** between any two points on the backplane on +5V or +3,3V | < 40mV |
| **VI/O** bridging (default) | +5V blue key; 3,3V yellow key, field changeable |
| **Clock frequency** | 33 MHz, 66 MHz up to 5 Slots |
| **PCI Bus Width** | 32bit; 64bit, check part# |
| **Data Transfer Rate (peak)**<br>33 MHz<br>66 MHz | <br>132 Mbyte/s (32 bit) / 264 Mbyte/s (64 bit)<br>264 Mbyte/s (32 bit) / 528 Mbyte/s (64 bit) |