REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	Change minimum limit of dimension Q for case outline T. Changes in accordance with NOR 5962-R145-97.	96-11-27	Raymond Monnin
B	Add note 4/ to t_{WLQZ}, t_{CDR}, and t_R in table I. Add note 5/ to t_{ELQX}, t_{WHQX}, t_{OLQX}, and t_{OHQZ} in table I. Add case outline 8. Change dimensions b, c, L, and Q for case outline T. Add CAGE 01295 as source of supply for case outlines T and 8. Update boilerplate. Editorial changes throughout.	97-04-17	Raymond Monnin
C	Change minimum dimensions A, b, and E for case outline U. Add CAGE 65786 as a source of supply . Editorial changes throughout. - ksr	97-10-24	Raymond Monnin
D	Change case outline 9 dimension A from .114 inches to .130 inches. - glg	00-03-01	Raymond Monnin
E	Added low-power devices 09 - 14 to drawing. Removed CAGE 0EU86 for devices 05 - 08. - glg	00-11-22	Raymond Monnin
F	Changed minimum dimension b for package "U" from 0.015 inches to 0.012 inches. - glg	00-12-13	Raymond Monnin
G	Changed minimum dimension b for package "M" from 0.019 inches to 0.012 inches. Updated boilerplate paragraphs. ksr	02-02-12	Raymond Monnin
H	Table I; Changed the I_{OL} from 8 mA to 6 mA V_{OL} test. Added device types 15 and 16. Editorial changes throughout. -sld	04-05-25	Raymond Monnin
J	Add case outline 7. Add CAGE 0EU86 as source of supply for case outline 7. Editorial changes throughout. tcr	08-08-18	Robert M. Heber
K	Add device 17 and add case outline 6. Add CAGE 6S055 as source of supply for case outline 6. Some editorial changes. ksr	09-01-22	Robert M. Heber

REV																				
SHEET																				
REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS OF SHEETS	REV	K	K	K	K	K	K	K	K	K	K	K	K	K	K
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Jeff Bowling

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael. A. Frye

DRAWING APPROVAL DATE
96-03-05

REVISION LEVEL
K

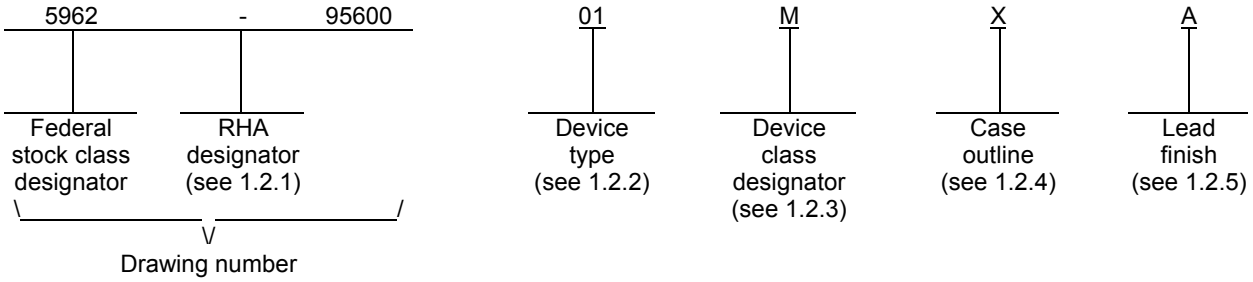
MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 512K X 8 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95600**

SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01		512K X 8 CMOS SRAM	No	45 ns
02		512K X 8 CMOS SRAM	No	35 ns
03		512K X 8 CMOS SRAM	No	25 ns
04		512K X 8 CMOS SRAM	No	20 ns
05		512K X 8 CMOS SRAM	Yes	45 ns
06		512K X 8 CMOS SRAM	Yes	35 ns
07		512K X 8 CMOS SRAM	Yes	25 ns
08		512K X 8 CMOS SRAM	Yes	20 ns
09		512K X 8 CMOS Low Power SRAM	Yes	45 ns
10		512K X 8 CMOS Low Power SRAM	Yes	35 ns
11		512K X 8 CMOS Low Power SRAM	Yes	25 ns
12		512K X 8 CMOS Low Power SRAM	Yes	20 ns
13		512K X 8 CMOS Low Power SRAM	Yes	15 ns
14		512K X 8 CMOS SRAM	No	15 ns
15		512K X 8 CMOS SRAM	Yes	12 ns
16		512K X 8 CMOS SRAM	No	12 ns
17		512K X 8 CMOS SRAM	Yes	12 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535, as applicable (see 6.6.1 and 6.6.2 herein).

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T32 or CDIP2-T32	32	Dual-in-line
Y	See figure 1	32	TSOP package
Z	See figure 1	32	Leadless chip carrier
U	See figure 1	32	SOJ package
T	See figure 1	36	Flat pack
M	See figure 1	36	SOJ package
N	See figure 1	36	Leadless chip carrier
9	See figure 1	32	Flat pack
8	See figure 1	36	SOJ package
7	See figure 1	36	SOJ package
6	See figure 1	44	TSOP package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Voltage on any input relative to V_{SS}	-0.5 V dc to +7.0 V dc
For device 17 only	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	6°C/W
Cases U, M, 8 and 7	11°C/W
Case T	10°C/W
Cases Z and N	20°C/W
Case 9	22°C/W
Case 6	7° C/W
Junction temperature (T_J)	+150°C 2/
For - 17	+140°C 2/
Output current	40 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH}) Devices 01 - 08	2.2 V dc to +6.0 V dc
Input high voltage range (V_{IH}) Devices 09 - 13	2.2 V dc to V_{CC} + 0.3 V dc
Input high voltage range (V_{IH}) Device 17	2.0 V dc to V_{CC} + 0.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 3/
Case operating temperature range (T_C)	-55°C to +125°C

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
3/ V_{IL} minimum = -3.0 V dc for pulse width less than 20 ns.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org/.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org/.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current 1/	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), V_{CC} = 5.5 V, $\overline{CE}$ = $\overline{WE}$ = V_{IL}, outputs open	1, 2, 3	01-08, 14		225	mA
				09-13		180	
				15, 16		90	
				17		110	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = 5.5 V	1, 2, 3	01-08, 14		60	mA
				09-13, 15 - 17		30	
Standby power supply current (CMOS)	I_{CC3}	$\overline{CE} \ge V_{CC}$ - 0.2 V, V_{CC} = 5.5 V, $V_{IN} < 0.2$ V or $> (V_{CC}$ -0.2 V)	1, 2, 3	01-04, 14		25	mA
				05-08		10	
				09-13, 15 - 17		20	
Data retention voltage	V_{DR}	$\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $\le$ 0.2 V	1, 2, 3	05-13, 15, 17	2		V
Data retention current	I_{CC4}	V_{CC} = 2.0 V	1, 2, 3	05-08		2	mA
				09-13		4.5	
				15		7	
				17		12	
Input leakage current, any input	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V	1, 2, 3	All		$\pm$10	µA
Off-state output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{IN} = 0 V to 5.5 V	1, 2, 3	All		$\pm$10	µA
Output high voltage	V_{OH}	I_{OUT} = -4.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	I_{OUT} = 6.0 mA, V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Input capacitance	C_{IN}	V_{IN} = 0 V, see 4.4.1e f = 1.0 MHz, T_A = +25°C,	4	All		12	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, see 4.4.1e f = 1.0 MHz, T_A = +25°C,	4	All		14	pF
Functional testing		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable access time	t_{ELQV}	See figure 5 2/ 3/	9,10,11	01,05,09		45	ns
				02,06,10		35	
				03,07,11		25	
				04,08,12		20	
				13,14		15	
				15 - 17		12	
Read cycle time	t_{AVAV}		9,10,11	01,05,09	45		ns
				02,06,10	35		
				03,07,11	25		
				04,08,12	20		
				13,14	15		
				15 - 17	12		
Address access time	t_{AVQV}		9,10,11	01,05,09		45	ns
				02,06,10		35	
				03,07,11		25	
				04,08,12		20	
				13,14		15	
				15 - 17		12	
Output hold after address change	t_{AVQX}		9,10,11	01-08	3		ns
				09-14, 15 - 17	2		
Chip enable to output active 4/ 5/	t_{ELQX}		9,10,11	01-08	3		ns
				09-14, 15 - 17	2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip disable to output inactive 4/ 5/	t_{EHQZ}	See figure 5 2/ 3/	9,10,11	01,05,09	0	20	ns
				02,06,10	0	15	
				03,07,11	0	10	
				04,08,12	0	8	
				13,14	0	7	
				15 - 17	0	6.5	
Output enable to output valid	t_{OLQV}	See figure 5 2/	9,10,11	01,05,09		25	ns
				02,06,10		15	
				03,07,11		12	
				04,08,12		10	
				13,14		8	
				15 - 17		7	
Output enable to output in low Z 4/ 5/	t_{OLQX}		9,10,11	All	0		ns
Output enable to output in high Z 4/ 5/	t_{OHQZ}		9,10,11	01,05,09	0	20	ns
				02,06,10	0	15	
				03,07,11	0	10	
				04,08,12	0	8	
				13,14	0	7	
				15 - 17	0	6.5	
Write cycle time	t_{AVAV}		9,10,11	01,05,09	45		ns
				02,06,10	35		
				03,07,11	25		
				04,08,12	20		
				13,14	15		
				15 - 17	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write pulse width	t_{WLWH} t_{WLEH}	See figure 5 2/	9,10,11	01,05,09	35		ns
				02,06,10	30		
				03,07,11	20		
				04,08,12	17		
				13,14	15		
				15 - 17	12		
Chip enable to end of write	t_{ELWH} t_{ELEH}		9,10,11	01,05,09	35		ns
				02,06,10	30		
				03,07,11	20		
				04,08,12	17		
				13,14	15		
				15 - 17	12		
Data setup to end of write	t_{DVWH} t_{DVEH}		9,10,11	01,05,09	25		ns
				02,06,10	20		
				03,07,11	12		
				04,08,12	10		
				13,14	7		
				15 - 17	6.5		
Data hold after end of write 4/	t_{WHDX} t_{EHDX}		9,10,11	All	0		ns
Address valid to end of write	t_{AVWH} t_{AVEH}		9,10,11	01,05,09	35		ns
				02,06,10	30		
				03,07,11	20		
				04,08,12	17		
				13,14	15		
				15 - 17	12		

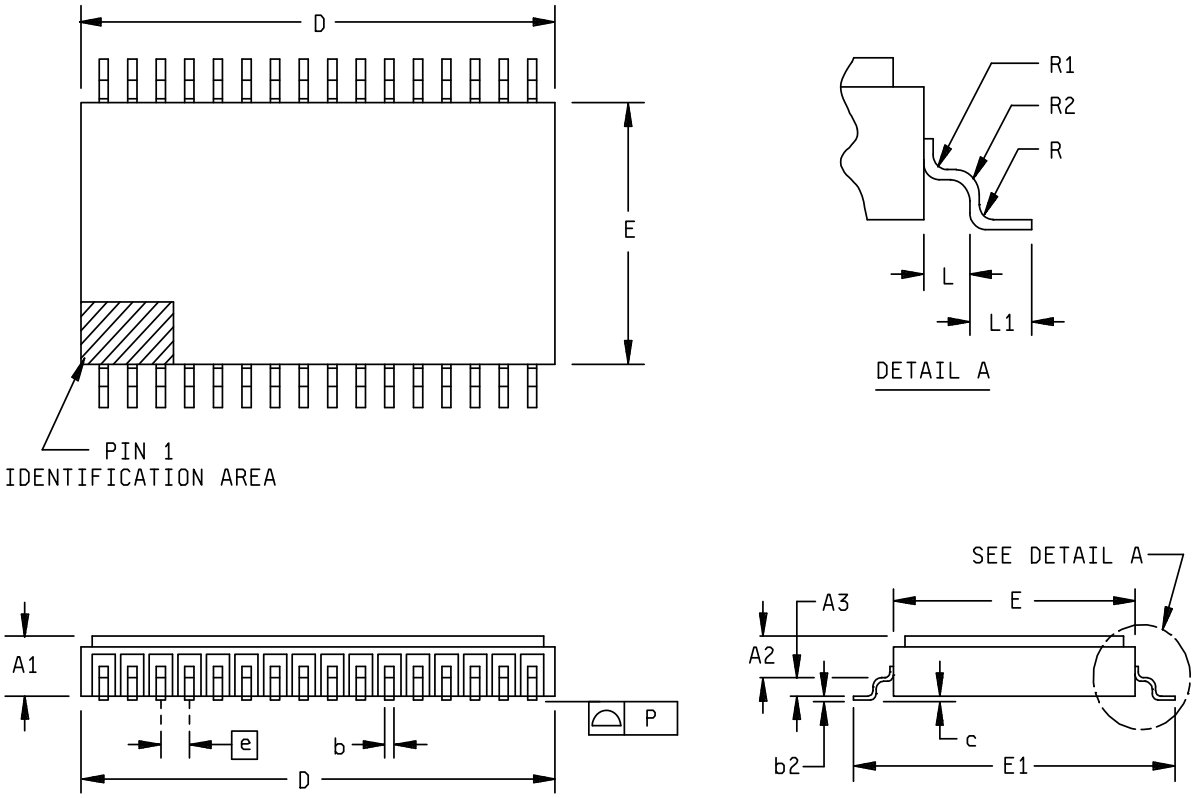
See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address setup to beginning of write	t_{AVWL} t_{AVEL}	See figure 5 2/	9,10,11	All	0		ns
Address hold after end of write	t_{WHAX} t_{EHAX}		9,10,11	01-12	1		ns
				13,14, 15 - 17	0		
Write enable to output disable 4/ 5/	t_{WLQZ}		9,10,11	01,05,09	0	30	ns
				02,06,10	0	25	
				03,07,11	0	10	
				04,08,12	0	8	
				13,14	0	7	
				15 - 17	0	6.5	
Output active after end of write 4/ 5/	t_{WHQX}		9,10,11	All	0		ns
Chip select to data retention time 4/	t_{CDR}	See figure 5 2/ $\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $V_{IN} \le 0.2$ V	9,10,11	05-13, 15 - 17	0		ns
Operation recovery time 4/	t_R		9,10,11	05-08, 17	t_{AVAV}		ns
				09-13	10		ms

1/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.
2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, output loading of 30 pF load capacitance, unless otherwise specified. Output timing reference is 1.5 V. See figure 4.
3/ For read cycles, $\overline{WE}$ is high for entire cycle.
4/ Parameter, if not tested, shall be guaranteed to the limits specified in table I.
5/ Measured ±500 mV from steady-state output voltage(±200 mV for device types 09-13). Load capacitance is 5.0 pF.

Case Y



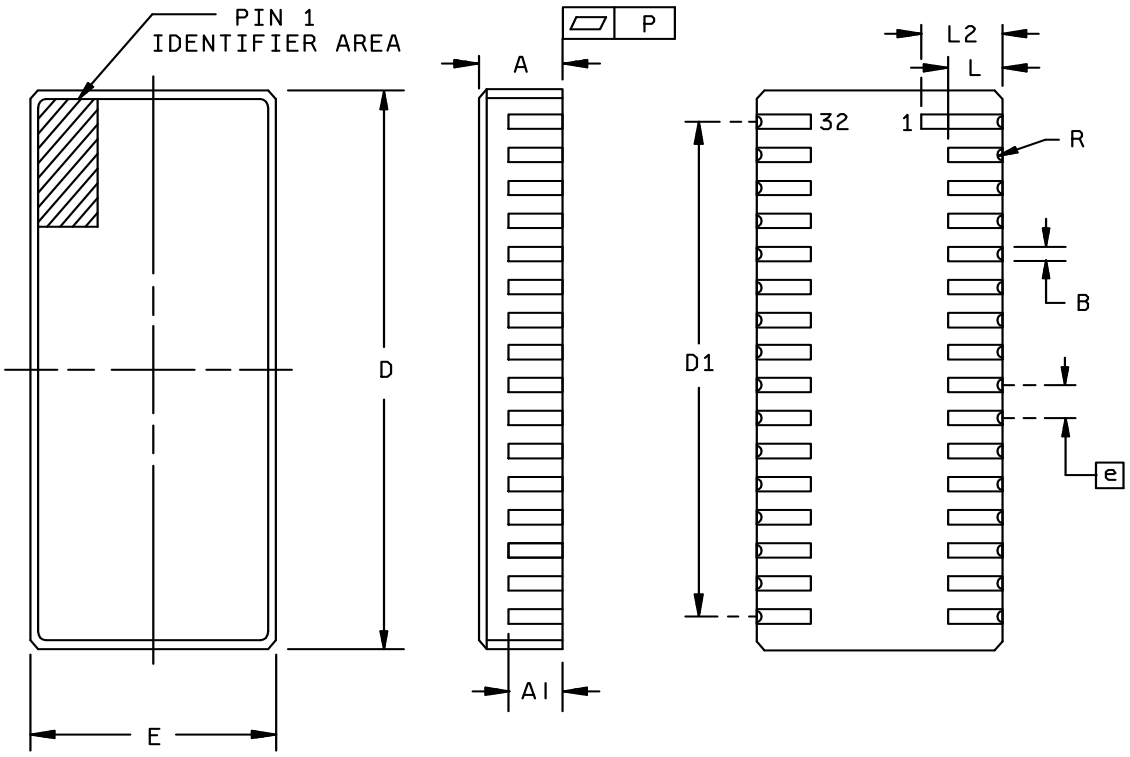
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A1	2.21	3.00	.087	.118
A2	1.27	1.78	.050	.070
A3	0.43	1.52	.017	.060
b	0.20	0.61	.008	.024
b2	0.13	0.20	.005	.008
c	---	0.25	---	.010
D	41.40	42.42	.820	.840
E	10.64	10.85	.419	.427
E1	14.20	14.40	.559	.567

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
e	1.27 BSC		.050 BSC	
L	0.51	1.40	.020	.055
L1	0.51	0.76	.020	.030
P	---	0.10	---	.004
R	0.10	---	.004	---
R1	0.10	0.36	.004	.014
R2	0.25	0.51	.010	.020
N	32			

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines.

Case Z

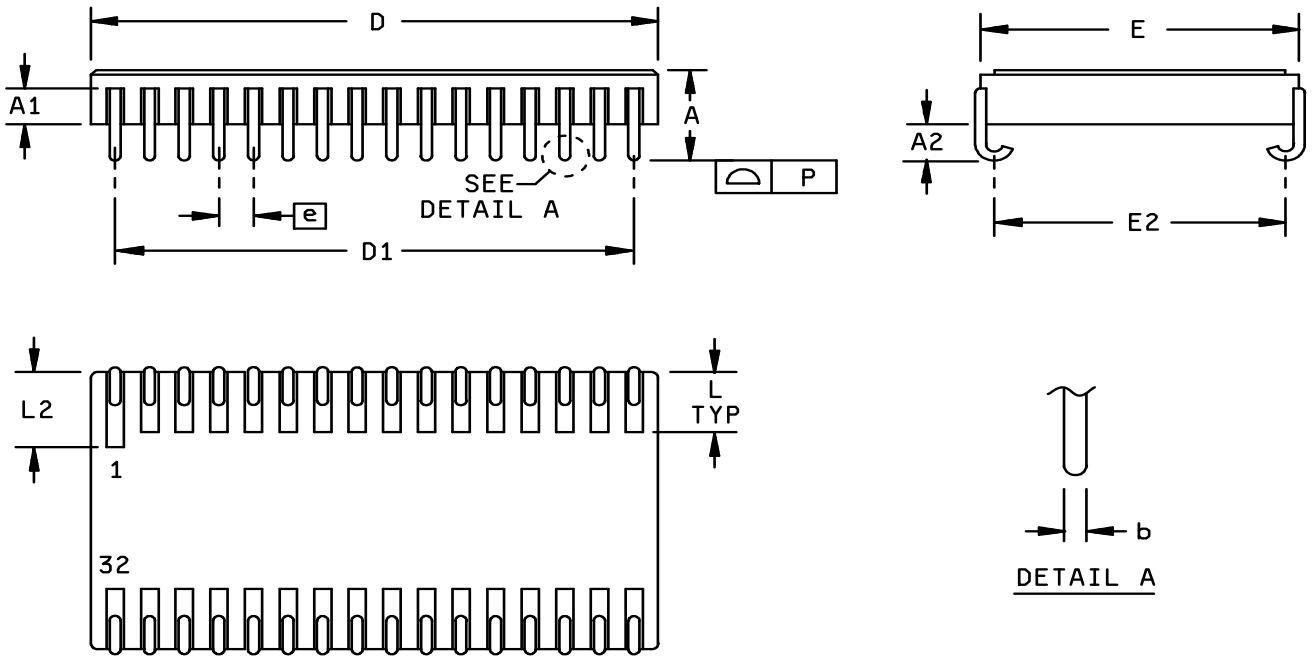


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	.080	.100
A1	1.37	1.68	.054	.066
B	0.56	0.71	.022	.028
D	20.70	21.21	.815	.835
D1	18.80	19.30	.740	.760
E	11.18	11.68	.440	.460
e	1.27 BSC		.050 BSC	
L	2.54 REF		.100 REF	
N	32			
P	---	0.15	---	.006
R	0.23 REF		.009 REF	

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

Case U

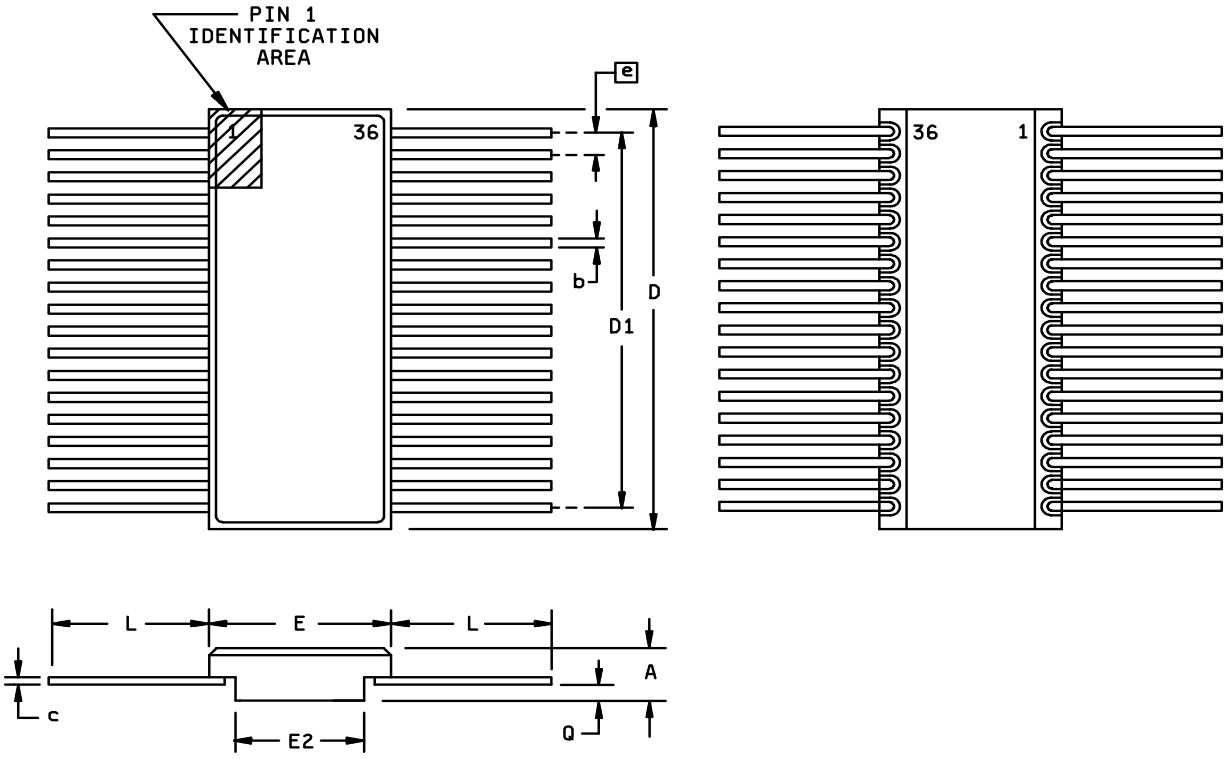


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	4.06	.115	.160
A1	1.37	1.91	.054	.075
A2	0.64	1.60	.025	.063
b	0.30	0.71	.012	.028
D	20.70	21.21	.815	.835
D1	18.80	19.30	.740	.760
E	10.62	11.68	.418	.460
E2	9.42	10.41	.371	.410
e	1.27 BSC		.050 BSC	
L	1.27	1.78	.050	.070
L2	2.92	3.43	.115	.135
N	32			
P	---	0.10	---	.004

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Case outline T

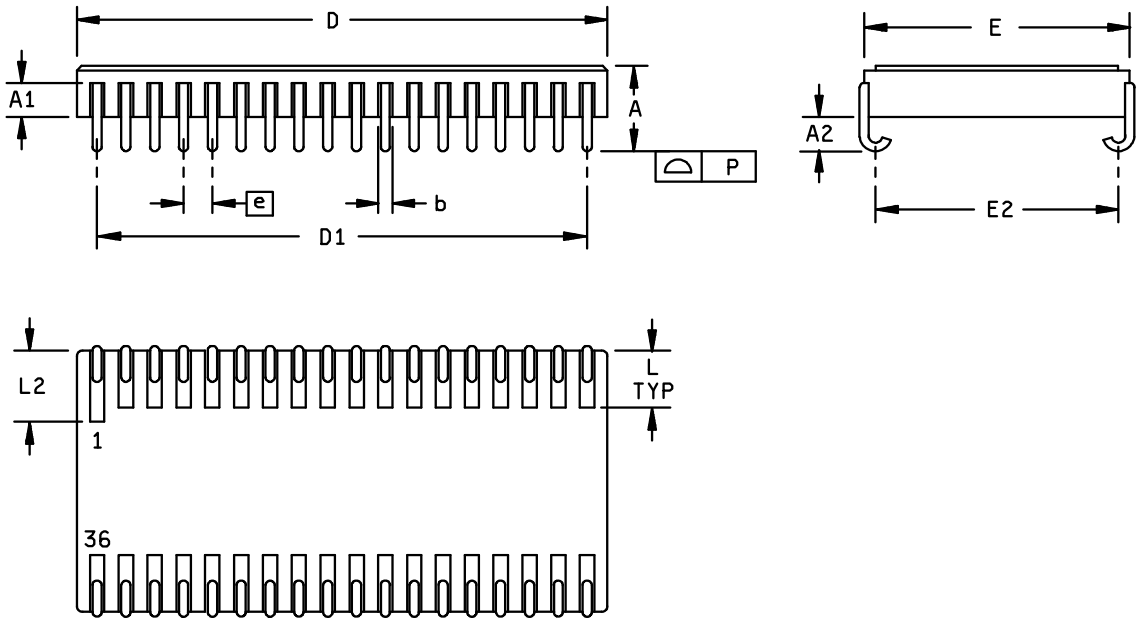


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.44	3.18	.096	.125
b	0.38	0.56	.015	.022
c	0.08	0.23	.003	.009
D	23.11	23.62	.910	.930
D1	21.34	21.84	.840	.860
E	12.83	13.08	.505	.515
E2	9.78	10.08	.385	.397
e	1.27 BSC		.050 BSC	
L	6.35	9.40	.250	.370
N	36			
Q	0.51	1.14	.020	.045

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

Case outline M

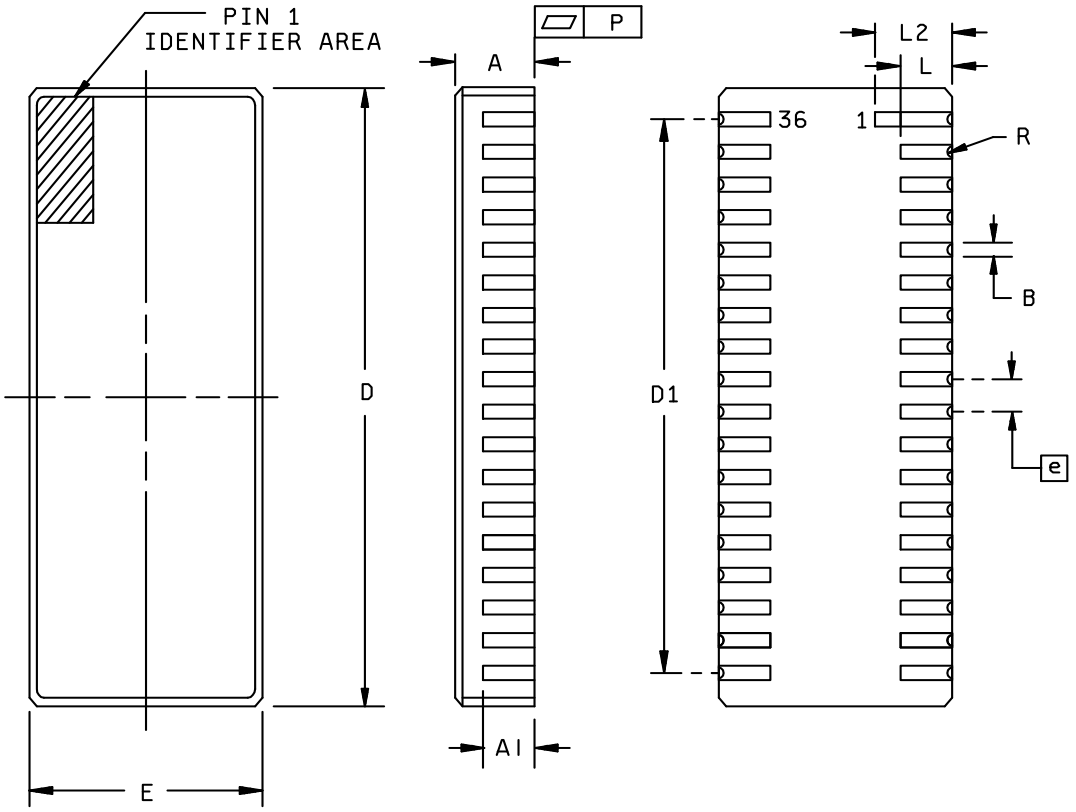


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	4.06	.140	.160
A1	1.37	1.91	.054	.075
A2	0.64	1.60	.025	.063
b	0.30	0.71	.012	.028
D	23.11	23.85	.910	.939
D1	21.34	21.84	.840	.860
E	11.02	11.68	.434	.460
E2	9.50	10.41	.374	.410
e	1.27 BSC		.050 BSC	
L	1.27	1.78	.050	.070
L2	2.92	3.43	.115	.135
N	36			
P	---	0.10	---	.004

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Case N

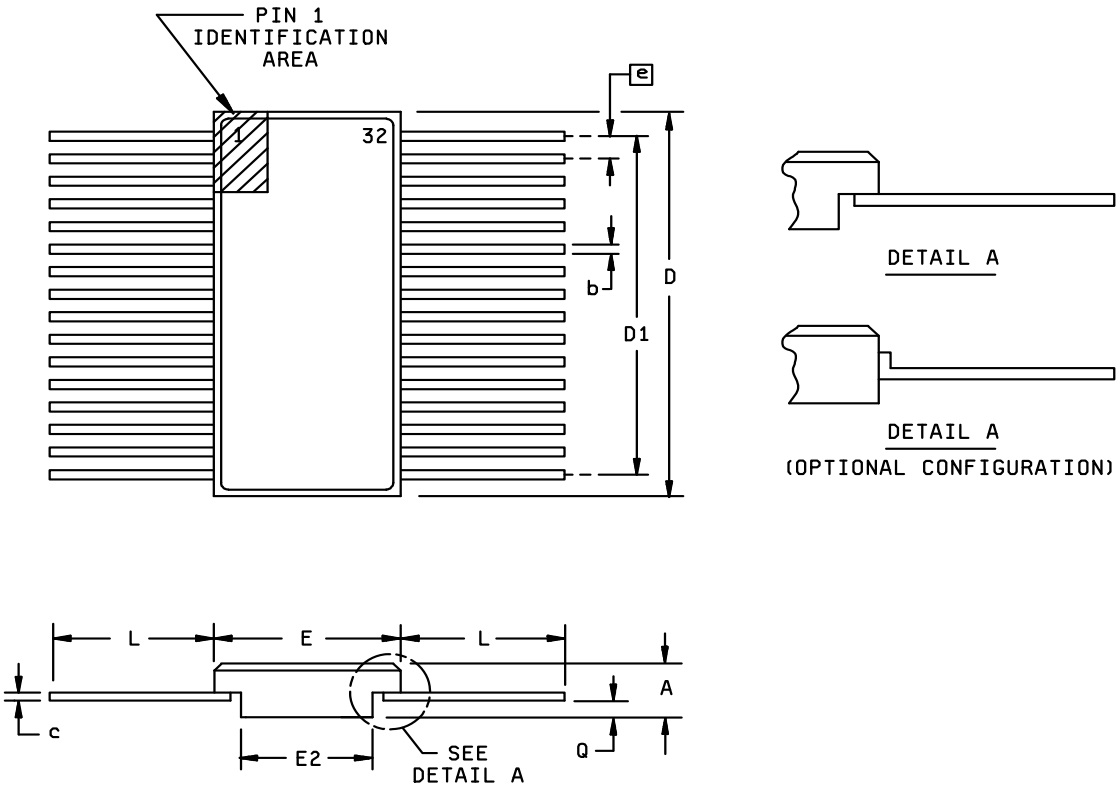


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	.080	.100
A1	1.37	1.68	.054	.066
b	0.56	0.71	.022	.028
D	23.11	23.62	.910	.930
D1	21.34	21.84	.840	.860
E	11.30	11.68	.445	.460
e	1.27 BSC		.050 BSC	
L	2.54 TYP		.100 TYP	
L2	2.92	3.43	.115	.135
N	36			
P	---	0.15	---	.006
R	0.23 TYP		.009 TYP	

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - Continued.

Case 9

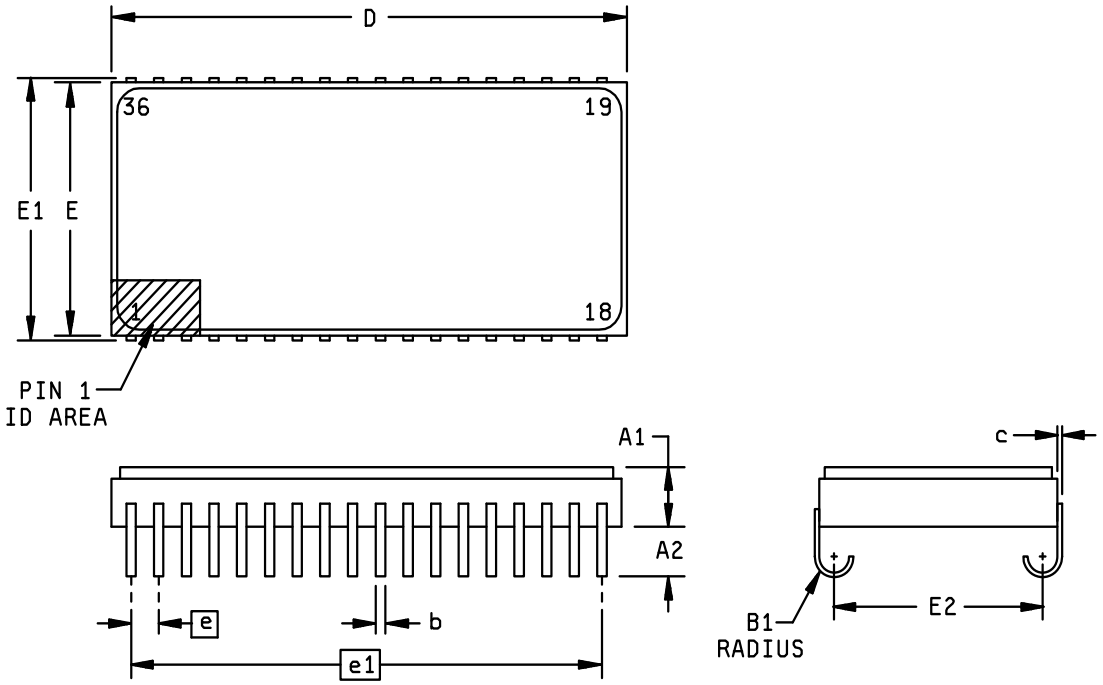


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.44	3.30	.096	.130
b	0.20	0.48	.008	.019
c	0.08	0.20	.003	.008
D	20.73	21.29	.816	.838
D1	18.85	19.25	.742	.758
E	10.64	11.68	.419	.460
E2	8.76	10.85	.345	.427
e	1.27 BSC		.050 BSC	
L	7.37	7.87	.290	.310
N	32			
Q	0.61	0.97	.024	.038

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Dimension E2 does not apply to optional configuration.

FIGURE 1. Case outlines - continued.

Case 8

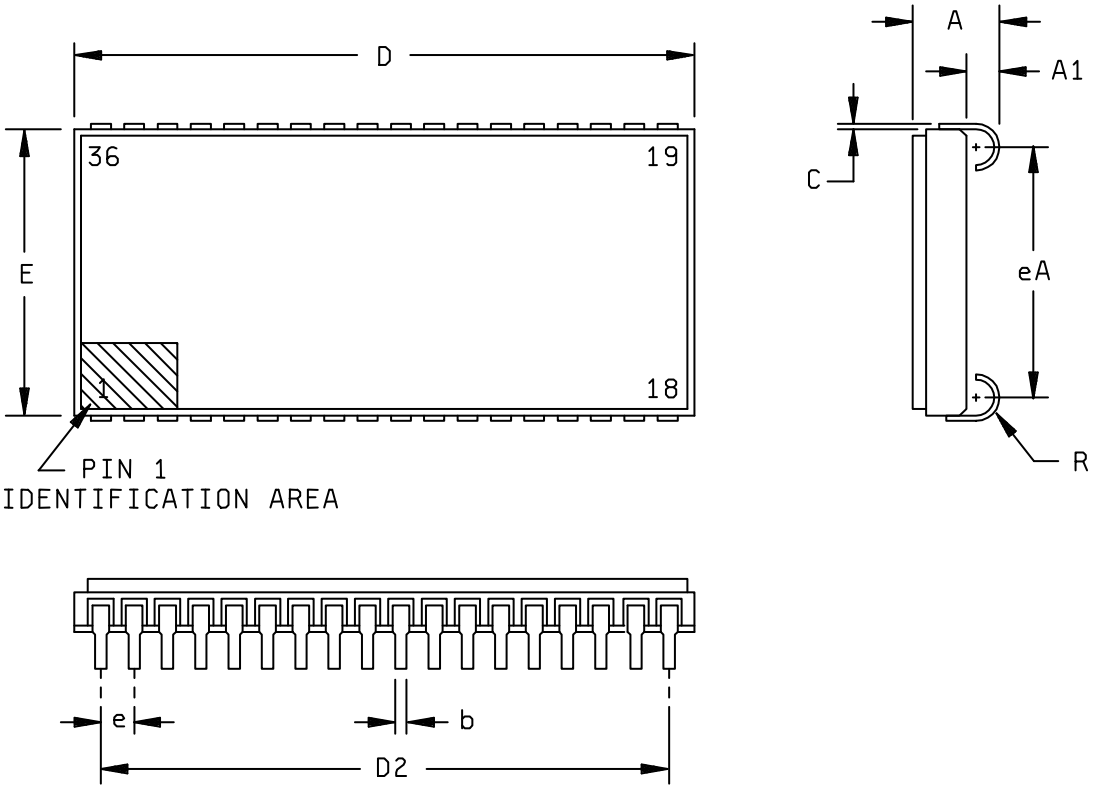


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A1	2.03	2.79	.080	.110
A2	1.47	1.98	.058	.078
B1	0.64R	0.89R	.025R	.035R
b	0.41	0.58	.016	.023
c	0.15	0.33	.006	.013
D	22.99	23.75	.905	.935
E	10.54	11.05	.415	.435
E1	11.30 REF		.445 REF	
E2	9.17	9.93	.361	.391
e	1.27 BSC		.050 BSC	
e1	21.59 BSC		.850 BSC	
N	36			

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

Case 7

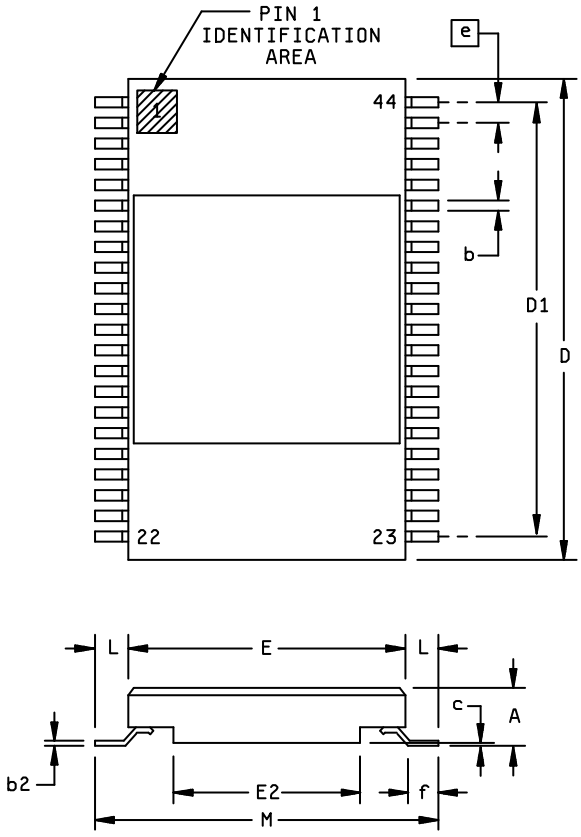


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	3.68	.115	.145
A1	.63	1.14	.025	.045
b	0.38	0.51	.015	.020
C	0.15	0.30	.006	.012
D	23.39	23.85	.921	.939
D2	21.46	21.71	.845	.855
E	10.54	10.92	.415	.430
e	1.27 BSC		.050 BSC	
eA	9.42	9.83	.371	.387
R	.76 TYP		.030 TYP	

NOTE: The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outlines - continued.

Case 6 (see notes)



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.986	3.842	E2	5.280	5.680
b	0.300	0.400	e	0.80 BSC	
b2	0.150	0.250	f	0.406	0.597
c	0.050	---	L	0.839 NOM (ref)	
D	18.215	18.615	M	11.735	11.938
D1	16.60	17.00	N	44	
E	9.96	10.36			

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outlines. – continued.

Device types	All				
Case outlines	X, Y, Z, U, 9	T, M, N, 8, 7	Case outlines	X, Y, Z, U, 9	T, M, N, 8, 7
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	A_{18}	A_0	19	I/O_5	NC
2	A_{16}	A_1	20	I/O_6	A_{10}
3	A_{14}	A_2	21	I/O_7	A_{11}
4	A_{12}	A_3	22	$\overline{CE}$	A_{12}
5	A_7	A_4	23	A_{10}	A_{13}
6	A_6	$\overline{CE}$	24	$\overline{OE}$	A_{14}
7	A_5	I/O_1	25	A_{11}	I/O_5
8	A_4	I/O_2	26	A_9	I/O_6
9	A_3	V_{CC}	27	A_8	V_{CC}
10	A_2	V_{SS}	28	A_{13}	V_{SS}
11	A_1	I/O_3	29	$\overline{WE}$	I/O_7
12	A_0	I/O_4	30	A_{17}	I/O_8
13	I/O_0	$\overline{WE}$	31	A_{15}	$\overline{OE}$
14	$I/0_1$	A_5	32	V_{CC}	A_{15}
15	$I/0_2$	A_6	33	---	A_{16}
16	V_{SS}	A_7	34	---	A_{17}
17	I/O_3	A_8	35	---	A_{18}
18	I/O_4	A_9	36	---	NC

NC = No connection

Device Type	All						
Case Outline	6						
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	A_0	12	V_{SS}	23	A_{10}	34	V_{SS}
2	A_1	13	NC	24	A_{11}	35	NC
3	A_2	14	NC	25	A_{12}	36	NC
4	A_3	15	I/O_2	26	A_{13}	37	I/O_6
5	A_4	16	I/O_3	27	A_{14}	38	I/O_7
6	$\overline{CE}$	17	$\overline{WE}$	28	NC	39	$\overline{OE}$
7	I/O_0	18	A_5	29	I/O_4	40	NC
8	I/O_1	19	A_6	30	I/O_5	41	A_{15}
9	NC	20	A_7	31	NC	42	A_{16}
10	NC	21	A_8	32	NC	43	A_{17}
11	V_{CC}	22	A_9	33	V_{CC}	44	A_{18}

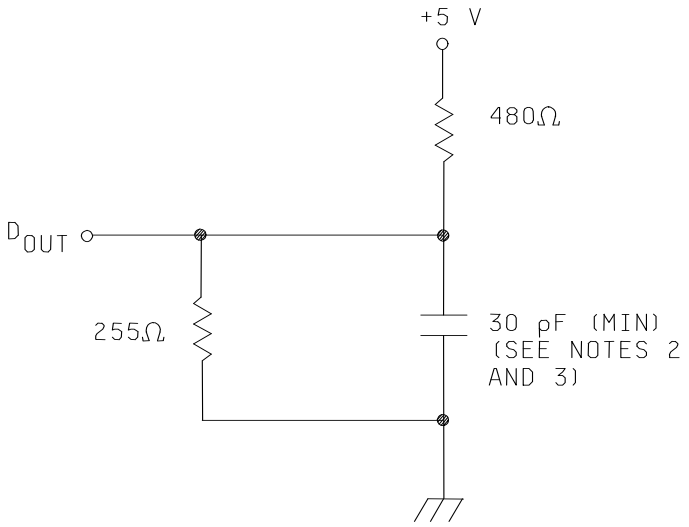
NC = No connection

FIGURE 2. Terminal connections.

$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	Mode	I/O	Power
X	H	X	Standby	High Z	Standby
H	L	H	Output deselect	High Z	Active
L	L	H	Read	D_{OUT}	Active
X	L	L	Write	D_{IN}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 3. Truth table.



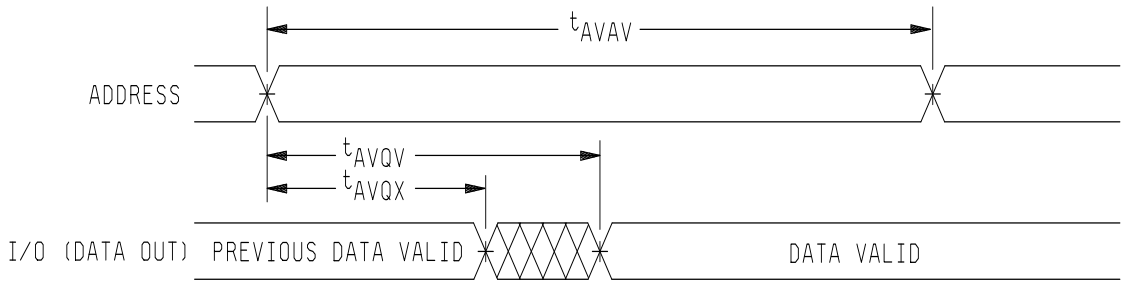
NOTES:
1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{ELQX}, t_{EHQZ}, t_{OLQX}, t_{OHQZ}, t_{WLQZ}, and t_{WHQX}.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise, fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuits.

READ CYCLE NO. 1 ($\overline{WE}$ HIGH, $\overline{CE}$ LOW)



READ CYCLE NO. 2 ($\overline{WE}$ HIGH)

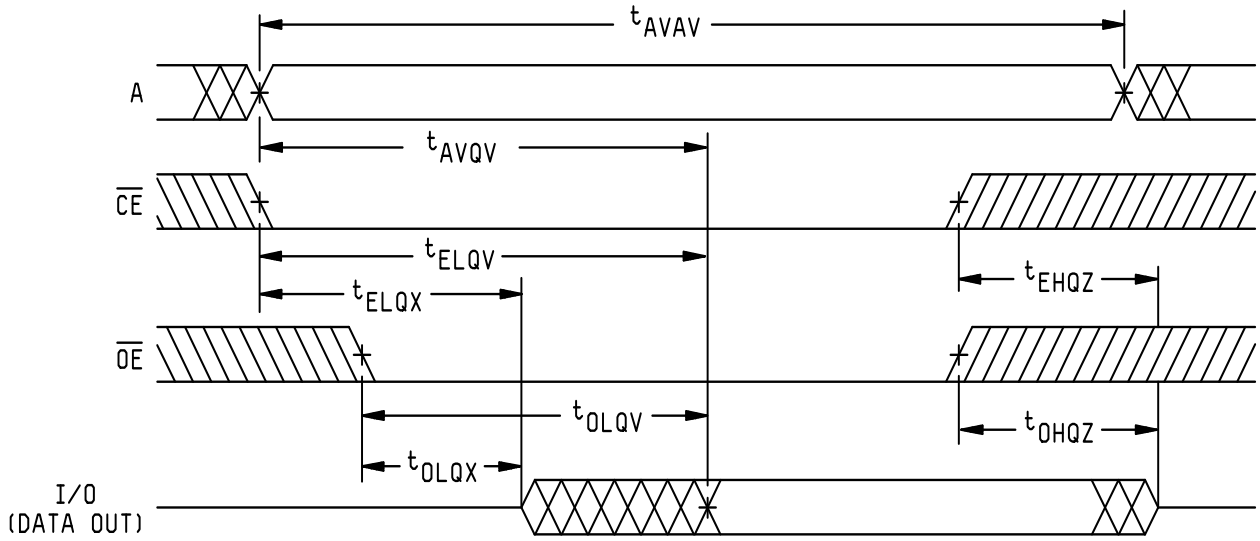
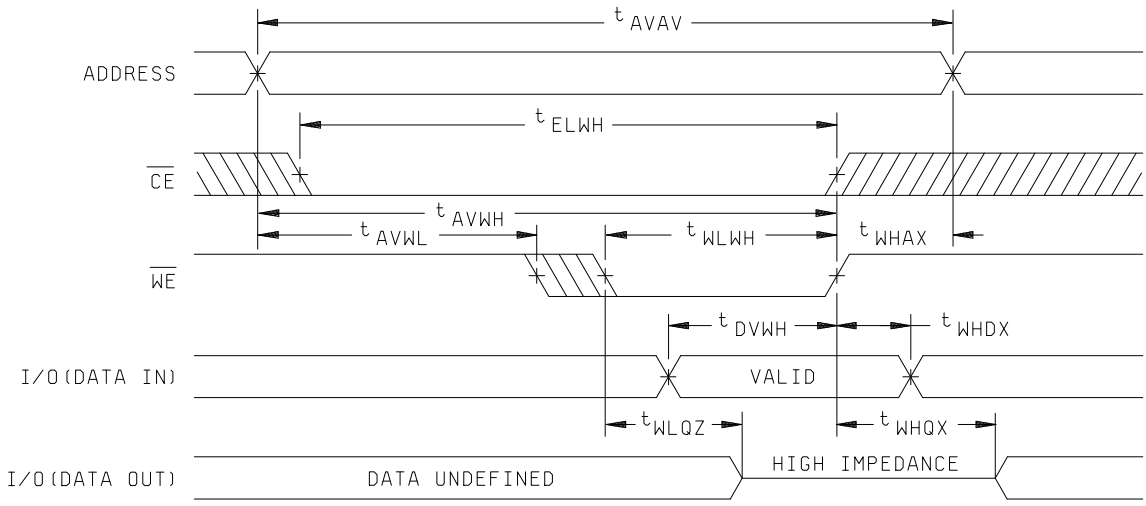


FIGURE 5. Timing waveforms.

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)

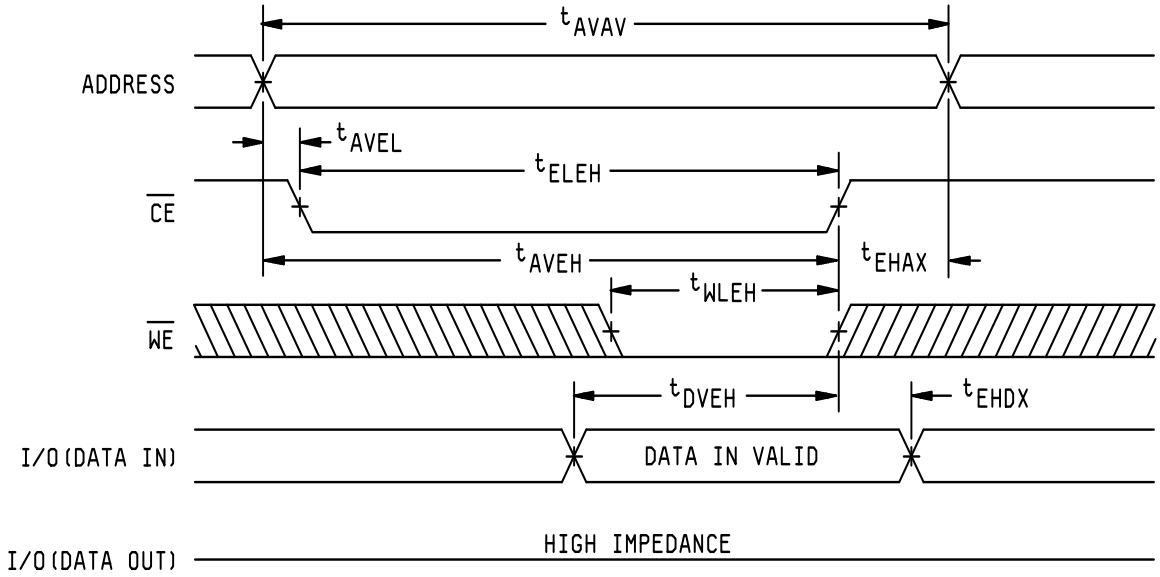


FIGURE 5. Timing waveforms - continued.

Data Retention Waveform

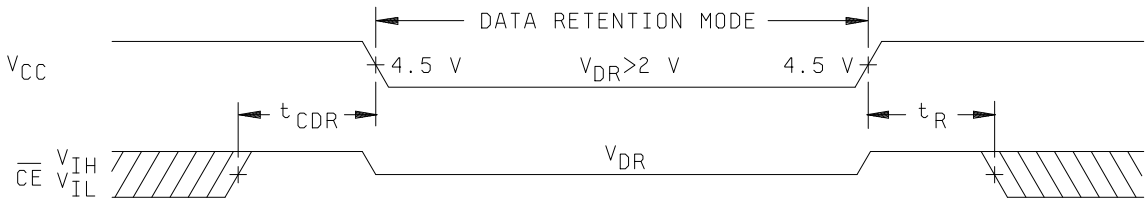


FIGURE 5. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC3} standby	±10%
I_{ILK}, I_{OLK}	±10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.1 Group A inspection Continued.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows.

C_{IN}, C_{OUT} ..... Input and bi-directional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{ILK} ..... Input leakage current.
I_{OLK} ..... Output leakage current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A

Appendix A forms a part of SMD 5962-95600

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 09-01-22

Approved sources of supply for SMD 5962-95600 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535, as applicable, during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560001MXA	54230	EDI88512CA45CB
	0EU86	AS5C4008CW-45
5962-9560001MYA	54230	EDI88512CA45B32B
5962-9560001MZA	0EU86	AS5C4008EC-45
	54230	EDI88512CA45L32B
5962-9560001MUA	54230	EDI88512CA45NB
	0EU86	AS5C4008ECJ-45
	3/	CY7C1048-45FJMB
5962-9560001MTA	54230	EDI88512CA45F36B
	0EU86	AS5C512K8F-45
	3DTT2	P4C1049-45FSMB
5962-9560001MMA	54230	EDI88512CA45N36B
	0EU86	AS5C512K8ECJ-45
5962-9560001MNA	0EU86	AS5C512K8EC-45
	3DTT2	P4C1049-45L36MB
5962-9560001M7A	0EU86	AS5C512K8SOJ-45
5962-9560001M9A	54230	EDI88512CA45F32B
	0EU86	AS5C4008F-45
5962-9560002MXA	54230	EDI88512CA35CB
	0EU86	AS5C4008CW-35
5962-9560002MYA	54230	EDI88512CA35B32B
5962-9560002MZA	0EU86 54230	AS5C4008EC-35 EDI88512CA35L32B
5962-9560002MUA	54230	EDI88512CA35NB
	0EU86	AS5C4008ECJ-35
	3/	CY7C1048-35FJMB
5962-9560002MTA	54230	EDI88512CA35F36B
	0EU86	AS5C512K8F-35
	3DTT2	P4C1049-35FSMB
	3/	SMJ684002-35HKEM
5962-9560002MMA	54230	EDI88512CA35N36B
	0EU86	AS5C512K8ECJ-35

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560002MNA	0EU86	AS5C512K8EC-35
	3DTT2	P4C1049-35L36MB
5962-9560002M9A	54230	EDI88512CA35F32B
	0EU86	AS5C4008F-35
5962-9560002M7A	0EU86	AS5C512K8SOJ-35
5962-9560002M8A	3/	SMJ684002-35HJAM
5962-9560003MXA	54230	EDI88512CA25CB
	0EU86	AS5C4008CW-25
5962-9560003MYA	54230	EDI88512CA25B32B
5962-9560003MZA	0EU86	AS5C4008EC-25
	54230	EDI88512CA25L32B
5962-9560003MUA	54230	EDI88512CA25NB
	0EU86	AS5C4008ECJ-25
	3/	CY7C1048-25FJMB
5962-9560003MTA	54230	EDI88512CA25F36B
	0EU86	AS5C512K8F-25
	3DTT2	P4C1049-25FSMB
	3/	SMJ684002-25HKEM
5962-9560003MMA	54230	EDI88512CA25N36B
	0EU86	AS5C512K8ECJ-25
5962-9560003MNA	0EU86	AS5C512K8EC-25
	3DTT2	P4C1049-25L36MB
5962-9560003M9A	54230	EDI88512CA25F32B
	0EU86	AS5C4008F-25
5962-9560003M7A	0EU86	AS5C512K8SOJ-25
5962-9560003M8A	3/	SMJ684002-25HJAM
5962-9560004MXA	54230	EDI88512CA20CB
	0EU86	AS5C4008CW-20
5962-9560004MYA	54230	EDI88512CA20B32B

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560004MZA	0EU86	AS5C4008EC-20
	54230	EDI88512CA20L32B
5962-9560004MUA	54230	EDI88512CA20NB
	0EU86	AS5C4008ECJ-20
	3/	CY7C1048-20FJMB
5962-9560004MTA	54230	EDI88512CA20F36B
	0EU86	AS5C512K8F-20
	3DTT2	P4C1049-20FSMB
	3/	SMJ684002-20HKEM
5962-9560004MMA	54230	EDI88512CA20N36B
	0EU86	AS5C512K8ECJ-20
5962-9560004MNA	0EU86	AS5C512K8EC-20
	3DTT2	P4C1049-20L36MB
5962-9560004M9A	54230	EDI88512CA20F32B
	0EU86	AS5C4008F-20
5962-9560004M7A	0EU86	AS5C512K8SOJ-20
5962-9560004M8A	3/	SMJ684002-20HJAM
5962-9560005MXA	54230	EDI88512LPA45CB
	0EU86	AS5C4008CW-45L
5962-9560005MYA	54230	EDI88512LPA45B32B
5962-9560005MZA	0EU86	AS5C4008EC-45L
	54230	EDI88512LPA45L32B
5962-9560005MUA	54230	EDI88512LPA45NB
	0EU86	AS5C4008ECJ-45L
	3/	CY7C1048L-45FJMB
5962-9560005MTA	54230	EDI88512LPA45F36B
	0EU86	AS5C512K8F-45L
	3DTT2	P4C1049L-45FSMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560005MMA	54230	EDI88512LPA45N36B
	0EU86	AS5C512K8ECJ-45L
5962-9560005MNA	0EU86	AS5C512K8EC-45L
	3DTT2	P4C1049L-45L36MB
5962-9560005M7A	0EU86	AS5C512K8SOJ-45L
5962-9560005M9A	54230	EDI88512LPA45F32B
	0EU86	AS5C4008F-45L
5962-9560006MXA	54230	EDI88512LPA35CB
	0EU86	AS5C4008CW-35L
5962-9560006MYA	54230	EDI88512LPA35B32B
5962-9560006MZA	0EU86	AS5C4008EC-35L
	54230	EDI88512LPA35L32B
5962-9560006MUA	54230	EDI88512LPA35NB
	0EU86	AS5C4008ECJ-35L
	3/	CY7C1048L-35FJMB
5962-9560006MTA	54230	EDI88512LPA35F36B
	0EU86	AS5C512K8F-35L
	3DTT2	P4C1049L-35FSMB
	3/	SMJ684002-35HKEM
5962-9560006MMA	54230	EDI88512LPA35N36B
	0EU86	AS5C512K8ECJ-35L
5962-9560006MNA	0EU86	AS5C512K8EC-35L
	3DTT2	P4C1049L-35L36MB
5962-9560006M9A	54230	EDI88512LPA35F32B
	0EU86	AS5C4008F-35L
5962-9560006M8A	3/	SMJ684002-35HJAM
5962-9560006M7A	0EU86	AS5C512K8SOJ-35L
5962-9560007MXA	54230	EDI88512LPA25CB
	0EU86	AS5C4008CW-25L

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560007MYA	54230	EDI88512LPA25B32B
5962-9560007MZA	0EU86	AS5C4008EC-25L
	54230	EDI88512LPA25L32B
5962-9560007MUA	54230	EDI88512LPA25NB
	0EU86	AS5C4008ECJ-25L
	3/	CY7C1048L-25FJMB
5962-9560007MTA	54230	EDI88512LPA25F36B
	0EU86	AS5C512K8F-25L
	3DTT2	P4C1049L-25FSMB
	3/	SMJ684002-25HKEM
5962-9560007MMA	54230	EDI88512LPA25N36B
	0EU86	AS5C512K8ECJ-25L
5962-9560007MNA	0EU86	AS5C512K8EC-25L
	3DTT2	P4C1049L-25L36MB
5962-9560007M9A	54230	EDI88512LPA25F32B
	0EU86	AS5C4008F-25L
5962-9560007M8A	3/	SMJ684002-25HJAM
5962-9560007M7A	0EU86	AS5C512K8SOJ-25L
5962-9560008MXA	54230	EDI88512LPA20CB
	0EU86	AS5C4008CW-20L
5962-9560008MYA	54230	EDI88512LPA20B32B
5962-9560008MZA	0EU86	AS5C4008EC-20L
	54230	EDI88512LPA20L32B
5962-9560008MUA	54230	EDI88512LPA20NB
	0EU86	AS5C4008ECJ-20L
	3/	CY7C1048L-20FJMB
5962-9560008MTA	54230	EDI88512LPA20F36B
	0EU86	AS5C512K8F-20L
	3DTT2	P4C1049L-20FSMB
	3/	SMJ684002-20HKEM
5962-9560008MMA	54230	EDI88512LPA20N36B
	0EU86	AS5C512K8ECJ-20L
5962-9560008MNA	0EU86	AS5C512K8EC-20L
	3DTT2	P4C1049L-20L36MB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560008M9A	54230	EDI88512LPA20F32B
	0EU86	AS5C4008F-20L
5962-9560008M8A	3/	SMJ684002-20HJAM
5962-9560008M7A	0EU86	AS5C512K8SOJ-20L
5962-9560009QXA	0EU86 54230	AS5C4008CW-45L EDI88512LPA45CB
5962-9560009QZA	0EU86 54230	AS5C4008EC-45L EDI88512LPA45L32B
5962-9560009QUA	0EU86 54230	AS5C4008ECJ-45L EDI88512LPA45NB
5962-9560009MTA	3DTT2	P4C1049L-45FSMB
5962-9560009QTA	0EU86 54230	AS5C512K8F-45L EDI88512LPA45F36B
5962-9560009QMA	0EU86 54230	AS5C512K8ECJ-45L EDI88512LPA45N36B
5962-9560009QNA	0EU86	AS5C512K8EC-45L
5962-9560009MNA	3DTT2	P4C1049L-45L36MB
5962-9560009Q9A	0EU86 54230	AS5C4008F-45L EDI88512LPA45F32B
5962-9560009Q7A	0EU86	AS5C512K8SOJ-45L
5962-9560010QXA	0EU86 54230	AS5C4008CW-35L EDI88512LPA35CB
5962-9560010QZA	0EU86 54230	AS5C4008EC-35L EDI88512LPA35L32B
5962-9560010QUA	0EU86 54230	AS5C4008ECJ-35L EDI88512LPA35NB
5962-9560010QTA	0EU86 54230	AS5C512K8F-35L EDI88512LPA35F36B
5962-9560010MTA	3DTT2	P4C1049L-35FSMB
5962-9560010QMA	0EU86 54230	AS5C512K8ECJ-35L EDI88512LPA35N36B
5962-9560010QNA	0EU86	AS5C512K8EC-35L
5962-9560010MNA	3DTT2	P4C1049L-35L36MB
5962-9560010Q9A	0EU86 54230	AS5C4008F-35L EDI88512LPA35F32B
5962-9560010Q7A	0EU86	AS5C512K8SOJ-35L
5962-9560011QXA	0EU86 54230	AS5C4008CW-25L EDI88512LPA25CB
5962-9560011QZA	0EU86 54230	AS5C4008EC-25L EDI88512LPA25L32B
5962-9560011QUA	0EU86 54230	AS5C4008ECJ-25L EDI88512LPA25NB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560011QTA	0EU86 54230	AS5C512K8F-25L EDI88512LPA25F36B
5962-9560011MTA	3DTT2	P4C1049L-25FSMB
5962-9560011QMA	0EU86 54230	AS5C512K8ECJ-25L EDI88512LPA25N36B
5962-9560011QNA	0EU86	AS5C512K8EC-25L
5962-9560011MNA	3DTT2	P4C1049L-25L36MB
5962-9560011Q9A	0EU86 54230	AS5C4008F-25L EDI88512LPA25F32B
5962-9560011Q7A	0EU86	AS5C512K8SOJ-25L
5962-9560012QXA	0EU86 54230	AS5C4008CW-20L EDI88512LPA20CB
5962-9560012QZA	0EU86 54230	AS5C4008EC-20L EDI88512LPA20L32B
5962-9560012QUA	0EU86 54230	AS5C4008ECJ-20L EDI88512LPA20NB
5962-9560012QTA	0EU86 54230	AS5C512K8F-20L EDI88512LPA20F36B
5962-9560012MTA	3DTT2	P4C1049L-20FSMB
5962-9560012QMA	0EU86 54230	AS5C512K8ECJ-20L EDI88512LPA20N36B
5962-9560012QNA	0EU86	AS5C512K8EC-20L
5962-9560012MNA	3DTT2	P4C1049L-20L36MB
5962-9560012Q9A	0EU86 54230	AS5C4008F-20L EDI88512LPA20F32B
5962-9560012Q7A	0EU86	AS5C512K8SOJ-20L
5962-9560013QXA	0EU86 54230	AS5C4008CW-15L EDI88512LPA15CB
5962-9560013QZA	0EU86 54230	AS5C4008EC-15L EDI88512LPA15L32B
5962-9560013QUA	0EU86 54230	AS5C4008ECJ-15L EDI88512LPA15NB
5962-9560013QTA	0EU86 54230	AS5C512K8F-15L EDI88512LPA15F36B
5962-9560013MTA	3DTT2	P4C1049L-15FSMB
5962-9560013QMA	0EU86 54230	AS5C512K8ECJ-15L EDI88512LPA15N36B
5962-9560013QNA	0EU86	AS5C512K8EC-15L
5962-9560013MNA	3DTT2	P4C1049L-15L36MB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560013Q9A	0EU86 54230	AS5C4008F-15L EDI88512LPA15F32B
5962-9560013Q7A	0EU86	AS5C512K8SOJ-15L
5962-9560014QXA	0EU86 54230	AS5C4008CW-15 EDI88512CA15CB
5962-9560014QZA	0EU86 54230	AS5C4008EC-15 EDI88512CA15L32B
5962-9560014QUA	0EU86 54230	AS5C4008ECJ-15 EDI88512CA15NB
5962-9560014QTA	0EU86 54230	AS5C512K8F-15 EDI88512CA15F36B
5962-9560014MTA	3DTT2	P4C1049-15FSMB
5962-9560014QMA	0EU86 54230	AS5C512K8ECJ-15 EDI88512CA15N36B
5962-9560014QNA	0EU86	AS5C512K8EC-15
5962-9560014MNA	3DTT2	P4C1049-15L36MB
5962-9560014Q9A	0EU86 54230	AS5C4008F-15 EDI88512CA15F32B
5962-9560014Q7A	0EU86	AS5C512K8SOJ-15
5962-9560015QXA	0EU86 54230	AS5C4008CW-12L EDI88512LPA12CB
5962-9560015QZA	0EU86 54230	AS5C4008EC-12L EDI88512LPA12L32B
5962-9560015QUA	0EU86 54230	AS5C4008ECJ-12L EDI88512LPA12NB
5962-9560015QTA	0EU86 54230	AS5C512K8F-12L EDI88512LPA12F36B
5962-9560015MTA	3DTT2	P4C1049L-12FSMB
5962-9560015QMA	0EU86 54230	AS5C512K8ECJ-12L EDI88512LPA12N36B
5962-9560015QNA	0EU86	AS5C512K8EC-12L
5962-9560015MNA	3DTT2	P4C1049L-12L36MB
5962-9560015Q9A	0EU86 54230	AS5C4008F-12L EDI88512LPA12F32B
5962-9560015Q7A	0EU86	AS5C512K8SOJ-12L
5962-9560016QXA	0EU86 54230	AS5C4008CW-12 EDI88512CA12CB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560016QZA	0EU86 54230	AS5C4008EC-12 EDI88512CA12L32B
5962-9560016QUA	0EU86 54230	AS5C4008ECJ-12 EDI88512CA12NB
5962-9560016QTA	0EU86 54230	AS5C512K8F-12 EDI88512CA12F36B
5962-9560016MTA	3DTT2	P4C1049-12FSMB
5962-9560016QMA	0EU86 54230	AS5C512K8ECJ-12 EDI88512CA12N36B
5962-9560016QNA	0EU86	AS5C512K8EC-12
5962-9560016MNA	3DTT2	P4C1049-12L36MB
5962-9560016Q9A	0EU86 54230	AS5C4008F-12 EDI88512CA12F32B
5962-9560016Q7A	0EU86	AS5C512K8SOJ-12
5962-9560017M6A	6S055	DPA71049D02A
5962-9560017M6C	6S055	DPA71049D02C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
54230	White Electronic Designs Corporation. 3601 East University Drive Phoenix, AZ 85034
0EU86	Austin Semiconductor 8701 Cross Park Drive Austin, TX 78754-4566
3DDT2	Pyramid Semiconductor Corporation 1340 Bordeaux Drive Sunnyvale, CA 94089
6S055	DPA Components International 2251 Ward Ave. Simi Valley, CA 93065