Design of High Speed Wallace-Tree Multiplier Using GDI based full adder: Performance comparison

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Abstract— Design of area optimized very high speed circuits less power utilization is a major concern for the VLSI (very large scale integration) circuit designers. Most of the arithmetic operations are performed using multiplier, which is the more power utilizing block in the digital circuits. In this paper, GDI (Gate Diffusion Input) logic is used to design a full adder in order to achieve low power consumption, optimized area and high speed 16-bit Wallace-tree multiplier. Wallace-tree multiplier designed using GDI logic need less number of transistors; substantially dissipate less power consumption as compare to conventional CMOS logic. The design is synthesized using LT-Spice tool.

Keywords— *VLSI; GDI; CMO; LT-SPICE.*

I. INTRODUCTION

The working of the processor basically relies upon the multiplier, because most of the processors time depends on the arithmetic operation called multiplication process. Essential applications like VLSI (very large scale integration), Digital signal processing requires high speed processors to acquire the handling of large amount of data. The procedure associated with the multipliers is calculation of partial products and then addition of partial products. CMOS (Complementary metal oxide semiconductor) multipliers involve significant zone and power in computerized circuits.

In recent years a great deal of research work has been completed [1][2][3][4][5]and [6] is going on to decrease the time delay and complexity of the multiplier circuit. In [1], a novel technique is utilized to reduce the complexity of the multiplier circuit with help of half adder. In addition to method used in [2], one all the more half adder is constituted to the right side column [4], so that there is a drastic reduction in area. In [5], half adder and full adders of second stage multiplier are replaced by XOR-XNOR gate, which acquires very high speed of operation. In [6] a full adder using 4:1 multiplexer is utilized to diminish the energy.

To further optimize power and area it is required to diminish the number of devices in the design of multipliers. Standard static CMOS logic, PTL(pass transistor logic) and transmission gates are the very important logic styles in the design of full adders[7] used in multipliers PTL(pass transistor logic) has a lot of advantages than CMOS technology, less power utilization because of less number of transistors[8], circuit design in PTL also has cut in voltage drop throughout the pass transistor leads to reduce the sink and source current, so that speed reduces at low supply voltages and high voltage as the input at the restoring inverter is not V_{DD}[9].

The aim of this work is to design a Wallace-tree multiplier circuit with optimized full adder, AND gates and half adder using GDI technique. Section II presents an overview of basic GDI technology, Section III explains the conventional CMOS full adder, Section IV deals with the proposed full adder, Section V enlightens the function of Wallace-tree multiplier, Section VI is all about result analysis and Section VII concludes the paper.

II. GDI (Gate Diffusion Input)

GDI technique is a novel approach to design area optimized very high speed circuits. GDI technique uses a simple logic cell design as illustrate in Fig1 [10]. GDI(Gate Diffusion Input) cell has common gate terminal, source/drain of pMOS, source /drain of nMOS and bulk terminal of both (pMOS and nMOS) the transistors connected to P or N terminals correspondingly.

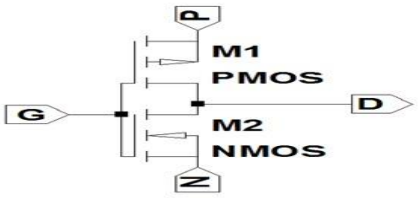

Fig.1. Basic GDI cell

The basic functions put into practice in GDI logic are as appeared in Table 1.

TABLE 1. GDI Function

N	P	D	G	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
0	1	A	A	NOT

GDI cell occupy small silicon area because it contains less number of transistor count, as the area is less node capacitance value is also less [11]. Due to this the operating speed of the GDI is high, which shows that GDI logic style is proficient method of design.The threshold voltage V_{th} of the transistor cell relies up on source terminal to bulk voltage [12]. In order to minimize the bulk effect the bulk terminal of both the transistor connected with their diffusion, change in threshold voltage V_{th} due to change in V_{SB} is called body effect.

III. CMOS FULL ADDER

A full adder circuit designed using CMOS has three input terminals (A, B and C_{in}) and two yield terminals (SUM, Cout) [13]. It is constructed with two Exclusive–OR gates and one 2:1 multiplexer. In this sum is generated at second Exclusive –OR gate and output of multiplexer is C_{out}. It is a 10 transistor full adder, in this each XOR gate is designed with 4 transistors and multiplexer designed with 2 transistors. This circuit consumes more power and occupies larger area. In order to avoid the disadvantage of existed circuit, im proposed a gate diffusion input logic full adder.

IV. PROPOSED FULL ADDER

Fig.2. signifies the block diagram of full adder circuit realized with 2 XOR gate and a 2:1 multiplexer. Output SUM is generated at XOR gate and C_{out} is generated at multiplexer output.

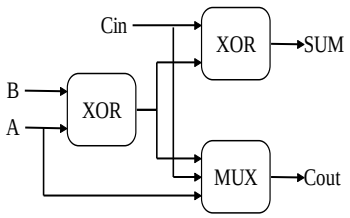

Fig.2. Block diagram of full adder

TABLE 2. Truth table of one bit full adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$SUM = (A \oplus B) \oplus C_{in} \quad \text{.....1}$$

$$C_{out} = A \oplus X \quad \text{.....2}$$

The straight way to plan a full adder design using XOR gate and multiplexer is as revealed in Fig 3. The proposed full adder circuit needs only 8 transistors, XOR gate designed with 3 transistors and multiplexer designed using only 2 transistors.

Fig.3. signifies the proposed full adder circuit with 8 transistors such as T1, T2, T3, T4, T5, T6, T7 and T8 [14]. Transistor T1, T2 and T3 combination acts as XOR gate, output of first XOR gate connected to input of second XOR gate with T4, T5 and T6 transistor combination which produce SUM as output. A full adder includes double numbers and records for values conveyed in and in addition out. A one-bit full adder includes three one-bit numbers, frequently composed as A, B, and C_{in}; A and B are the operands, and Cin is a bit conveyed in from the past less-noteworthy stage. The basic way of a full adder goes through both XOR-gates and closures at the whole bits.

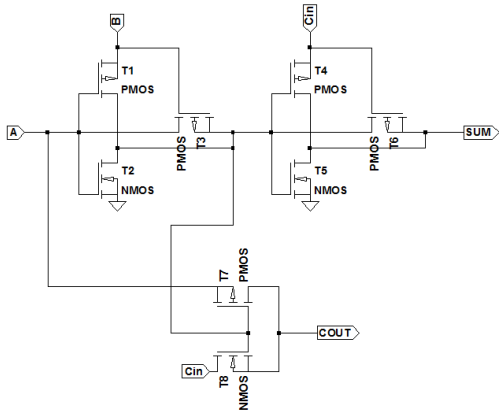

Fig.3. GDI Full adder

Two AND gates and one OR gate of full adder replaced with a multiplexer in proposed circuit. Here output obtained from first XOR gate is also applied as input to the gate terminal of the transistor T7 and T8, input A is connected to drain of T7 as well as C_{in} input connected at the source of transistor T8. The combination of transistor connection T7 and T8 acts as multiplier.

In usual CMOS full adder 10 transistors are used to build a complete full adder, but in proposed GDI based full adder circuit the number of transistors used to design a complete circuit is 8.

V. DESIGN OF WALLACE-TREE MULTIPLIER

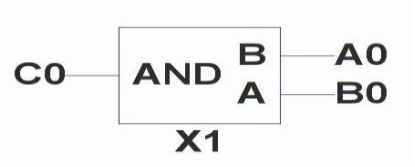

Fig.4. Partial Product

The multiplier bits starts from A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0 multiplied with multiplicand bits B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0

In this 16-bit Wallace-tree multiplier A0 to A15 bits are multiplied with B0 to B15 bits. One among that is as shown in Fig 4. After multiplication of binary bits the resultant partial products are represented in 16 rows [15].

There are few main steps to design Wallace-tree multiplier, Step1: Multiply every bit multiplier with every bit of multiplicand as shown in Fig 5. Step2: Let the initial three rows of multiplier partial products and minimize them into two rows with help of half adders and full adders, repeat the same procedure until two rows obtained.

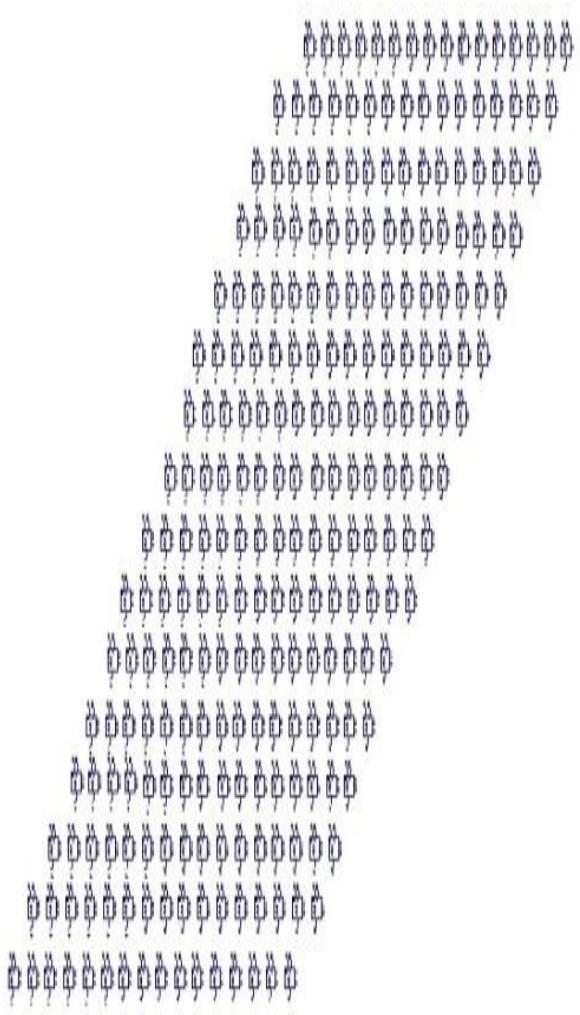

Fig.5. 16*16 partial products

Each group of three rows is diminished by utilizing full adders and half adders.

Eight transistor full adders are utilized as a part of every segment where there are three bits. Half adders are utilized as a part of every segment where there are two bits. Any single bit in a column is passed to the following stage in a similar column without processing. This diminishment system is rehashed in each progressive stage until the point when just two rows remain

Fig.6. of 16*16 bit Wallace-tree multiplier; in initial step we obtain 16 rows of multiplied 256 partial products. In stage one, all the 16 rows of partial products are bifurcated into 5 parts of which primary three rows selected and reduced them into two rows by using GDI full adders and half adders. All the 5 parts of stage one used 145 full adders and 15 half adders. In the subsequent stage the same process continued and 61 full adders and 17 half adders are used to reduce the hard ware. In stage 3 of Wallace-tree multiplier 15 full adders and 8 half adders are used to reduce the complexity.

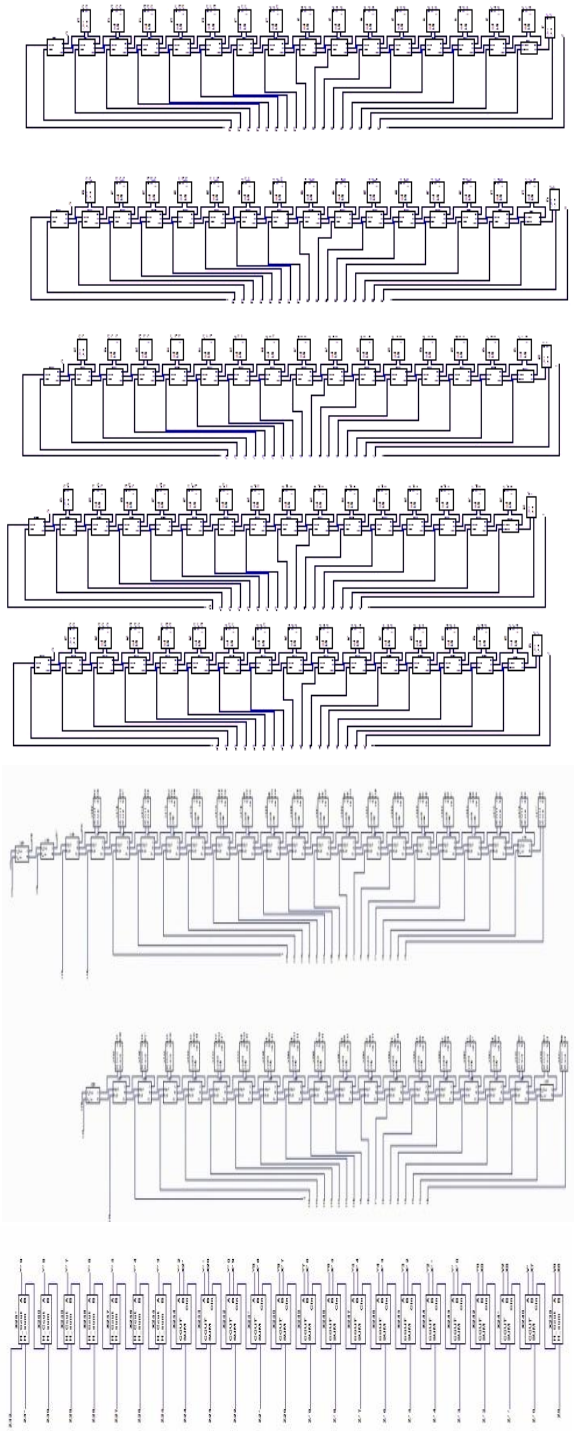

Fig.6. 16*16 Wallace-tree Multiplier.

VI. RESULT

The functionality of proposed 16- bit Wallace-tree multiplier is verified using LT-Spice tool implemented on BASYS-3, Artix-7 FPGA Device. The whole investigation is tabulated in table 2. The Fig of transistors used to design a CMOS based Wallace-tree multiplier is 2490, where as in proposed GDI based Wallace-tree multiplier transistor count reduced to a great extent i.e. 1968, when there is a decrease in the number of transistor count in GDI based full adder circuit leads to reduce the overall transistor count in Wallace-tree multiplier. If the area is optimized then the operating speed of the circuit increase, delay decrease and power utilized by the circuit decreases.

TABLE 2. Comparative analysis

Parameter	Wallace-tree multiplier using GDI	Wallace-tree multiplier using CMOS
No. of bits	16	16
No. of transistors	1968	2490
Delay(ns)	6.231	8.486
Power(mW)	52.32	83.22

VII. CONCLUSION

A simple logic is proposed in this paper in order to minimize the area of Wallace-tree multiplier using GDI full adder. From the above analysis it is observed that the Area is reduced almost 21%, Delay is reduced 27% and the power is reduced 38%. Hence Proposed Wallace-tree multiplier is occupying less area, less delay and utilized less power compare to CMOS Wallace-tree multiplier technique.

REFERENCES

[1]. R. S. Waters, E. E. Swartzlander, "A reduced complexity Wallace multiplier reduction," IEEE Transactions on Computers, vol. 59, no. 8, pp.1134-1137, 2010.

[2]. Shahzad Asif and Yinan Kong, "Low Area Wallace Multiplier," VLSI Design, vol. 2014.

[3]. M. J. Rao, S. Dubey, "A high speed and area efficient Booth recoded Wallace-tree multiplier for Fast Arithmetic Circuits," in Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Hyderabad, India, 5-7 Dec. 2012, pp.220-223.

[4]. Karthick, S. Karthika and S. Valannathy, "Design and Analysis of Low Power Compressors," International Journal of Advanced Research in Electrical, Electronics and instrumentation Engineering, YoU, Issue 6, Dec. 2012.

[5]. S. Murugeswari, S. K. Mohideen, "Design of area efficient and low power multipliers using multiplexer based full adder," in 2nd International Conference on Current Trends in Engineering and technology (ICCTET), Enathi, India, July 2014, pp.388-392.

[6]. Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder," IEEE transactions on circuits and systems, vol. 51, no. 7, July 2004, pp. 345-348.

[7]. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," Solid-State Circuits, IEEE Journal of, vol. 32, pp.1079-1090, 1997.

[8]. Jaume Segura, Charles F. Hawkins CMOS electronics: how it works, how it fails, Wiley-IEEE, 2004, page 132.

[9]. A. P. Chandrakasan, R. W. Brodersen, "Minimizing Power Consumption in Digital CMOS Circuits", Proceedings of the IEEE, vol. 83, no. 4, pp. 498-523, April 1995.

[10]. Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish,"Gate Diffusion Input (GDI) Logic in standard CMOS Nanoscale process", IEEE 26th Convention of Electrical and Electronics Engineers, Israel, 2010.

[11]. Biswarup Mukherjee and Aniruddha Ghosal, "Design & Study of a Low Power High Speed Full Adder Using GDI Multiplexer",978-1-4799-8349-0/15/ ©2015 IEEE

[12]. K. Roy, S. Mukhopadhyay, H. Mahmoodi- Meimand, "Leakage Current Mechanism and Leakage Reduction Techniques in Deep Submicrometer CMOS circuits", proceedings of the IEEE, vol. 91, no. 2, Feb 2003.

[13]. CMOS digital integrated circuits By Sung-Mo Kang, Yusuf Leblebici , McGraw-Hill Professional, 2002.

[14]. Korra Ravi kumar, Mahipal reddy,M.Sadanandam, Santhosh kumar, M.Raju, "Design of 2T XOR Gate Based Full Adder Using GDI Technique", 978-1-5090-5960-7/17/ ©2017 IEEE.

[15]. Kokila Bharti Jaiswal1 , Nithish Kumar V1 , Pavithra Seshadri2 and Lakshminarayanan G1, "Low Power Wallace Tree Multiplier Using Modified Full Adder", 978-1-4673-6823-0/15/c 2015 IEEE