Optimization of Domino Logic Circuit using 22nm FinFET Technology for Low Power and High Speed Applications

RitikaSingh[1], Prince Nagar[2]
[1]*M.tech Scholar, Sharda University, Greater Noida, UP, India*
[2]*Assistant Professor, Sharda University, Greater Noida, UP, India*

Abstract- CMOS technology is the most feasible semiconductor technology but it fails to perform as per expectations beyond and at 32nm technology node due to the short channel effects. Multigate FET technology like DGFET has FINFET category is the most viable successor of MOSFETs at 32nm and beyond. The MOSFET has been used widely in current technology. But below 32nm technology, controlling the channel of the MOSFET becomes difficult. So there is need to invent newtechnology which will allow us to design devices below 32nm technology. Fin-type field-effect transistors (FinFET)are promising substitutes forbulk CMOS at the nanoscale. In this paper, we design a Low Power &High Speed FinFET based Domino Logic Circuits which is based on technique foot driven stack transistor based on FinFET Technology in 22nm model. The results show that the Average Power Consumption, delay, PDP and EDP are improved. Simulations are performed on HSPICE software. The circuits designed are OR and AND Gate based on FINFET Foot Driven Stack Transistor.

Keywords- FinFET, Domino, 32nm, Foot Driven, 22nm

I. INTRODUCTION

As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for non-portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. [1] Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. [2] This project explores how circuits based on FinFET (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs. [3]

The desire to optimize the design metrics of performance, power, area, cost, and time to market (opportunity cost) has not changed since the inception of the IC industry. In fact, Moore's Law is all about optimizing those parameters. [5] [4] However, as scaling of manufacturing nodes progressed towards 20-nm, some of the device parameters could not be scaled any further, especially the power supply voltage, the dominant factor in determining dynamic power. And optimizing for one variable such as performance automatically translated into big compromises in other areas, like power. [6] Designing in FinFET broadens the design window once again. Operating voltage continues to scale down, significantly saving on dynamic and static power. Short channel effects are reduced significantly, reducing the guard-banding needed to deal with variability. And performance continues to improve compared to planar at an identical node. In fact, at very low power supply voltages, the performance advantage of the FinFET compared to its planar equivalent widens due to the superior gate control of the channel in the FinFET. [7] For memory designers, an added advantage of FinFET is the significantly lower retention voltage requirements of FinFET-based SRAMs compared to planar FETs. [8]

1. Domino Logic based on Foot Drive Stack Transistor using MOSFET:

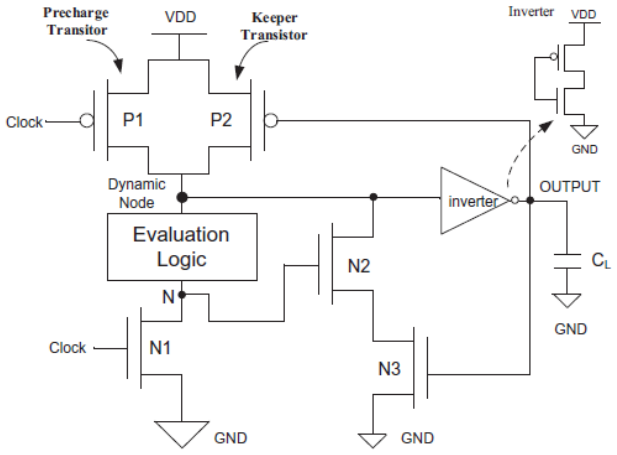

Fig.1: Foot Drive Stack Transistor based on MOSFET [1]

In figure 1, the circuit chart of Foot Driven Stack Transistor dependent on MOSFET is shown. The circuit has two segments, input area has a PMOS precharge transistor P1, evaluation arrange comprising of NMOS transistors in parallel and a footer transistor N1 though output segment includes attendant transistor P2, static inverter and stacked NMOS transistors N2 and N3. The contributions to the circuit are connected through gate of the NMOS transistors in evaluation

organize. Transistor N2 is driven by the voltage at the foot N of evaluation organize though transistor N3 is driven by the output voltage. Transistors N2 and N3 are utilized in a stack setup. At whatever point
there is a voltage drop crosswise over N1 because of noise pulses, transistor N3 gives stacking impact by making the gate to source voltage of N2 littler. This will diminish the spillage intensity of N2 and makes N1 direct less. The circuit works in two stages:
I) Precharge stage: During the precharge stage, the clock is low. Thusly, transistor P1 turns ON. The dynamic node charges to VDD and output of the circuit goes low because of the nearness of inverter. This output drives the manager transistor turning it ON and keeps up the dynamic node to high voltage. Subsequently, keeping any undesirable release of dynamic node because of noise. As of now, transistor N1 kills, as the clock is low. In this way, keeping any release of dynamic node. As of now, inputs are connected however since N1 is OFF, in this way these sources of info have no impact on output. Presently, on the off chance that any of the contributions to PDN is high, at that point the voltage of node N will be almost equivalent to the voltage at the dynamic node in light of the fact that N1 is OFF in precharge mode. As of now, N2 turns ON while N3 stays OFF because of low voltage at the output. Subsequently, spillage control utilization of circuit decreases and noise execution improves.
ii) Evaluation stage: During the Evaluation stage, the clock is high. Along these lines, transistor P1 kills and transistor N1 turns ON. Right now, inputs are connected in the evaluation logic. In the event that any of the contributions to the evaluation logic goes high amid this stage, the relating N channel MOSFET turns on associating the dynamic node to ground. Subsequently, dynamic node releases to low voltage and output of the circuit goes high which is as per the logic of OR gate.
Here transistors N2 and N3 turn ON and OFF on the other hand decreasing the spillage current in the circuit. Here transistor N3 fills in as stack transistor. A deferral is there between releasing of the dynamic node and charging of the output node because of the nearness of inverter between dynamic node and output.

2. Proposed Circuit od Domino Foot Driven Stack Transistor based on FinFET Technology:

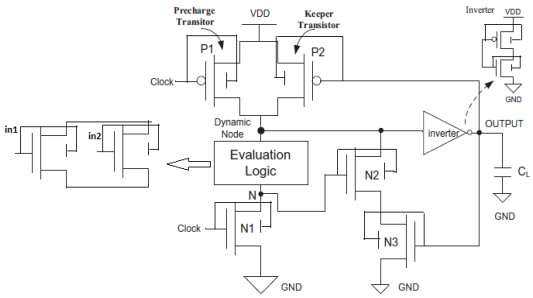

Fig.2: FinFET based Foot Drive Stack Transistor based OR GATE proposed

Figure 2 presents FinFET based OR gate with proposed domino technique.

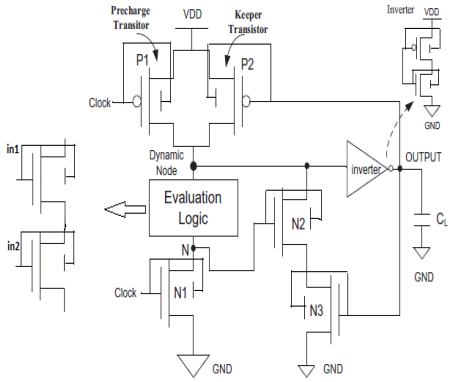

Fig.3: FinFET based Foot Drive Stack Transistor based AND GATEproposed

Figure 3 presents FinFET based AND gate with proposed domino technique. The working is same as the MOSFET based only FinFET are replaced in short gate mode.

3. Simulation Results:

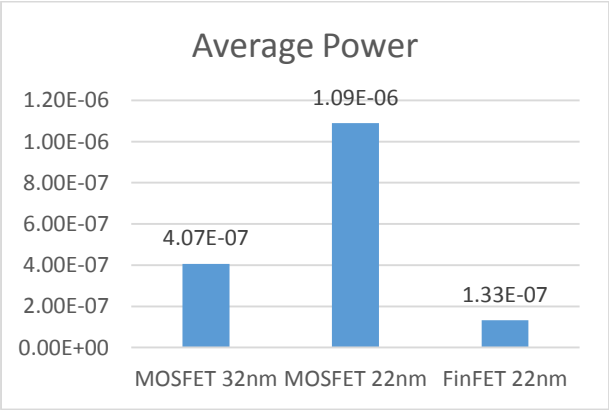

Fig.4: Average Power Consumption OR Gate between MOSFET 32nm, 22nm and FinFET 22nm

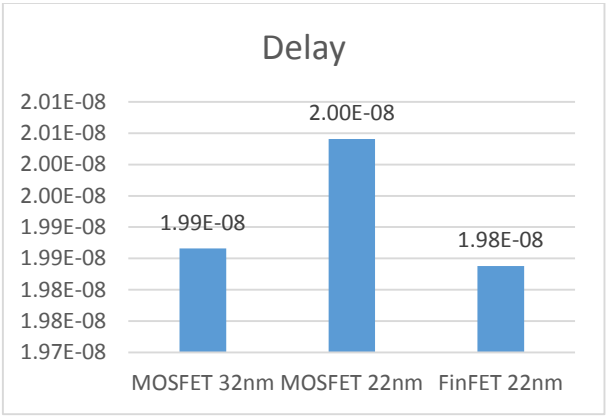

Fig.5: Delay OR Gate between MOSFET 32nm, 22nm and FinFET 22nm

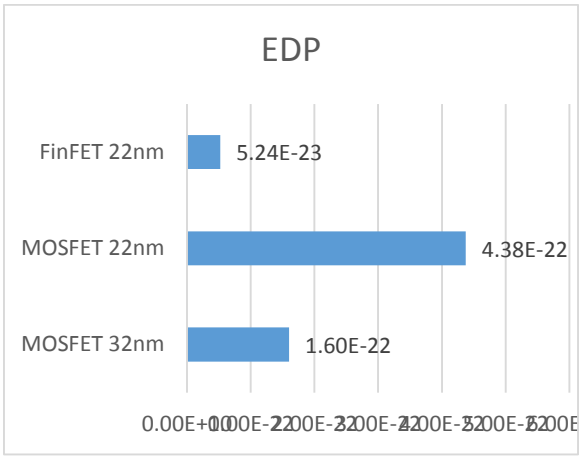

Fig.6: EDP OR Gate between MOSFET 32nm, 22nm and FinFET 22nm

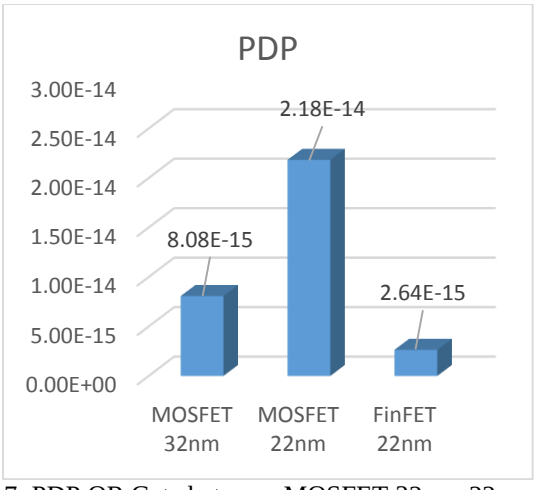

Fig.7: PDP OR Gate between MOSFET 32nm, 22nm and FinFET 22nm

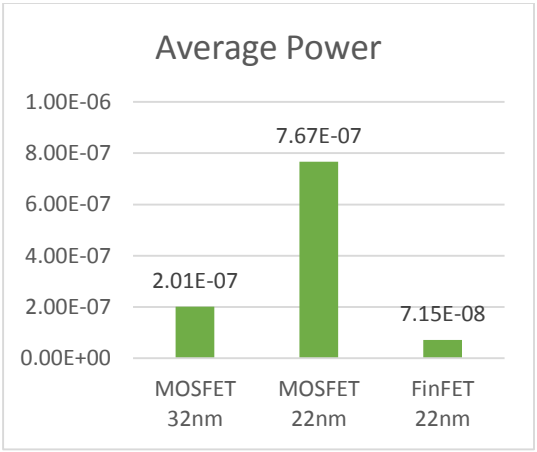

Fig.8: Average Power Consumption AND Gate between MOSFET 32nm, 22nm and FinFET 22nm

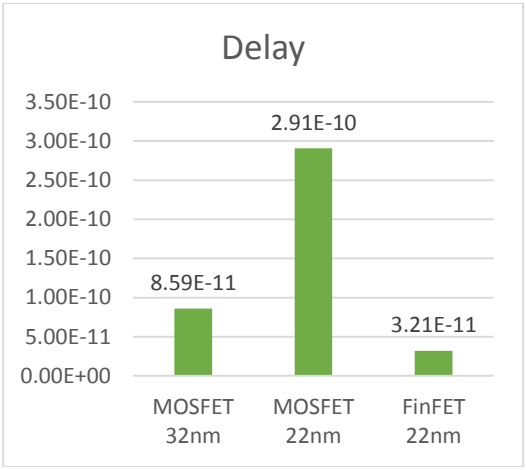

Fig.9: Delay AND Gate between MOSFET 32nm, 22nm and FinFET 22nm

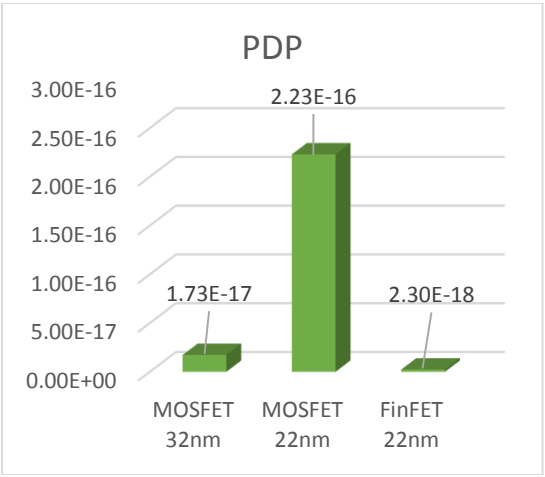

Fig.10: PDP AND Gate between MOSFET 32nm, 22nm and FinFET 22nm

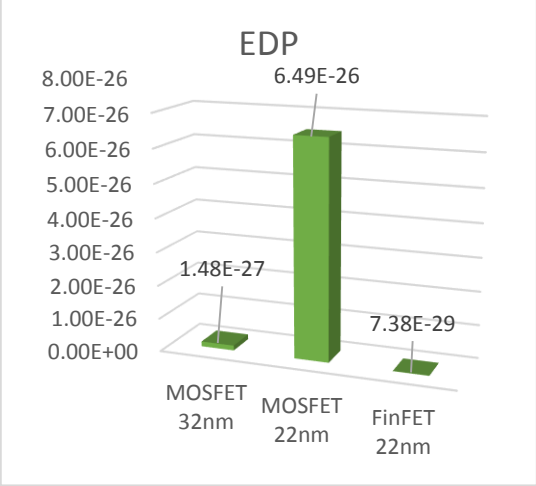

Fig.11: EDP AND Gate between MOSFET 32nm, 22nm and FinFET 22nm

IV. CONCLUSION

Simulation results show that Domino FinFET based Foot Driven Stack Transistor technique have improved speed and a lower consumption of average power, PDP and EDP.With FinFET Technology we can accomplish low power and decreased short channel effects as seen in 22nm results of MOSFET, so the FinFET based domino circuit can be utilized as a part of low power VLSI applications with reduced short channel effects. In view of the utilization of FinFET innovation we can decrease the postponement speed altogether so this FinFET based Foot Driven Stack Transistor Domino Logic can be utilized as a part of planning recollections with high performance beneath 32nm and specially at 22nm and furthermore in fast applications proficiently.

V. REFERENCES

[1]. M. Anis, S. Areibi, M. Elmasry, Design and optimization of multi-threshold CMOS (MTCMOS) circuits, IEEE Trans. Comput. Aided Design Integr. Circuits Syst. 22 (10) (2003) 1324–1342.

[2]. K. Roy, S. Mukhopadhyay, H. Mahmoodi, Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits, Proc. IEEE 91 (2) (2003) 305–327.

[3]. T.K. Gupta, A.K. Pandey, O.P. Meena, Analysis and design of lector-based dual-Vt domino logic with reduced leakage current, Circuit World 43 (3) (2017) 97–104.

[4]. A. Peiravi, M. Asyaei, Robust low leakage controlled keeper by currentcomparison domino for wide fan-in gates Integration, VLSI J. 45 (1) (2012)

[5]. E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C.-T. Chuang, K. Bernstein, and R. Puri, "Turning silicon on its edge," IEEE Circuits and Devices Magazine, vol. 20, no. 1, pp. 20–31, Jan.-Feb. 2004.

[6]. H.-S. P. Wong, K. K. Chan, and Y. Taur, "Self-aligned (top and bottom) double-gate MOS- FET with a 25 nm thick silicon channel," in Proc. Int. Electronic Device Mtg., Dec. 1997, pp. 427–430.

[7]. T.-J. King, "FinFETs for nanoscale CMOS digital integrated circuits," in Proc. Int. Conf. Computer-Aided Design, Nov. 2005, pp. 207–210.

[8]. "Circuit design of 2 i/p reconfigurable Dynamis Logic based on DG MOSFETs with whole set of 16 functions", Junki Kato, CES, 2014

[9]. "Short Channel Effects in FinFet" Zhichao Lu, IEEE, Vol 28, Feb- 2007

[10]."Design of Logic Gates and Flip-Flops in High-performance FinFet Technology" Ajay N. Bhoj and Niraj K. Jha, IEEE, 2013